## Basic Electronics Subject Code: BE-2101



# Debashis De 

With contributions from Kamakhya Prasad Ghatak

# BASIC ELECTRONICS 

First Year

Biju Patnaik University of Technology, Orissa
Subject Code: BE-2101

Debashis De<br>Associate Professor<br>Department of Computer Science and Engineering<br>West Bengal University of Technology, Kolkata

With contributions from
Kamakhya Prasad Ghatak

## PEARSON

Delhi • Chennai • Chandigarh

This publishers would like to thank H. N. Pratihari of Orissa Engineering College, Bhubaneswar, for his help in mapping the contents of this book to the requirements of Biju Patnaik University of Technology, Orissa.

## Copyright © 2012 Dorling Kindersley (India) Pvt. Ltd

Licensees of Pearson Education in South Asia
No part of this eBook may be used or reproduced in any manner whatsoever without the publisher's prior written consent.

This eBook may or may not include all assets that were part of the print version. The publisher reserves the right to remove any material present in this eBook at any time.

## CONTENTS

Preface ..... $x i$
Roadmap to the Syllabus ..... xiii
About the Author ..... $x v$
1 Operational Amplifier ..... 1-1
1-1 Introduction to Electronics ..... 1-1
1-2 The Operational Amplifier ..... 1-5
1-3 Properties of the Ideal Operational Amplifier ..... 1-5
1-4 Specifications of IC 741C ..... 1-6
1-4-1 Description of Op-Amp 741 IC Pins ..... 1-6
1-5 Operational Amplifier and Its Terminal Properties ..... 1-7
1-5-1 Input Offset Voltage and Output Offset Voltage ..... 1-8
1-5-2 Input-Bias Current ..... 1-8
1-5-3 Input Offset Current and Output Offset Current ..... 1-10
1-5-4 Input Offset Null Voltage ..... 1-12
1-5-5 Differential Input Resistance ..... 1-13
1-5-6 Input Capacitance ..... 1-13
1-5-7 Offset Voltage Adjustment Range ..... 1-13
1-5-8 Input Voltage Range ..... 1-13
1-5-9 Common-Mode Rejection Ratio (CMRR) ..... 1-13
1-5-10 Supply Voltage Rejection Ratio (SVRR) ..... 1-15
1-5-11 Large Signal Voltage Gain ..... 1-15
1-5-12 Output Voltage Swing ..... 1-15
1-5-13 Output Resistance ..... 1-16
1-5-14 Supply Voltage ..... 1-16
1-5-15 Supply Current ..... 1-16
1-5-16 Power Consumption ..... 1-16
1-5-17 Slew Rate ..... 1-16
1-5-18 Gain Bandwidth Product ..... 1-18
1-5-19 Virtual Ground ..... 1-18
1-6 Applications of the Operational Amplifier ..... 1-19
1-6-1 Inverting Mode of Operation ..... 1-19
1-6-2 Non-Inverting Mode of Operation ..... 1-20
1-6-3 Voltage Summing, Difference, and Constant Gain Multiplier ..... 1-21
1-6-4 Voltage Follower or Unity Gain Amplifier ..... 1-25
1-6-5 Comparator ..... 1-25
1-6-6 Integrator ..... 1-26
1-6-7 Differentiator ..... 1-29
1-6-8 Logarithmic Amplifier ..... 1-30
1-7 Real-Life Applications ..... 1-47
Points to Remember ..... 1-47
Important Formulae ..... 1-47
Objective Questions ..... 1-48
Review Questions ..... 1-49
Practice Problems ..... 1-50
Suggested Readings ..... 1-51
2 Diode Fundamentals ..... 2-1
2-1 Introduction ..... 2-1
2-2 Formation of the $p-n$ Junction ..... 2-2
2-3 Energy Band Diagrams ..... 2-2
2-3-1 The p-n Junction at Thermal Equilibrium ..... 2-2
2-4 Concepts of Junction Potential ..... 2-4
2-4-1 Space-Charge Region ..... 2-4
2-4-2 Built-in and Contact Potentials ..... 2-4
2-4-3 Effect of Doping on Barrier Field ..... 2-5
2-4-4 Formulation of Built-in Potential ..... 2-7
2-5 Modes of the $\boldsymbol{p}-\boldsymbol{n}$ Junction ..... 2-9
2-5-1 The p-n Junction with External Applied Voltage ..... 2-9
2-5-2 Rectifying Voltage-Current Characteristics of a $\mathrm{p}-\mathrm{n}$ Junction ..... 2-10
2-5-3 The Junction Capacitance ..... 2-11
2-5-4 The Varactor Diode ..... 2-19
2-6 Derivation of the I-V Characteristics of a $\boldsymbol{p}-\boldsymbol{n}$ Junction Diode ..... 2-21
2-7 Linear Piecewise Models ..... 2-37
2-8 Breakdown Diode ..... 2-38
2-8-1 Zener Breakdown ..... 2-38
2-8-2 Avalanche Breakdown ..... 2-39
Points to Remember ..... 2-46
Important Formulae ..... 2-48
Objective Questions ..... 2-49
Review Questions ..... 2-52
Practice Problems ..... 2-53
Suggested Readings ..... 2-60
3 Diode Circuits ..... 3-1
3-1 Introduction ..... 3-1
3-2 Analysis of Diode Circuits ..... 3-1
3-3 Load Line and $Q$-point ..... 3-2
3-4 Zener Diode as Voltage Regulator ..... 3-4
3-4-1 Line Regulation ..... 3-5
3-4-2 Load Regulation: Regulation with Varying Load Resistance ..... 3-6
3-5 Rectifiers ..... 3-10
3-5-1 Half-Wave Rectifier ..... 3-10
3-5-2 Full-Wave Rectifier ..... 3-12
3-5-3 Use of Filters in Rectification ..... 3-14
3-5-4 Regulation ..... 3-16
3-5-5 Performance Analysis of Various Rectifier Circuits ..... 3-17
3-6 Clipper and Clamper Circuits ..... 3-29
3-6-1 Clipper ..... 3-29
3-6-2 Clamper ..... 3-35
3-7 Comparators ..... 3-38
3-8 Additional Diode Circuits ..... 3-39
3-8-1 Voltage Multiplier ..... 3-39
3-8-2 Peak Detector ..... 3-39
3-8-3 Digital Circuits ..... 3-40
3-8-4 Switching Regulators ..... 3-40
3-9 Special types of $p-n$ Junction Semiconductor Diodes ..... 3-47
3-9-1 Tunnel Diode ..... 3-47
3-9-2 Light-Emitting Diode ..... 3-50
3-9-3 Photo Detector Diode ..... 3-51
3-9-4 Photovoltaic Diode ..... 3-53
3-10 Applications of Diode ..... 3-55
3-10-1 Radio Demodulation ..... 3-55
3-10-2 Power Conversion ..... 3-55
3-10-3 Over-Voltage Protection ..... 3-55
3-10-4 Logic Gates ..... 3-55
3-10-5 Ionizing Radiation Detectors ..... 3-55
3-10-6 Temperature Measuring ..... 3-56
3-10-7 Charge-Coupled Devices ..... 3-56
Points to Remember ..... 3-56
Important Formulae ..... 3-58
Objective Questions ..... 3-59
Review Questions ..... 3-61
Practice Problems ..... 3-62
Suggested Readings ..... 3-66
4 BJT Fundamentals ..... 4-1
4-1 Introduction ..... 4-1
4-2 Formation of $p-n-p$ and $n-p-n$ Junctions ..... 4-2
4-3 Transistor Mechanism ..... 4-2
4-4 Energy Band Diagrams ..... 4-3
4-5 Transistor Current Components ..... 4-4
4-5-1 Current Components in p-n-p Transistor ..... 4-5
4-5-2 Current Components in $\mathrm{n}-\mathrm{p}-\mathrm{n}$ Transistor ..... 4-7
4-6 CB, CE and CC Configurations ..... 4-8
4-6-1 Common-Base (CB) Mode ..... 4-8
4-6-2 Common-Emitter (CE) Mode ..... 4-8
4-6-3 Common-Collector (CC) Mode ..... 4-9
4-7 Expression for Current Gain ..... 4-10
4-7-1 Relationship Between $\alpha$ and $\beta$ ..... 4-11
4-8 Transistor Characteristics ..... 4-12
4-8-1 Input Characteristics ..... 4-12
4-8-2 Output Characteristics ..... 4-13
4-9 Operating Point and the Concept of Load Line ..... 4-17
4-10 Early Effect ..... 4-18
4-11 Transistor as Amplifier ..... 4-24
4-11-1 The Parameter $\alpha^{\prime}$ 4-25
4-12 Expressions of Current Gain, Input Resistance, Voltage Gain and Output Resistance ..... 4-26
4-12-1 Current Gain ( $A_{1}$ ) ..... 4-26
4-12-2 Input Resistance ( $R_{\text {, }}$ ) ..... 4-27
4-12-3 Voltage Gain ( $A_{V}$ ) ..... 4-27
4-12-4 Output Resistance ( $R_{0}$ ) ..... 4-28
4-13 Frequency Response for CE Amplifier With and Without Source Impedance ..... 4-28
4-13-1 Conclusions 4-28
4-14 Emitter Follower ..... 4-30
Points to Remember ..... 4-34
Important Formulae ..... 4-35
Objective Questions ..... 4-35
Review Questions ..... 4-38
Practice Problems ..... $4-39$
Suggested Readings ..... 4-43
5 BJT Circuits ..... 5-1
5-1 Introduction ..... 5-1
5-2 Biasing and Bias Stability ..... 5-2
5-2-1 Circuit Configurations ..... 5-2
5-2-2 Stabilization Against Variations in $I_{C O} V_{B E}$, and $\beta$ ..... 5-7
5-3 Calculation of Stability Factors ..... 5-9
5-3-1 Stability Factor $S$ ..... 5-9
5-3-2 Stability Factor $S^{\prime}$ ..... 5-10
5-3-3 Stability Factor $S^{\prime \prime}$ ..... 5-10
5-3-4 General Remarks on Collector Current Stability ..... 5-11
5-4 CE, CB Modes and their Properties ..... 5-12
5-4-1 Common-Emitter (CE) Mode ..... 5-12
5-4-2 Common-Base Mode ..... 5-14
5-5 Small-Signal Low-Frequency Operation of Transistors ..... 5-23
5-5-1 Hybrid Parameters and Two-Port Network ..... 5-23
5-6 Equivalent Circuits through Hybrid Parameters as a Two-Port Network ..... 5-25
5-7 Darlington Pair ..... 5-25
5-8 Transistor at High Frequencies ..... 5-26
5-9 Real-Life Applications of the Transistor ..... 5-26
Points to Remember ..... 5-27
Important Formulae ..... 5-28
Objective Questions ..... 5-29
Review Questions ..... 5-29
Practice Problems ..... 5-30
Suggested Readings ..... 5-32
6 Feedback Amplifier ..... 6-1
6-1 Introduction ..... 6-1
6-2 Conceptual Development Through Block Diagrams ..... 6-2
6-2-1 Input Signal ..... 6-2
6-2-2 Output Signal ..... 6-2
6-2-3 Sampling Network ..... 6-2
6-2-4 Comparison or Summing Network ..... 6-3
6-2-5 Basic Amplifier ..... 6-4
6-3 Properties of Negative Feedback ..... 6-4
6-4 Calculations of Open-Loop Gain, Closed-Loop Gain and Feedback Factors ..... 6-4
6-4-1 Loop Gain or Return Ratio 6-6
6-5 Topologies of the Feedback Amplifier ..... 6-7
6-5-1 Voltage-Series or Series-Shunt Feedback ..... 6-7
6-5-2 Current-Series or Series-Series Feedback ..... 6-7
6-5-3 Current-Shunt or Shunt-Series Feedback ..... 6-8
6-5-4 Voltage-Shunt or Shunt-Shunt Feedback ..... 6-8
6-6 Effect of Feedback on Gain, Input and Output Impedances ..... 6-9
6-6-1 Effect of Feedback on Input Impedance ..... 6-9
6-6-2 Effect of Feedback on Output Impedance ..... 6-12
6-7 Practical Implementations of the Feedback Topologies ..... 6-13
6-7-1 Voltage-Series Feedback Using Transistor ..... 6-14
6-7-2 Current-Series Feedback Using Transistor ..... 6-14
6-7-3 Voltage-Shunt Feedback Using Transistor ..... 6-15
6-7-4 Current-Shunt Feedback Using Transistor ..... 6-16
6-8 Sensitivity ..... 6-17
6-9 Bandwidth Stability ..... 6-18
6-10 Effect of Positive Feedback ..... 6-19
6-10-1 Instability and Oscillation ..... 6-20
6-10-2 Nyquist Criterion ..... 6-20
6-10-3 Condition of Oscillation ..... 6-20
6-10-4 Barkhausen Criterion ..... 6-21
Points to Remember ..... 6-42
Important Formulae ..... 6-43
Objective Questions ..... 6-43
Review Questions ..... 6-44
Practice Problems ..... 6-45
Suggested Readings ..... 6-45
7 Oscillators ..... 7-1
7-1 Introduction ..... 7-1
7-2 Classifications of Oscillators ..... 7-2
7-3 Circuit Analysis of a General Oscillator ..... 7-2
7-3-1 Hartley Oscillator ..... 7-5
7-3-2 Colpitts Oscillator ..... 7-6
7-3-3 Phase-Shift Oscillator ..... 7-7
7-3-4 Wien-Bridge Oscillator ..... 7-9
7-4 Conditions for Oscillation: Barkhausen Criterion ..... 7-11
7-4-1 Nyquist Criterion for Oscillation ..... 7-11
7-5 Tuned Oscillator ..... 7-12
7-5-1 Circuit Analysis ..... 7-12
7-6 Crystal Oscillator ..... 7-13
7-7 Real-Life Applications ..... 7-25
7-7-1 Voltage-Controlled Oscillator ..... 7-25
7-7-2 Cascode Crystal Oscillator ..... 7-26
Points to Remember ..... 7-27
Important Formulae ..... 7-27
Objective Questions ..... 7-28
Review Questions ..... 7-31
Practice Problems ..... 7-31
Suggested Readings ..... 7-32
8 Electronic Instruments ..... 8-1
8-1 Introduction ..... 8-1
8-2 Components of the Cathode-Ray Oscilloscope ..... 8-2
8-3 Time-Base Generators ..... 8-2
8-3-1 Oscilloscope Amplifiers ..... 8-4
8-3-2 Vertical Amplifiers ..... 8-4
8-4 Sweep Frequency Generator ..... 8-5
8-4-1 Applications of the Sweep Frequency Generator ..... 8-6
8-5 Measurements Using the Cathode-Ray Oscilloscope ..... 8-6
8-5-1 Measurement of Frequency ..... 8-6
8-5-2 Measurement of Phase ..... 8-7
8-5-3 Measurement of Phase Using Lissajous Figures ..... 8-7
8-6 Types of Cathode-Ray Oscilloscope ..... 8-11
8-6-1 Analog CRO ..... 8-11
8-6-2 Digital CRO ..... 8-11
8-6-3 Storage CRO ..... 8-11
8-6-4 Dual-Beam CRO ..... 8-11
8-7 Cathode-Ray Tube ..... 8-11
8-7-1 Electron Gun ..... 8-11
8-7-2 Deflection Systems ..... 8-12
8-7-3 Fluorescent Screen ..... 8-15
8-8 Sine Wave Generator ..... 8-19
8-9 Square Wave Generator ..... 8-20
8-10 AF Signal Generator ..... 8-22
8-11 Function Generator ..... 8-22
Points to Remember ..... 8-24
Important Formulae ..... 8-24
Objective Questions ..... 8-24
Review Questions ..... 8-25
Practice Problems ..... 8-26
Suggested Readings ..... 8-27
9 Digital Electronic Principles ..... 9-1
9-1 Introduction ..... 9-1
9-2 Number System ..... 9-2
9-3 Conversion of Number System ..... 9-2
9-3-1 Binary to Decimal ..... 9-3
9-3-2 Decimal to Binary ..... 9-3
9-3-3 Numer System Conversions ..... 9-4
9-4 Boolean Algebra ..... 9-5
9-4-1 Addition ..... 9-5
9-4-2 Subtraction ..... 9-7
9-4-3 Basic Boolean Laws ..... $9-8$
9-5 Logic Gates ..... 9-8
9-5-1 AND Gate ..... 9-9
9-5-2 OR Gate ..... 9-9
9-5-3 NOT Gate ..... 9-10
9-5-4 NAND Gate ..... 9-10
9-5-5 NOR Gate ..... 9-10
9-5-6 XOR Gate ..... 9-11
9-5-7 XNOR Gate ..... 9-11
9-5-8 Universal Gate ..... 9-11
9-5-9 Characteristics of Logic Gates ..... 9-13
9-6 De Morgan's Theorem ..... 9-14
9-6-1 Using Basic Logic Gates ..... 9-14
9-6-2 Application of De Morgan's Theorem ..... 9-15
9-7 Simplification of Boolean Expression ..... 9-15
9-8 Logic Gate Circuits ..... 9-17
9-8-1 Combinational Logic ..... 9-17
9-8-2 Sequential Logic Circuit ..... 9-22
9-9 Basic Concepts of Memory ..... 9-33
9-10 Real-Life Applications ..... 9-35
Points to Remember ..... 9-35
Important Formulae ..... 9-35
Objective Questions ..... 9-35
Review Questions ..... 9-36
Practice Problems ..... 9-37
Suggested Readings ..... 9-38
Solved Question Papers ..... Q-1
Index I-1

## PREFACE

Basic Electronics has been written to serve as a comprehensive textbook for first-year students of the B.Tech. programme at Biju Patnaik University of Technology (BPUT), Orissa. The objective of this book is to develop the reader's basic ability to understand electronics as a science. The required concepts from physics and mathematics have been developed throughout the book-and no prior knowledge of physical electronics has been assumed.

This book has been organized in accordance with the syllabus of BPUT. The book breaks down the complex subject of electronics into small and simple units, and explains each one thoroughly with the help of theory, concepts, solved examples and diagrams. The major points of each chapter are recapitulated at the end, and all important formulae have been listed for the benefit of the students. These elements make the book an easy reference guide.

Finally, this book is designed to assist in self-study. Students can test their understanding of each topic by solving the numerous objective and review questions, as well as practical problems, at the end of each chapter. To give an indication of the trend of examination questions, three latest BPUT question papers have been included in the book.

## ACKNOWLEDGEMENTS

I am grateful to my colleagues, students and research scholars at West Bengal University of Technology, University of Western Australia, University of Calcutta, and Bengal Engineering and Science University. I would like to thank Professor K. P. Ghatak (University of Calcutta)—friend, philosopher and guide; Dr Sitangshu Bhattacharya (Indian Institute of Science, Bangalore); and Anushka Roychowdhury (Cognizant Technology Solutions). I would like to thank all the members of Sadananda Bhavan for their constant support and encouragement. To all the reviewers, I am grateful for their valuable feedback and inputs. I would also like to express my gratitude to Pearson Education for kindly agreeing to publish this book. Special thanks are due to Rupesh Singh, Tapan Kumar Saha, Vishwajeet Banik, Thomas Mathew Rajesh, Yajnaseni Das, Preeta Priyamvada Pandey, Jennifer Sargunar and Insiya Poonawala for their support and cooperation. Suggestions and comments to improve this edition further are welcome.

This page is intentionally left blank.

## ROADMAP TO THE SYLLABUS

## MODULE I (11 hours)

1. Introduction to Electronics: Signals, frequency spectrum of signals, analog and digital signals, amplifiers, digital logic inverters.
2. The Operational Amplifier (Op-Amp): The ideal op-amp, inverting and non-inverting configurations, the difference amplifier, CMRR, applications of op-amps (instrumentation amplifier, summing amplifier, integrator and differentiator).

## Refer Chapter 1

3. Semiconductor Diodes: Introduction, the physical operation of $p-n$ junction diodes, characteristics of the $p-n$ junction diodes, zener diodes, rectifier circuits (half-wave, full-wave, bridge and peak rectifiers), diode clipper and clamper circuits, light-emitting diodes.
(4 lectures)

## Refer Chapters 2 and 3

4. BipolarJunction Transistors (BJTs): Simplified structure and physical operation of $n-p-n$ and $p-n-p$ transistors in the active region, current-voltage characteristics of BJT, BJT as an amplifier and as a switch.
(3 lectures)

## Refer Chapter 4

## MODULE II (11 hours)

6. Bipolar Junction Transistors (BJTs): BJT circuits at DC, biasing in BJT amplifier circuits, small signal operation of BJT, the simplified hybrid- $\pi$ model and its application to single-stage BJT amplifiers (common-emitter, common-base and common-collector configurations). (4 lectures)

## Refer Chapter 5

7. Feedback Amplifiers and Oscillators: General feedback structure, properties and advantages of negative feedback, basic principles of sinusoidal oscillators, the Barkhausen criterion, op-amp oscillator circuits (Wien-Bridge oscillator, RC phase-shift oscillator and crystal oscillator).
(4 lectures)

## Refer Chapters 6 and 7

8. Electronic Instruments: The basic principle of oscilloscopes, function of the sweep generator, block diagrams of an oscilloscope, simple CRO, measurement of frequency and phase by the Lissajous method, application of the oscilloscope for measurement of voltage, period and frequency, block diagram of standard signal generator, AF sine and square wave generator, function generator.

## Refer Chapter 8

## MODULE III (10 hours)

9. Digital Electronics Principles: Introduction, binary digits, logic levels and digital waveforms, introduction to the basic logic operation, the number system, decimal numbers, binary numbers, decimal-to-binary conversion, simple binary arithmetic.
(2 lectures)
10. Logic Gates and Boolean Algebra: The inverter, AND, OR, NAND, NOR, exclusive-OR and exclusive-NOR gates, Boolean operations and expressions, laws and rules of Boolean algebra, De Morgan's theorem, Boolean analysis of logic circuits, standard forms of Boolean expressions, Boolean expressions and the truth table.
11. Combinational Logic and Their Functions: Basic combinational logic circuits, implementation of combinational logic, universal properties of the NAND and NOR gates, basic adders, multiplexers and demultiplexers, elementary treatment of latches, basic concepts of memory (RAMs).
(4 lectures)

## Refer Chapter 9

Students will attend three hours of lecture each week. This course carries a credit of three points.

## ABOUT THE AUTHOR



Debashis De studied radio physics and electronics and obtained his Ph.D. from Jadavpur University in 2005. He is currently Associate Professor at the Department of Computer Science and Engineering, West Bengal University of Technology, Kolkata. With research interests in the field of semiconductor nanostructures, Dr De has more than 30 publications in international journals and conferences to his credit. In 2005, the International Union of Radio Science awarded him the International Young Scientists Award. In 2008, he was invited as a Post Doctoral Endeavour Research Fellow to the University of Western Australia, Perth, and the Australian Government awarded him the Endeavour Award for research and professional development. He is currently an adjunct research fellow at the University of Western Australia. Dr De has co-authored Einstein Relation in Compound Semiconductors and Their Nanostructures with Professor K. P. Ghatak. His current research topics include theoretical and simulative investigation of different electronic and transport properties of armchair and zigzag nanotubes, nanoscale transistors, quantum wells, wires, dots, superlattices, $n-i-p-i$ structures, and heavily doped systems under external controlled fields.

This page is intentionally left blank.

## 1

## Operational Amplifier

## Outline

1-1 Introduction to Electronics
1-2 The Operational Amplifier
1-3 Properties of the Ideal Operational
Amplifier
1-4 Specifications of IC 741C

## 1-5 Operational Amplifier and Its Terminal Properties

1-6 Applications of the Operational Amplifier
1-7 Real-Life Applications

## Objectives

In this chapter we examine the operational amplifier, which is the basic component of analog computers. The most commonly used op-amp IC is the 8 pin IC 741C. The internal structure of the op-amp, and the basic fabrication steps of integrated circuits are discussed in detail. All the basic terminal properties of the op-amp are also explained in this chapter and some practical applications of the op-amp are illustrated with real-life examples.

## 1-1 INTRODUCTION TO ELECTRONICS

The journey of electronics began in 1887 with the discovery of the elementary particle electron by the Nobel laureate British scientist Sir J. J. Thompson. Since the invention of the first amplifying device-the triode vacuum tube-in 1904 by John A. Fleming, electronics has evolved by leaps and bounds. The silicon diode was patented by Greenleaf Whittier Pickard in 1906, and this was followed by the invention of the first radio circuits using diodes and triodes between 1907 and 1927, the super heterodyne receiver by Major Edwin Howard Armstrong in 1920, the television in 1925, the field-effect devices in 1925, the concept of modulation by Armstrong in 1933 and the radar in 1940. The discovery of silicon transistor by John Bardeen, Walter Brattain and William Shockley in 1947 (the trio received Nobel Prize in 1956 for this wonderful discovery) marked the beginning of the era of solid-state electronics.

The next breakthrough came in 1956 with the development of the thyristor-the key device of power electronics. The first integrated circuit was developed in 1958 by Jack Kilby at Texas Instruments, and Robert Noyce and Gordon Moore at Fairchild Semiconductor, announcing the beginning of computer-based electronics. Jack Kilby received the Nobel Prize in Physics in the year 2000. This discovery was followed by the 4004 microprocessor in 1971, the 8-bit microprocessor in 1972, and


Figure 1-1 Major milestones in the path of electronic revolution
the gigabit memory chip in 1995, all by Intel. The ultra-large-scale integrated circuits, having more than $10^{9}$ components per chip, were developed in the mid-1990s.

All the aforementioned devices are made up of solid-state materials in general. The sound understanding of the functioning of these devices requires a detailed investigation into the electronic processes, which are different for different materials. Among the multidimensional aims of modern electronics, we need the choice of appropriate materials for different applications that can be monitored just by controlling the electrical behaviour. A majority of solid-state devices in the industry today are made of semiconductors. The recent developments in VLSI technology make electronic goods compact, cheaper and versatile so that it becomes popular in the global industrial market. Figure 1-1 provides a chronological view of the journey from resistors to nano-devices. It may be noted that 67 major devices and 110 related devices have been discovered within a period of less than 200 years. Let us take a look at some of the terms and concepts in electronics.

Signal: A signal contains a set of information. TV signals, radio signal or mobile signals are real life examples. Signal processing is performed by transducers. A transducer converts non-electrical signals to electrical ones. The telephone transducer converts an audio signal to an electrical signal at the transmission end, while electrical signal is converted to audio signal at the receiver end. The


Figure 1-2 A CRO waveform showing voltage ( $y$ axis) with respect to time ( $x$ axis)
modulation and demodulation processes are used for proper signal transmission in a telecommunication network. In electrical and electronic circuits, DC and AC signals are used. A voltage signal plays a major role in electrical and electronic circuit parameters and performance.

Noise: Noise is an unwanted signal. Noise is the enemy of any communication system.
Frequency spectrum of signals: The time domain signal can be represented graphically using a Cathode-Ray Oscilloscope. Signal voltage $(V)$ is plotted along the $y$ axis and time $(t)$ along the $x$ axis using the CRO as shown in Figure 1-2. The frequency domain of a signal can be represented using a spectrum analyzer. Signal power versus frequency is plotted using a spectrum analyzer as shown in Figure 1-3.

Analog and digital signals: There are two types of signals-analog and digital. The waveform of an analog signal is shown in Figure 1-4(a) and that of a digital signal in Figure 1-4(b). Digital signals


Figure 1-3 Spectrum of a satellite signal plotted using a spectrum analyzer where signal power is marked on the $y$ axis and frequency on the $x$ axis


Figure 1-4(a) An analog signal waveform


Figure 1-4(b) A digital signal waveform showing the 10101 ... pattern
are expressed as $10101 \ldots$ patterns. Generally, signals are analog in nature, and they are converted to the digital form using an analog to digital converter (ADC).

Today, digital signals are widely prevalent in every application. Most communication signals earlier were analog. But they have now been replaced with digital signals. For example, almost all satellite televisions use digital signals to transmit data. Digital signals help in eliminating noisesomething that is rather difficult to do when using analog signals. For long distance communication systems, repeater stations are used. Repeater stations perform regeneration, reshaping and retiming using a digital signal. This repeater operation is possible only because of the digital pattern. Digital signal processing is used for better signal transmission. Direct-to-home or DTH TV provides studioquality signals from the comfort of the home.

Amplifiers: The electronic circuit that increases the magnitude of the signal several times based on circuit parameters and system requirements is called an amplifier. For example, voltage amplifiers and current amplifiers increase the magnitude of voltage and current several times. When the magnitude of signal is very low, transducers cannot handle the signal. In such a case amplification of the signal becomes essential. By using amplifiers, the desired level of the signal can be reached. Microvolt $(\mu \mathrm{V})$ signals can be converted to milivolt $(\mathrm{mV})$ signals by amplifying the input voltage a thousand times using a suitable circuit. After increasing the voltage, the signal becomes suitable for the transducer. If $V_{i}$ is the input voltage and $A$ is the gain of amplifier, then the expression of output voltage $\left(V_{0}\right)$ is expressed as:

$$
V_{0}=A V_{i}
$$

The amplification factor $(A)$ or gain is the ratio of output to input parameter. For a voltage amplifier, it is the ratio of the output voltage to the input voltage.

$$
A=\frac{V_{0}}{V_{i}}
$$

Linearity is an important property of an amplifier. Output voltage or current should increase linearly based on the amplification factor. Ideally, the amplifier should be linear and distortion-free. The
output signal waveform should be identical to the input signal. Any deviation or change is called distortion-where the non-linearity of the circuit elements deviates from linearity. Power amplifiers can be designed using the op-amp voltage. Power amplifiers are used in music systems and televisions, among others.

Digital logic inverters: The digital logic inverter is the basic element for circuit design. As the name indicates, this logic performs the inverse operation-that is, input zero is converted to output one, and input one is converted to output zero. An inverter can be designed using a transistor or CMOS. An inverter or NOT gate is a logic gate which implements logical negation. The truth table of a digital logic inverter is shown in Table 1-1.

| Input | Output |
| :---: | :---: |
| 0 | 1 |
| 1 | 0 |

$\begin{array}{ll}\text { Table 1-1 } & \begin{array}{l}\text { Truth table of a digital } \\ \text { logic inverter }\end{array}\end{array}$

## 1-2 THE OPERATIONAL AMPLIFIER

The operational amplifier (popularly known as op-amp) is an active device used to design circuits that perform useful operations, such as generating sine waves or square waves; amplifying, combining, integrating, differentiating and removing noise; and transforming alternating current into direct current and vice-versa. It can also change the shape of a waveform, produce a change in the output when an input signal reaches a certain level, provide constant voltage or current, and perform various other important circuit operations. Op-amp circuits are very important as we develop a valuable perception about how electronic circuits work in general.

An op-amp is a very high-gain differential amplifier with high input impedance and low output impedance. Figure $1-5$ shows a basic op-amp with two inputs and one output. The negative terminal is known as the inverting input terminal (Input 1), and the positive terminal is known as the non-inverting input terminal (Input 2). Each input results in an


Figure 1-5 Basic op-amp output, which further depends upon the input that is being applied to positive $(+)$ or negative $(-)$ input terminals. The op-amp is known as the differential amplifier because it amplifies the voltage difference of the inverting and non-inverting terminals.

## 1-3 PROPERTIES OF THE IDEAL OPERATIONAL AMPLIFIER

An ideal op-amp should have the following properties:

1. Gain must be infinite
2. Output voltage must be zero when input voltages are same or when both are zero
3. The input resistance must be infinite
4. The output resistance must be zero
5. The common mode rejection ratio (CMMR) must be infinite

Table 1-2 Comparison between the parameters of an ideal op-amp and a practical op-amp

| Op-amp <br> Parameters | Ideal Op-amp <br> Parameters | Practical Op-amp <br> Parameters |
| :--- | :--- | :--- |
| Gain | Infinite | $10^{3}$ to $10^{6}$ order |
| Output voltage | Zero (0 volt) | Few volts (in $\mu \mathrm{V}$ or nV ), due <br> to offset |
| Input resistance | Infinite $(\alpha)$ | $10^{3} \Omega$ to $10^{6} \Omega$ order |
| Output resistance | Zero $(0 \Omega)$ | Few ohm $(\Omega)$ order |
| CMRR | Infinite $(\alpha)$ | 100 dB order |
| Bandwidth | Infinite $(\alpha)$ | Mega Hz order |
| Slew rate | Infinite $(\alpha)$ | $0.5 \mathrm{~V} / \mu \mathrm{s}$ order |

6. Infinite bandwidth, i.e., it must allow all frequencies to pass
7. Op-amp characteristics should not drift with temperature

All these parameters for an ideal op-amp are different from those of a practical op-amp, as illustrated by the comparison given in Table 1-2.

## 1-4 SPECIFICATIONS OF IC 741C

The op-amp popularly used in the laboratory is IC 741C. It is an eight (8) pin DIP (dual input package) IC, as shown in the Figure 1-6.

## 1-4-1 Description of Op-Amp 741 IC Pins

## Pins 1 and 5: These two pins are used for offset null process.

Pin 2: Inverting input terminal, i.e., when a sinusoidal signal is applied to the input pin 2, inverted output is obtained at the output terminal 6.


Figure 1-6 Block diagram of 8 pin IC 741C

Pin 3: Non-inverting input terminal, i.e., when a sinusoidal signal is applied to the input pin 3, waveform of same phase output is obtained.
Pin 4: $\quad-V_{c c}$, i.e., negative terminal of supply voltage is connected to this pin.
Pin 6: Output terminal.
Pin 7: $\quad+V_{c c}$ i.e., positive terminal of supply voltage is connected to this pin.
Pin 8: No electrical connection is there in this pin; this pin is just for balance and the symmetric dual-input package look.

## 1-5 OPERATIONAL AMPLIFIER AND ITS TERMINAL PROPERTIES

An ideal operational amplifier is perfectly balanced with the output voltage $V_{o}=0$ for $V_{1}=V_{2}$ i.e., the op-amp output is zero when the same or zero (ground) voltage is applied to both the inverting and non-inverting terminals, as shown in Figure 1-7(a). A complete representation of the op-amp is


Figure 1-7(a) Op-amp input and output terminals shown in Figure 1-7(b).

A practical op-amp exhibits an unbalance caused by a mismatch of the input transistors $\left(Q_{1}\right.$ and $Q_{2}$ ). This mismatch results in the flow of unequal bias currents through the input terminals. This in turn, causes a change in the various parameters of an op-amp. The circuit diagram of a differential amplifier is shown in Figure 1-8.


Figure 1-7(b) Complete representation of op-amps


Figure 1-8 Circuit diagram of a differential amplifier


Figure 1-9 Input offset voltage in an op-amp


Figure 1-10 Output offset voltage in an op-amp

## 1-5-1 Input Offset Voltage and Output Offset Voltage

The input offset voltage, $V_{i o}$, is the differential input voltage that exists between two input terminals of an op-amp without any external inputs applied. In other words, it is the amount of input voltage that should be applied between the two input terminals in order to force the output voltage to zero, as shown in Figure 1-9.

The output offset voltage, $V_{o o}$, is a dc voltage; it may be positive or negative in polarity depending upon whether the potential difference between two input terminals is positive or negative. It is impossible to predict the polarity of the output offset voltage as it is dependent on the mismatching between the two input terminals.

To reduce $V_{o o}$ to zero we need to have a circuit at the input terminals of the op-amp that will give us the flexibility of obtaining $V_{i o}$ with proper amplitude and polarity. Such a circuit is called input offset voltage- compensating network, as shown in Figure 1-9. Before we apply external input to the op-amp, with the help of an offset voltage-compensating network, we reduce the output offset voltage $V_{o o}$ to zero; the op-amp is said to be nulled or balanced. The total output offset voltage can be expressed as:

Output offset voltage $V_{o o}=$ offset due to input voltage $V_{i o}+$ offset due to input offset current.
The output offset voltage diagram is given in Figure 1-10.

## 1-5-2 Input-Bias Current

The input-bias current $I_{B}$ is defined as the average of the two input-bias currents, $I_{B 1}$ and $I_{B 2}$ as shown in Figure 1-11, and is given by:

$$
\begin{equation*}
I_{B}=\frac{I_{B 1}+I_{B 2}}{2} \tag{1-1}
\end{equation*}
$$

where, $I_{B 1}$ is the dc bias current flowing into the non-inverting input, and $I_{B 2}$ is the dc bias current flowing into the inverting input.

In the Figure 1-11, both the input terminals are grounded so that no input voltage is applied to the op-amp. However, the plus-minus sign supply voltages are necessary to bias the op-amp properly.

The input-bias currents $I_{B 1}$ and $I_{B 2}$ are the base bias currents of the two transistors in the input differential amplifier stage of the op-amp. Even though both of the input transistors are identical, it is not possible to have $I_{B 1}$ and $I_{B 2}$ exactly equal to each other because of the external imbalance between the two inputs.
Figure 1-11 Input-bias current in an op-amp

Although very small, the input-bias current $I_{B}$ can cause a significant output offset voltage in circuits using relatively large feedback resistors. This output offset voltage may not be as large as that caused by the input offset voltage, but certain precautions must be taken to minimize it.

Here we obtain the expression for the output offset voltage caused by the inputbias current $I_{B}$ in the inverting and noninverting amplifiers, and then devise some scheme to eliminate or minimize it. The non-inverting or inverting amplifier with $V_{\text {in }}$ $=0$ is shown in Figure 1-12. Let us assume that the input offset voltage $V_{i o}$ is zero, and


Figure 1-12 Output offset voltage due to input-bias current in an inverting or non-inverting amplifier there is no offset voltage due to $V_{i o}$. Let $V_{o I_{B}}$ be the output voltage due to the input-bias current $I_{B}$.

In Figure 1-12 the input-bias currents $I_{B 1}$ and $I_{B 2}$ are flowing into the non-inverting and inverting input leads, respectively. The non-inverting terminal is connected to the ground; therefore, the voltage $V_{1}=0 \mathrm{~V}$. The controlled voltage source $A V_{i o}=0$, since $V_{i o}=0$ is assumed. With output resistance $R_{0}$ negligibly small, the right end of $R_{F}$ is essentially at ground potential; that is resistors $R_{1}$ and $R_{F}$ are in parallel, and the bias current $I_{B 2}$ flows through them. Therefore, the voltage at the inverting terminal is:

$$
\begin{align*}
& V_{2}=\left(R_{1} \| R_{F}\right) I_{B 2}  \tag{1-2}\\
& V_{2}=\frac{R_{1} R_{F}}{R_{1}+R_{F}} I_{B 2} \tag{1-3}
\end{align*}
$$

Writing the node voltage equation for node $V_{2}$, we get:

$$
\begin{array}{r}
I_{1}+I_{2}=I_{B 2} \\
\frac{0-V_{2}}{R_{1}}+\frac{V_{o I_{B}}-V_{2}}{R_{F}}=\frac{V_{2}}{R_{i}} \tag{1-4}
\end{array}
$$

where, $V_{o_{B}}$ is the output offset voltage due to input-bias current, and $R_{i}$ is the input resistance of the op-amp.
Re-arranging Equation (1-4), we get:

$$
\frac{V_{o I_{B}}}{R_{F}}=V_{2}\left(\frac{1}{R_{1}}+\frac{1}{R_{F}}+\frac{1}{R_{i}}\right)
$$

Since $R_{i}$ is extremely high (ideally $\left.\infty\right) \frac{1}{R_{i}} \cong 0$. Therefore:

$$
\begin{equation*}
\frac{V_{o I_{B}}}{R_{F}}=V_{2}\left(\frac{R_{1}+R_{F}}{R_{1} R_{F}}\right) \tag{1-5}
\end{equation*}
$$

Substituting the value of $V_{2}$ from Equation (1-3) in Equation (1-5), we get:

$$
\begin{align*}
& V_{o I_{B}}=\frac{R_{1} R_{F} I_{B 2}}{R_{1}+R_{F}}\left(\frac{R_{1}+R_{F}}{R_{1}}\right) \\
& V_{o I_{B}}=R_{F} I_{B 2} \tag{1-6}
\end{align*}
$$

Since, $I_{B 1}=I_{B 2}=I_{B}$, we can write Equation (1-6) as:

$$
\begin{equation*}
V_{o I_{B}}=R_{F} I_{B} \tag{1-7}
\end{equation*}
$$

According to Equation (1-7), the amount of output offset voltage $V_{o_{B}}$ is a function of feedback resistor $R_{F}$ for a specified value of input-bias current $I_{B}$. The amount of $V_{o I_{B}}$ is increased by the use of relatively large feedback resistors. Therefore, the use of small feedback resistors is recommended.

To eliminate or to reduce the output offset voltage $V_{o I_{B}}$ due to input-bias current $I_{B}$, we have to introduce some scheme at the input by which voltage $V_{1}$ can be made equal to voltage $V_{2}$. In other words, if voltages $V_{1}$ and $V_{2}$-caused by the currents $I_{B 1}$ and $I_{B 2}$ - can be made equal, there will be no output voltage $V_{o I_{B}}$.

From Equation (1-3) we have:
where,

$$
\begin{align*}
V_{2} & =R_{P} I_{B 2}  \tag{1-8}\\
R_{P} & =\frac{R_{1} R_{F}}{R_{1}+R_{F}}
\end{align*}
$$

Equation (1-8) implies that we must express voltage $V_{1}$ at the non-inverting input terminal as a function of $I_{B 1}$ and some specific resistor $R_{O M}$. This can be accomplished as follows. The input-bias current $I_{B 1}$ does not produce any voltage at the non-inverting input terminal, because this terminal is directly connected to the ground. If we could connect the proper value of resistor $R_{O M}$ to the noninverting terminal, the voltage $V_{1}$ would be:

$$
\begin{equation*}
V_{1}=R_{O M} I_{B 1} \tag{1-9}
\end{equation*}
$$

To have voltage $V_{1}$ equal to $V_{2}$, the right hand side of Equations (1-8) and (1-9) must be equal, therefore:
or,

$$
\begin{align*}
R_{P} I_{B 2} & =R_{O M} I_{B 1}  \tag{1-10}\\
\frac{R_{1} R_{F}}{R_{1}+R_{F}} & =R_{O M} \tag{1-11}
\end{align*}
$$

Thus, the proper value required of a $R_{O M}$ resistor connected to the non-inverting terminal is the parallel combination of resistors $R_{1}$ and $R_{F}$. However, the use of $R_{O M}$ may eliminate the output offset voltage $V_{o I_{B}}$ because the currents $I_{B 1}$ and $I_{B 2}$ are not exactly equal. Nevertheless, the use of $R_{O M}$ will minimize the amount of output offset voltage $V_{o I_{B}}$; therefore, the $R_{O M}$ resistor is referred to as the offset minimizing resistor.

## 1-5-3 Input Offset Current and Output Offset Current

We have seen that the use of $R_{O M}$ in series with the non-inverting terminal reduces the output offset voltage $V_{o I_{B}}$ caused by $I_{B}$. However, the value of $R_{O M}$ was derived on the assumption that the input-
bias currents $I_{B 1}$ and $I_{B 2}$ are equal. In practice, these currents are not equal because of the internal imbalances in the op-amp circuitry. The algebraic difference between the individual currents entering into the inverting and non-inverting terminals of a balanced amplifier is referred to as input offset current $I_{i o}$. The input offset current $I_{i o}$ is used as an indicator of the degree of mismatch between these two currents. Therefore, the value of $I_{i o}$ is the difference between two input-bias currents. The input offset current for the 741 C is 200 nA maximum. From Figure 1-13, we can write the expression for input offset current as:

$$
\begin{equation*}
I_{i o}=\left|I_{B 1}-I_{B 2}\right| \tag{1-12}
\end{equation*}
$$

In the circuit shown in Figure 1-14, there will be an output offset voltage due to the input-bias currents $I_{B 1}$ and $I_{B 2}$. In other words, the output offset voltage can be expressed as a function of input offset current $I_{i o}$. Let $V_{o I_{i o}}$ be the output offset voltage caused by the input offset current $I_{i o}$. To separate the effect of the input offset current from that of the input offset voltage, assume that $V_{i o}=0 \mathrm{~V}$.

Referring to Figure 1-14, and expressing the voltages $V_{1}$ and $V_{2}$ in terms of a function of $I_{B 1}$ and $I_{B 2}$ for a given value of $R_{1}$ and $R_{F}$, we get:
where,
Applying the superposition theorem, we can now find the output offset voltage due to $V_{1}$ and $V_{2}$ in terms of $I_{B 1}, I_{B 2}$ and $R_{F}$. From Equation (1-6) we have:

$$
V_{o I_{B 2}}=-R_{F} I_{B 2}
$$

Here the negative sign is used because voltage $V_{2}$ is the voltage at the inverting input terminal. This output offset voltage $V_{o I_{B 2}}$ is due to voltage $V_{2}$, only in terms of $I_{B 2}$, and $R_{F}$. Similarly, the output offset voltage $V_{o_{B 1}}$ due to $V_{1}$, only in terms of $I_{B 1}$ and $R_{F}$, can be obtained as follows:

$$
\begin{equation*}
V_{o I_{B 1}}=V_{1}\left(1+\frac{R_{F}}{R_{1}}\right) \tag{1-15}
\end{equation*}
$$

where, $V_{1}$ is the voltage at the non-inverting terminal, and $\left(1+\frac{R_{F}}{R_{1}}\right)$ is the gain of the non-inverting
amplifier.
Substituting the value of $V_{1}$ from Equation (1-13) in Equation (1-15), we get:

$$
\begin{align*}
V_{o I_{B 1}} & =R_{O M} I_{B 1}\left(1+\frac{R_{F}}{R_{1}}\right) \\
& =\frac{R_{1} R_{F}}{R_{1}+R_{F}} I_{B 1} \frac{R_{1}+R_{F}}{R_{1}} \\
V_{o I_{B 1}} & =R_{F} I_{B 1} \tag{1-16}
\end{align*}
$$

Therefore, the maximum magnitude of the output offset voltage due to $I_{B 1}$ and $I_{B 2}$ is:

$$
\begin{align*}
V_{o I_{B 1}}+V_{o I_{B 2}} & =R_{F} I_{B 1}-R_{F} I_{B 2} \\
& =R_{F}\left(I_{B 1}-I_{B 2}\right) \\
V_{o I_{i o}} & =R_{F} I_{i o} \tag{1-17}
\end{align*}
$$

where, $V_{o I_{B 1}}+V_{o I_{B 2}}=V_{o I_{i 8}}$ is the output offset voltage due to $I_{i o}=\left|I_{B 1}-I_{B 2}\right|$, the input offset current. Thus, for a given value of the input offset current $I_{i o}$, the amount of output offset voltage $V_{o I_{i o}}$ depends on the value of feedback resistor $R_{F}$.

The output offset voltage $V_{o o}$ caused by $V_{i o}$ could be either positive or negative with respect to the ground. Similarly, the output offset voltage $V_{o I_{B}}$ caused by $I_{B}$ could also be positive or negative with respect to the ground. If these output offset voltages are of different polarities, the resultant output offset will be very little. On the other hand, if both of these output offset voltages were of the same polarity, the maximum amplitude of the total output offset would be:

$$
\begin{align*}
V_{o o T} & =V_{o o}+V_{o I_{B}} \\
& =\left(1+\frac{R_{F}}{R_{1}}\right) V_{i o}+R_{F} I_{B} \tag{1-18}
\end{align*}
$$



Figure 1-15 Input offset voltage $V_{i o}$

## 1-5-4 Input Offset Null Voltage

Input offset null voltage is the voltage that must be applied between the two input terminals of an op-amp to null the output or to balance the amplifier. In Figure 1-15, $V_{d c 1}$ and $V_{d c 2}$ are dc voltages, and $R_{s}$ represents the source resistance. Input offset voltage is represented by $V_{i o}$. This voltage $V_{i o}$ could be positive or negative (its absolute value is listed in the datasheet). For

IC 741 C , the maximum value of $V_{i o}$ is 6 mV . The smaller the value of $V_{i o}$, the better the input terminals are matched.

## 1-5-5 Differential Input Resistance

Differential input resistance or input resistance $R_{i}$ is the equivalent resistance that can be measured either at the inverting or at the non-inverting input terminal with the other terminal connected to the ground. For 741 C , the input resistance is a relatively high, $2 \mathrm{M} \Omega$.

## 1-5-6 Input Capacitance

Input capacitance $C_{i}$ is the equivalent capacitance that can be measured either at the inverting or at the non-inverting terminal with other terminal connected to the ground. A typical value of $C_{i}$ is 1.4 pF for 741C.

## 1-5-7 Offset Voltage Adjustment Range

One of the features of the 741 family of op-amp is an offset voltage null capability. The $741 \mathrm{op}-$ amp has pins 1 and 5 marked as offset null for this purpose. A potentiometer can connect offset null pins 1 and 5 , and the wiper of the potentiometer can be connected to the negative supply $-V_{E E}$. By varying the potentiometer, the output offset voltage can be reduced to zero. Thus, offset voltage adjustment range is the range through which the input offset voltage can be adjusted by varying the potentiometer. For 741 C , the offset voltage adjustment range is $\pm 15 \mathrm{mV}$.

## 1-5-8 Input Voltage Range

When the same voltage is applied to both input terminals, the voltage is called a common-mode voltage $V_{c m}$ and the op-amp is said to be operating in common-mode configuration. For the 741 C , the range of the input common-mode voltage is $\pm 13 \mathrm{~V}$ at the maximum. This means that the common-mode voltage applied to both input terminals can be as high as +13 V and as low as -13 V , without disturbing the proper functioning of the op-amp. In other words, the input voltage range is the range of the common-mode voltage over which the offset specifications apply. The common-mode configuration is used only for test purposes to determine the degree of matching between the inverting and non-inverting input terminals.

## 1-5-9 Common-Mode Rejection Ratio (CMRR)

If $V_{1}$ and $V_{2}$ are the signal voltages applied to the non-inverting and inverting terminals of an op-amp respectively, and $V_{o}$ is the voltage appearing at the output terminal, then we can define the two terms related to the voltage.

1. Difference signal voltage:

$$
V_{d}=V_{1}-V_{2}
$$

2. Common-mode signal voltage:

$$
\begin{equation*}
V_{c}=\frac{V_{1}+V_{2}}{2} \tag{1-19}
\end{equation*}
$$

The unwanted common-mode signal $V_{c}$ is the cause of distortion in the output voltage. The differential amplifier has the property of rejecting the noise. The output voltage $V_{o}$ at the output terminal of the differential op-amp will be:

$$
\begin{equation*}
V_{o}=A_{1} V_{1}+A_{2} V_{2} \tag{1-20}
\end{equation*}
$$

where, $A_{1}$ is the voltage gain when the inverting terminal is grounded, and $A_{2}$ is the voltage gain when the non-inverting terminal is grounded.

From Equations (1-20) and (1-21) we get:

$$
\begin{align*}
& V_{1}=V_{c}+\frac{V_{d}}{2}  \tag{1-21}\\
& V_{2}=V_{c}-V_{d} \tag{1-22}
\end{align*}
$$

Using Equations (1-22) and (1-23) in Equation (1-21) we can write:

$$
\begin{gathered}
V_{o}=\frac{\left(A_{1}-A_{2}\right)}{2} V_{d}+\left(A_{1}+A_{2}\right) V_{c} \\
V_{o}=A_{d} V_{d}+A_{c} V_{c}
\end{gathered}
$$

where, $A_{d}=\left(A_{1}-A_{2}\right) / 2$ is the difference signal voltage gain, and $A_{C}=A_{1}+A_{2}$ is the common-mode voltage gain.

Considering the ideal case we find at $A_{c}=0$ that $A_{1}=-A_{2}$. Therefore:

$$
A_{d}=\frac{\left[A_{1}-\left(-A_{1}\right)\right]}{2}=A_{1}
$$

The value of $A_{d}$ can be infinitely large. In practice it is not true. So, the CMRR is defined as the ratio of the differential voltage gain $A_{d}$ to the common-mode voltage gain $A_{c m}$. Therefore:

$$
\begin{equation*}
\mathrm{CMRR}=\frac{\text { Differential voltage gain }}{\text { Common-mode voltage gain }}=\frac{A_{d}}{A_{c m}} \tag{1-23a}
\end{equation*}
$$

The value of CMRR can be expressed in logarithmic form as:

$$
\begin{equation*}
\mathrm{CMRR}=20 \log _{10}\left|\frac{A_{d}}{A_{c m}}\right| \tag{1-23b}
\end{equation*}
$$

The differential voltage gain $A_{d}$ is the same as the large signal voltage gain $A$, however, the commonmode voltage gain is given by:

$$
\begin{equation*}
A_{c m}=\frac{V_{o c m}}{V_{c m}} \tag{1-24}
\end{equation*}
$$

where, $V_{o c m}$ is the output common-mode voltage, and $V_{c m}$ is the input common-mode voltage.
Generally, $A_{c m}$ is very small and $A_{d}=A$ is very large; therefore, CMRR is very large. Being very large, CMRR is expressed in decibels (dB). For the 741 C , CMRR is 90 dB . The higher the value of CMRR, the better is the matching between the two input terminals and the smaller is the output common-mode voltage.

## 1-5-10 Supply Voltage Rejection Ratio (SVRR)

The change in an op-amp's input offset voltage $V_{i o}$ caused by a variation in one supply voltage when the other supply voltages remain constant in the circuit is called the supply voltage rejection ratio (SVRR). It is also referred to as power supply rejection ratio (PSRR) or power supply sensitivity (PSS). These are expressed in terms of microvolts per volt or in decibels. If we denote the change in supply voltages by $\Delta V$, and the corresponding change in the input offset voltage by $\Delta V_{i o}$, then SVRR can be defined as:

$$
\begin{equation*}
\mathrm{SVRR}=\frac{\Delta V_{i o}}{\Delta V} \tag{1-25}
\end{equation*}
$$

For the $741 \mathrm{C}, \mathrm{SVRR}=150 \mu \mathrm{~V} / \mathrm{V}$. On the other hand, for the 741 C :

$$
\begin{equation*}
\mathrm{SVRR}=20 \log _{10}\left(\frac{\Delta V}{\Delta V_{\text {io }}}\right)=104 \mathrm{~dB} \tag{1-26}
\end{equation*}
$$

This means, that the lower the value of SVRR in microvolts/volt, the better it is for the op-amp performance.

## 1-5-11 Large Signal Voltage Gain

Since the op-amp amplifies the difference voltage between the two input terminals, the voltage gain of amplifier is defined as:

$$
\begin{align*}
\text { Voltage gain } & =\frac{\text { Output voltage }}{\text { Differential input voltage }} \\
A & =\frac{V_{o}}{V_{i d}} \tag{1-27}
\end{align*}
$$

Under the test conditions $R_{L} \geqslant 2 \mathrm{k} \Omega$ and $V_{o}= \pm 10 \mathrm{~V}$; the large signal voltage gain of 741 C is 200,000 typically.

## 1-5-12 Output Voltage Swing

The output voltage swing $V_{o_{\max }}$ of the 741 C is guaranteed between -12 V and +12 V for $R_{L} \geqslant 2 \mathrm{k} \Omega$, i.e., giving a 26 V peak-to-peak undistorted sine wave for ac input signals. In fact, the output voltage swing indicates the values of positive and negative saturation voltages of the op-amp. The output voltage never exceeds these limits for the given supply voltages, $+V_{c c}$ and $-V_{c c}$.


Figure 1-16 Transfer characteristics of an op-amp

## 1-5-13 Output Resistance

The output resistance $R_{o}$ is the equivalent resistance that can be measured between the output terminal of the op-amp and the ground. For an ideal op-amp, the output resistance is zero. But it is typically $50 \Omega$ or less for the 741 C op-amp.

## 1-5-14 Supply Voltage

The op-amp has a dual dc input supply voltage. Supply voltage $V_{c c}$ used in op-amp is generally of a few volts. Typically it varies from -12 V to +12 V . In IC 741 C , pin 4 is connected with the negative supply voltage, say -12 V Volt $\left(-V_{c c}\right)$, and pin 7 is connected with the positive supply, say +12 $\mathrm{V}\left(+V_{c c}\right)$. Voltage transfer characteristics of an op-amp depends upon the input supply voltage. The transfer characteristics of an op-amp are shown in Figure 1-16.

## 1-5-15 Supply Current

Supply current $I_{s}$ is the current drawn by the op-amp from the power supply. For the 741C the supply current is typically $I_{s}=2.8 \mathrm{~mA}$.

## 1-5-16 Power Consumption

Power consumption $\left(P_{c}\right)$ is the amount of quiescent power $\left(v_{i n}=0 \mathrm{~V}\right)$ that must be consumed by the op-amp in order to operate properly. The amount of power consumed by the 741 C is 85 mW .

## 1-5-17 Slew Rate

Slew rate (SR) is defined as the maximum rate of change in output voltage per unit of time, and is expressed in volts per $\mu$-seconds. The slew rate can be expressed as:

$$
\begin{equation*}
\mathrm{SR}=\left.\frac{d V_{\mathrm{o}}}{d t}\right|_{\text {maximum }} \mathrm{V} / \mu \mathrm{S} \tag{1-28}
\end{equation*}
$$

Slew rate indicates how rapidly the output of an op-amp changes in response to changes in the input frequency. The slew rate changes with change in voltage gain and is normally specified at unity $(+1)$ gain. The slew rate of an op-amp is fixed. Therefore, if the slope requirements of the output signal are greater than the slew rate, then distortion occurs. Thus, slew rate is one of the important factors in selecting the op-amp for ac applications; particularly at relatively high frequencies. One of the drawbacks of the 741C is its low slew rate $(0.5 \mathrm{~V} / \mu \mathrm{s})$, which limits its use in relatively high frequency applications, especially in comparators, oscillators, and filters.

For the purpose of calculating the slew rate equation, consider the voltage follower circuit, as shown in Figure 1-17. From this we can assume that the amplitude of the input voltage is large and of a high-frequency sine wave.

So, we can express the input voltage $V_{i n}$ as follows:

$$
\begin{equation*}
V_{i n}=V_{p} \sin \omega t \tag{1-29a}
\end{equation*}
$$



Figure 1-17 Schematic diagrams for slew rate

And the output voltage $V_{o}$ can be written as:

$$
\begin{equation*}
V_{o}=V_{p} \sin \omega t \tag{1-29b}
\end{equation*}
$$

Therefore, the rate of change of the output voltage is:

$$
\begin{equation*}
\frac{d V_{o}}{d t}=V_{p} \omega \cos \omega t \tag{1-29c}
\end{equation*}
$$

So, the maximum rate of change of the output occurs when:

$$
\begin{array}{lc} 
& \cos \omega t=1 \\
\therefore & \left.\frac{d V_{o}}{d t}\right|_{\max }=V_{p} \omega \\
\text { or, } & S R=2 \pi f V_{p} \text { volts } / \mathrm{sec} \\
\text { or, } & S R=\frac{2 \pi f V_{p}}{10^{6}} \text { volts } / \mu \mathrm{sec}
\end{array}
$$

where, $S R$ is the slew rate in volts/sec, $f$ is the input frequency, and $V_{p}$ is the peak value of the output sine wave in volts.

It can be concluded from Equation (1-29e), that the small value of input frequency $f$ determines the maximum undistorted output voltage swing.


Figure 1-18 Open-loop configuration using IC 741C and large signal pulse response curve

## Application of slew rate

Slew rate has an important application in both open-loop and closed-loop op-amp circuit. The open-loop configuration is shown in Figure 1-18. The output voltage rises from -14 V to +14 V because the open-loop voltage gain is very high. Calculating the slew rate of op-amp 741C we can calculate the time taken by the output to reach from -14 V to +14 V . The slew rate can be determined from the slope of the voltage follower from the large signal pulse response curve of Figure 1-18.

For a high-frequency operation the slew rate has to be increased. From Equation (1-29d) we can write:
$S R=2 \pi f_{\text {max }} V_{p}$
$f_{\max }=\frac{S R}{2 \pi V_{p}} \quad$ where, $V_{p}$ is fixed
$S R=\left.\frac{d V_{c}}{d t}\right|_{\max }=\frac{I_{\max }}{C}$
So, from Equation (1-29g) we can conclude that:

$$
\begin{aligned}
S R & =I_{\max } \\
& =g_{m} V_{t}
\end{aligned}
$$

Therefore, for better slew rate, the first stage differential amplifiers are composed of FETs, and are independent of $g_{m}$, unlike transistors. Hence, operational amplifiers are hybrid BiFETs. It is important to note that the slew rate is a small signal phenomenon. At the output there is no distortion, but only attenuation of magnitude.

## 1-5-18 Gain Bandwidth Product

The gain bandwidth product $(\mathrm{GB})$ is the bandwidth of the operational amplifier when the voltage gain is 1 . For the 741 C , it is found to be 1 MHz .

## 1-5-19 Virtual Ground

Virtual ground is defined as a node that has zero voltage, i.e., it is maintained at a steady reference potential, without being physically grounded. Sometimes the reference potential is considered to be the surface of the earth, from which "ground" is derived. Virtual ground is a concept that is used in
operational amplifiers and depends on very large voltage gain used to calculate the overall voltage gain of the amplifier.

## 1-6 APPLICATIONS OF THE OPERATIONAL AMPLIFIER

The op-amp is used either in inverting mode or non-inverting mode. In many practical applications the op-amp is used as adder, subtractor, intergrator, integrator, differentiator, voltage follower, phase changer, etc.

## 1-6-1 Inverting Mode of Operation

In the inverting mode of operation, the input supply $V_{i n}$ is connected to the inverting terminal, and the non-inverting terminal is directly connected to the ground, as shown in Figure 1-19. The resistor $R_{1}$ is connected to the inverting terminal of op-amp 741C pin 2, and feedback resistor $R_{F}$ is connected between inverting pin 2 and output pin 6, to the circuit.

Our aim here is to calculate the gain of the inverting amplifier. As the non-inverting terminal is directly connected to the ground, we get $V_{1}=0$, a consequence of virtual ground;


Figure 1-19 Operational amplifier in the inverting mode of operation $V_{2}=0$; and the terminal current $I_{2}=0$. Therefore, $V_{1}=V_{2}=0$.

Using KCL at node 2, we have:

$$
\begin{array}{ll}
I_{1}=I_{F}+I_{2} \\
\text { or, } & \frac{V_{i n}-V_{2}}{R_{1}}
\end{array}=\frac{V_{2}-V_{o}}{R_{F}}+0 \quad 1 \quad\left(\text { since } V_{2}=V_{1}=0\right)
$$

From Equation (1-30), it is clear that the negative sign indicates that the output voltage is in the opposite phase with that of the input. Therefore, this mode is said to be the inverting mode of operation.

Feedback gain of the inverting amplifier is represented as:

$$
\begin{equation*}
A_{F}=\frac{V_{o}}{V_{i n}}=-\frac{R_{F}}{R_{1}} \tag{1-31}
\end{equation*}
$$

## 1-6-2 Non-Inverting Mode of Operation



Figure 1-20 Op-amp in non-inverting configuration

In the non-inverting mode of operation the power supply $V_{i n}$ is connected to the non-inverting terminal of op-amp 741 C pin 3 and the inverting terminal is directly connected to the ground, as shown in Figure 1-20. The resistor $R_{1}$ is connected to the inverting terminal of opamp 741C pin 2, and feedback resistor $R_{F}$ is connected between inverting the pin 2 and the output pin 6 , to the circuit.

Our aim here is to calculate gain of the non-inverting amplifier shown in Figure 1-20. As the inverting terminal is directly connected to the ground and the terminal current $I_{2}=0$. Input voltage is applied to the non-inverting terminal of op-amp 741C pin 3.

$$
V_{1}=V_{2}=V_{i n}
$$

Using KCL at node 2 in Figure 1-20 we have:

$$
\begin{gathered}
I_{1}=I_{F}+I_{2} \\
\frac{V_{2}-V_{i n}}{R_{1}}=\frac{V_{i n}-V_{o}}{R_{F}}+0
\end{gathered}
$$

or,

$$
\frac{0-V_{i n}}{R_{1}}=\frac{V_{i n}-V_{o}}{R_{F}}+0
$$

or,

$$
-\frac{V_{i n}}{R_{1}}=\frac{V_{i n}-V_{o}}{R_{F}}
$$

or,

$$
\frac{V_{o}}{R_{F}}=\frac{V_{i n}}{R_{F}}+\frac{V_{i n}}{R_{1}}
$$

$$
\begin{equation*}
V_{o}=V_{i n}\left(1+\frac{R_{F}}{R_{1}}\right) \tag{1-32}
\end{equation*}
$$

Equation (1-32) shows that the output has the same phase as that of the input due to the same sign. Therefore, this mode of operation is said to be the non-inverting mode of operation. The feedback gain is given by:

$$
\begin{equation*}
A_{F}=\frac{V_{o}}{V_{i n}}=1+\frac{R_{F}}{R_{1}} \tag{1-33}
\end{equation*}
$$

Equation (1-33) indicates that the voltage gain is greater than or equal to unity. The feedback gain is unity if $R=0$ or $R=\alpha$. In this case, the non-inverting mode of the op-amp acts as a voltage follower.

## 1-6-3 Voltage Summing, Difference, and Constant Gain Multiplier

## Inverting configuration

Figure 1-21 shows the inverting configuration with three inputs $V_{a}, V_{b}$ and $V_{c}$. Depending on the relationship between $R_{a}, R_{b}$ and $R_{c}$, the circuit can be used as a summing amplifier/scaling amplifier or as an averaging amplifier.

Let $V_{o}$ be the output voltage. Using KCL at node $V_{2}$, we have:

$$
\begin{equation*}
I_{a}+I_{b}+I_{c}=I_{B}+I_{F} \tag{1-34}
\end{equation*}
$$

Since the op-amp is ideal, we have:

$$
\begin{align*}
& \frac{V_{a}-V_{2}}{R_{a}}+\frac{V_{b}-V_{2}}{R_{b}}+\frac{V_{c}-V_{2}}{R_{c}}=\frac{V_{2}-V_{o}}{R_{F}} \\
& I_{B}=0 \text { and } V_{1}=V_{2} \cong 0 \mathrm{~V} \\
& \therefore \quad V_{o}=-\left(\frac{R_{F}}{R_{a}} V_{a}+\frac{R_{F}}{R_{b}} V_{b}+\frac{R_{F}}{R_{c}} V_{c}\right) \\
& \text { or, } \quad \frac{V_{a}}{R_{a}}+\frac{V_{b}}{R_{b}}+\frac{V_{c}}{R_{c}}=-\frac{V_{o}}{R_{F}}
\end{align*}
$$

Now if $R_{a}=R_{b}=R_{c}=R_{F}=R$, we have from Equation (1-35)

$$
\begin{equation*}
V_{o}=-\left(V_{a}+V_{b}+V_{c}\right) \tag{1-36}
\end{equation*}
$$



Figure 1-21 Inverting configurations with three inputs


Figure 1-22 Output characteristics of an inverting amplifier

Hence, the amplifier shown in Figure 1-21 acts as the summing amplifier.
The output characteristic of an inverting amplifier, as shown in Figure 1-22 is that the output voltage is of opposite polarity to the input voltage. Hence, it is called the inverting amplifier.

## Non-inverting configuration

From Figure 1-23, using superposition theorem, the voltage $V_{1}$ at the non-inverting terminal is derived as:


Figure 1-23 Non-inverting configurations with three inputs


Figure 1-24 Output characteristics of a non-inverting amplifier
or,

$$
\begin{array}{r}
V_{1}=\frac{\frac{R_{a}}{2}}{R_{a}+\frac{R_{a}}{2}} V_{a}+\frac{\frac{R_{b}}{2}}{R_{b}+\frac{R_{b}}{2}} V_{b}+\frac{\frac{R_{c}}{2}}{R_{c}+\frac{R_{c}}{2}} V_{c} \\
V_{1}=\frac{V_{a}}{3}+\frac{V_{b}}{3}+\frac{V_{c}}{3}=\frac{V_{a}+V_{b}+V_{c}}{3} \tag{1-37}
\end{array}
$$

Hence, the output voltage $V_{o}$ is given by:

$$
\begin{align*}
V_{o}= & V_{1}\left(1+\frac{R_{F}}{R_{1}}\right) \\
& =\left(1+\frac{R_{F}}{R_{1}}\right) \frac{V_{a}+V_{b}+V_{c}}{3} \tag{1-38}
\end{align*}
$$

If, $1+\frac{R_{F}}{R_{1}}=3$, then the output voltage is given by:

$$
V_{o}=V_{a}+V_{b}+V_{c}
$$

Hence, the amplifier acts as a summing amplifier.
The output characteristics of a non-inverting amplifier as shown in the Figure 1-24 is that output voltage is of the same polarity as the input voltage. Hence, the name of the amplifier is non-inverting amplifier.


Figure 1-25 Basic differential amplifier used as subtractor

## Subtractor

A basic differential amplifier can be used as a subtractor as shown in Figure 1-25. The input signals can be scaled to the desired values by selecting appropriate values for the external resistors.

In Figure 1-25 all the resistors are of the equal value so that the gain of the amplifier is equal to 1 .

Using the superposition theorem, the output due to voltage $V_{a}$ is given by:

$$
\begin{aligned}
V_{o a} & =-\frac{R}{R} V_{a} \\
& =-V_{a}
\end{aligned}
$$

Here,

$$
V_{1}=V_{b} \frac{R}{R+R}=\frac{V_{b}}{2}
$$

The output voltage due to voltage $V_{b}$ is:

$$
\begin{aligned}
V_{o b} & =\left(1+\frac{R}{R}\right) V_{1} \\
& =2 V_{1}=V_{b}
\end{aligned}
$$

Therefore, output voltage $V_{o}$ is given by:

$$
\begin{align*}
V_{o} & =V_{o a}+V_{o b} \\
& =V_{b}-V_{a} \tag{1-39}
\end{align*}
$$

Thus, the output voltage $V_{o}$ is equal to the voltage $V_{b}$ applied to the non-inverting terminal minus the voltage $V_{a}$ applied to the inverting terminal. Hence, the circuit is called the subtractor.

## 1-6-4 Voltage Follower or Unity Gain Amplifier

The lowest gain that can be obtained from the non-inverting amplifier with feedback is 1 . When the non-inverting amplifier is configured for unity gain, it is called a voltage follower because the output voltage is equal to, and also in phase with the input. In other words, in the voltage follower the output follows the input voltage.

It is similar to the discrete emitter follower, but the voltage follower is preferred because it has much higher input resistance, and the output amplitude is exactly equal to the input. To obtain the voltage follower from the non-inverting amplifier $R_{1}$ is simply made open, and $R_{F}$ is shorted. Voltage follower is also called non-inverting buffer because, when placed between two networks, it removes the loading on the first network.

In the non-inverting mode of operation the power supply $V_{i n}$ is connected to the non-inverting terminal, and the inverting terminal is connected to the ground, as shown in Figure 1-26. The resistor $R_{1}$ and feedback resistor $R_{F}$ are replaced by a short circuit. We rewrite the Equation (1-32) as follows:


Figure 1-26 Voltage follower circuit

$$
V_{o}=V_{\text {in }}\left(1+\frac{R_{F}}{R_{1}}\right)
$$

In this case, voltage follower $R_{F}=0$, so the output voltage will become equal to input voltage; hence the name voltage follower becomes more appropriate. And the voltage gain becomes unity.

$$
A_{F}=\frac{V_{o}}{V_{i n}}=1+\frac{R_{F}}{R_{1}}=1+\frac{0}{R_{1}}=1
$$

## 1-6-5 Comparator

The comparator in the non-inverting mode is shown in Figure 1-27.
A fixed reference voltage $\left(V_{\text {ref }}\right)$ is applied to the $(-)$ ve input, and the other time-varying signal voltage $v_{i n}$ is applied to the $(+)$ ve input. When $v_{i n}$ is less than $V_{\text {ref }}$, the output voltage $v_{o}$ is at $-V_{\text {sat }}\left(\cong-V_{E E}\right)$, because the voltage at $(-)$ ve input is higher than that at the $(+)$ ve input. On the other hand, when $v_{i n}$ is greater than $V_{\text {ref }}$, the $(+)$ ve input becomes positive with respect to the $(-)$ ve input, and $v_{o}$ goes to $+V_{\text {sat }}\left(\cong+V_{C C}\right)$. Thus, $v_{o}$ changes from one saturation level to another whenever $v_{\text {in }} \cong V_{\text {ref }}$, as shown in Figure1-27. In


Figure 1-27 Non-inverting comparator


Figure 1-28 (a) Output if $V_{\text {ref }}$ is positive (b) Output if $V_{\text {ref }}$ is negative
short, the comparator is a type of analog-to-digital converter. At any given time, the $v_{o}$ waveform shows whether $v_{i n}$ is greater or less than $V_{\text {ref }}$. The comparator is sometimes also called a voltage level detector, because for a desired value of $V_{\text {ref }}$, the voltage level of the input $v_{\text {in }}$ can be detected.

In Figure 1-27, the diodes $D_{1}$ and $D_{2}$ pro-


Figure 1-29 Inverting comparator tect the op-amp from damage caused by the excessive input voltage $v_{i n}$. Because of these diodes, the difference input voltage $v_{i d}$ of the op-amp is clamped to either 0.7 V or -0.7 V ; hence, the diodes are called clamp diodes.

Ifthe reference voltage $V_{\text {ref }}$ is negative with respect to the ground, with sinusoidal signal applied to the $(+)$ ve input, the output waveform will be as shown in Figure 1-28. When $v_{\text {in }}>V_{\text {ref }}, v_{o}$ is at $+V_{\text {sat }}$; on the other hand, when $v_{i n}<V_{\text {ref }}, v_{o}$ is at $-V_{\text {sat }}$. The amplitude of $v_{\text {in }}$ must be large enough to pass through $V_{\text {ref }}$ if the switching action is to take place.
Figure 1-29 shows an inverting comparator in which the reference voltage $V_{\text {ref }}$ is applied to the $(+)$ ve input and $v_{i n}$ is applied to the $(-)$ ve terminal. In this circuit, $V_{\text {ref }}$ is obtained by using a potentiometer that forms a voltage divider with the dc supply voltages $+V_{C C}$ and $-V_{E E}$, and the wiper is connected to the $(+)$ ve input. As the wiper is moved towards $-V_{E E}, V_{\text {ref }}$ becomes more negative. When it is moved towards $+V_{C C} V_{\text {ref }}$ becomes more positive (see Figure 1-30). Thus, the reference voltage $V_{\text {ref }}$, of desired amplitude and polarity can be obtained by simply adjusting the potentiometer.

## 1-6-6 Integrator

A circuit in which the output voltage waveform is the integral of the input voltage waveform is the integrator or the integration amplifier. Such a circuit is obtained by using a basic inverting amplifier configuration if the feedback resistor $R_{F}$ is replaced by a capacitor $C_{F}$, as shown in Figure 1-31.


Figure 1-30 $\quad$ (a) Output if $V_{\text {ref }}$ is positive (b) Output if $V_{\text {ref }}$ is negative

The expression for the output voltage $v_{o}$ can be obtained by using KCL at node $v_{2}$ :

$$
i_{1}=I_{B}+i_{F}
$$

Since, $I_{B}$ is negligibly small:

$$
i_{1} \cong i_{F}
$$

Relation between the current through and voltage across the capacitor is given by:

$$
i_{C}=C \frac{d v_{C}}{d t}
$$

From Figure 1-31, applying KCL, we get:


Figure 1-31 The integrator circuit

$$
\frac{v_{i n}-v_{2}}{R_{1}}=C_{F} \frac{d}{d t}\left(v_{2}-v_{0}\right)
$$

However, $v_{1}=v_{2} \cong 0$, because $A$ is very large. Therefore:

$$
\frac{v_{i n}}{R_{1}}=C_{F}\left(\frac{d}{d t}\right)\left(-v_{0}\right)
$$

The output voltage can be obtained by integrating both sides with respect to time:

$$
\begin{aligned}
\int_{0}^{t} \frac{v_{i n}}{R_{1}} d t & =\int_{0}^{t} C_{F}\left(\frac{d}{d t}\right)\left(-v_{0}\right) d t \\
& =C_{F}\left(-v_{0}\right)+\left.v_{0}\right|_{t=0}
\end{aligned}
$$





Figure 1-32 Input and output waveforms
or,

$$
\begin{equation*}
v_{0}=-\frac{1}{R_{1} C_{F}} \int_{0}^{t} v_{i n} d t+c \tag{1-40}
\end{equation*}
$$

where, $C$ is the integration constant and is proportional to the value of the output voltage $v_{0}$ at time $t=0$.


Figure 1-33 Frequency response of integrator

Equation (1-40) indicates that the output voltage is directly proportional to the negative integral of the input voltage and inversely proportional to the time constant $R_{1} C_{F}$. The corresponding input and output waveforms are shown in Figure 1-32.

When $v_{i n}=0$, the integrator shown in Figure 1-33 works as an open-loop amplifier. This is because the capacitor $C_{F}$ acts as an open circuit $\left(X_{C F}=\infty\right)$ to the input offset voltage $V_{i o}$, i.e., the input offset voltage $V_{i o}$ and the part of the input current charging capacitor $C_{F}$ produce the error voltage at the output of the integrator.

## 1-6-7 Differentiator

The op-amp circuit whose output voltage is proportional to the differential form of the input voltage is known as differentiator.

Figure 1-34 shows the differentiator or differentiating amplifier. As the name suggests, the circuit performs the mathematical operation of differentiation; so, the output waveform is the derivative of the input waveform. The differentiator may be constructed from a basic inverting amplifier if an input resistor $R_{1}$ is replaced by capacitor $C_{1}$.

The expression for the output voltage can be obtained from KCL at node $v_{2}$ as follows,

$$
i_{C}=I_{B}+i_{F}
$$



Figure 1-34 The differentiator

Since, $i_{B} \cong 0: \quad i_{C}=i_{F}$





Figure 1-35 Input and output waveform

Table 1-3 Comparison between the output waveform of an integrator and a differentiator

| Input Signal <br> Waveform | Integrator Output <br> Waveform | Differentiator Output <br> Waveform |
| :--- | :--- | :--- |
| Sine | Minus cosine | Cosine |
| Square wave | Triangular wave | Pulse train |
| Triangular wave | Modified parabola | Square wave |
| Saw tooth wave | Parabolic ramp | Step function |
| Step function | Ramp function | Single pulse |
| Ramp function | Parabola | Step function |

$$
C_{1} \frac{d}{d t}\left(v_{i n}-v_{2}\right)=\frac{v_{2}-v_{o}}{R_{F}}
$$

However, $v_{1}=v_{2} \cong 0 \mathrm{~V}$, because $A$ is very large. Therefore:

$$
\begin{align*}
C_{1} \frac{d v_{i n}}{d t} & =-\frac{v_{o}}{R_{F}} \\
v_{o} & =-R_{F} C_{1} \frac{d v_{i n}}{d t} \tag{1-41}
\end{align*}
$$

Thus, the output $v_{o}$ is equal to $R_{F} C_{1}$ times the negative instantaneous rate of change of the input voltage $v_{i n}$ with time. Since the differentiator performs the reverse of the integrator's function, a cosine wave input will produce a sine wave output, or a triangular input will produce a square wave output as shown in Figure 1-35.

Table 1-3 shows the comparison between the output waveform of an integrator and a differentiator.

## 1-6-8 Logarithmic Amplifier



Figure 1-36 Logarithmic amplifier for positive input

If the feedback resistor $R_{f}$ in the op-amp circuit of Figure 1-36 is replaced by a diode, we obtain a logarithmic amplifier giving an output voltage $V_{o}$ that changes as the logarithm of the input voltage $V_{1}$.

The voltage-ampere characteristic of the diode is given by:

$$
i=I_{S}\left[\exp \left(\frac{e V_{f}}{\eta k_{B} T}\right)-1\right]
$$

where, $\quad e=1.6 \times 10^{-19} \mathrm{C}$

$$
\begin{aligned}
k_{B} & =1.38 \times 10^{-23} \mathrm{~J} / \mathrm{K} \\
T & =300 \mathrm{~K}
\end{aligned}
$$

Here, $i$ is the diode current for the forward voltage $V_{f}$ If $e V_{f} /\left(\eta k_{B} t\right) \gg 1$, then $i \gg I_{S}$.
We have:

$$
i=I_{S}\left[\exp \left(\frac{e V_{f}}{\eta k_{B} T}\right)\right]
$$

or,

$$
\ln \left(\frac{i}{I_{S}}\right)=\frac{e V_{f}}{\eta k_{B} T}
$$

Therefore,

$$
V_{f}=\frac{\eta k_{B} T}{e} \ln \left(\frac{i}{I_{S}}\right)
$$

Since $G$ is the virtual ground in Figure 1-36, we have $i=V_{1} / R_{1}$, and the output voltage is:

$$
V_{o}=-V_{f}=-\frac{\eta k_{B} T}{e} \ln \left(\frac{V_{1}}{R_{1} I_{S}}\right)
$$

Hence, $V_{o}$ responds to the logarithm of $V_{1}$.

## Solved Examples

Example 1-1 For an op-amp having a slew rate of $\mathrm{SR}=2 \mathrm{~V} / \mu \mathrm{s}$, what is the maximum closed-loop voltage gain that can be used when the input signal varies by $0.5 \mathrm{~V} / \mu \mathrm{s}$ ?

## Solution:

Since $V_{o}=A_{C L} V_{i}$, we have:

$$
\begin{gathered}
\mathrm{SR}=\frac{d V_{o}}{d t}=A_{C L} \frac{d V_{i}}{d t} \\
A_{C L}=\frac{\frac{d V_{o}}{d t}}{\frac{d V_{i}}{d t}}=\frac{\mathrm{SR}}{\frac{d V_{i}}{d t}}=\frac{2 \mathrm{~V} / \mu \mathrm{s}}{0.5 \mathrm{~V} / 10 \mu \mathrm{~s}}=40
\end{gathered}
$$

From this:

Example 1-2 A non-inverting amplifier has an input voltage of 1 V . The input resistance $R_{1}=1 \mathrm{k} \Omega$ and feedback resistance is $5 \mathrm{k} \Omega$. Find the output voltage and voltage gain of the amplifier.

## Solution:

Output voltage of a non-inverting amplifier is given by:

$$
\begin{aligned}
& v_{o}=\left(1+\frac{R_{F}}{R_{1}}\right) v_{i} \\
& v_{o}=\left(1+\frac{5}{1}\right) 1 \mathrm{~V}
\end{aligned}
$$

$$
\begin{aligned}
& v_{o}=6 \mathrm{volt} \\
& A_{v}=\frac{v_{o}}{v_{\text {in }}}=\frac{6}{1}=6 \mathrm{~V}
\end{aligned}
$$

Example 1-3 An inverting amplifier with input voltage is 1 V . Input resistance is $R_{1}=1 \mathrm{k} \Omega$ and feedback resistance is $5 \mathrm{k} \Omega$. Find the output voltage and voltage gain of the amplifier.

## Solution:

Output voltage of a non-inverting amplifier is given by:

$$
\begin{aligned}
v_{o} & =-\frac{R_{F}}{R_{1}} v_{i} \\
v_{o} & =-\frac{5}{1} \times 1 \mathrm{~V} \\
v_{o} & =-5 \mathrm{volt} \\
A_{v}=\frac{v_{o}}{v_{i n}} & =-\frac{5}{1}=-5 \mathrm{~V}
\end{aligned}
$$

Example 1-4 For an adder circuit, feedback resistance is $10 \mathrm{k} \Omega$. Input arm resistances are all $1 \mathrm{k} \Omega$. If the input voltages are $0.2 \mathrm{~V}, 0.3 \mathrm{~V}$ and 0.4 V , find the output voltage of the adder circuit.

## Solution:

Output of an adder is given by:

Since,

$$
V_{o}=-\left(\frac{R_{F}}{R_{a}} V_{a}+\frac{R_{F}}{R_{b}} V_{b}+\frac{R_{F}}{R_{c}} V_{c}\right)
$$

$$
\begin{aligned}
R_{a} & =R_{b}=R_{c}=R \\
V_{o} & =-\frac{R_{F}}{R}\left(V_{a}+V_{b}+V_{c}\right) \\
V_{o} & =-\frac{10}{1}(0.2+0.3+0.4) \\
V_{o} & =-10(0.9)=-9 \mathrm{~V}
\end{aligned}
$$

Example 1-5 For an adder circuit feedback resistance is $10 \mathrm{k} \Omega$. Input arm resistances are $1 \mathrm{k} \Omega$, $2 \mathrm{k} \Omega$ and $3.3 \mathrm{k} \Omega$. If the input voltage is $0.2 \mathrm{~V}, 0.06 \mathrm{~V}$ and 0.33 V , find the output voltage of the adder.

## Solution:

Output of an adder is given by:

$$
V_{o}=-\left(\frac{R_{F}}{R_{a}} V_{a}+\frac{R_{F}}{R_{b}} V_{b}+\frac{R_{F}}{R_{c}} V_{c}\right)
$$

$$
\begin{aligned}
V_{o} & =-\left[\frac{10}{1}(0.2)+\frac{10}{2}(0.06)+\frac{10}{3.3}(0.33)\right] \\
V_{o} & =-(2+0.3+1) \mathrm{V} \\
V_{o} & =-3.3 \mathrm{~V}
\end{aligned}
$$

Example 1-6 Determine the ideal voltage gain for the circuit shown in the following diagram.

## Solution:

Both the op-amps, as given in the diagram, are in an inverting configuration. With $v_{m}$ as the output of the first op-amp:

$$
v_{m}=-\frac{R_{F 1}}{R_{1}} v_{1}=-\frac{200 \mathrm{k} \Omega}{40 \mathrm{k} \Omega} v_{1}=-5 v_{1}
$$



Then, with $v_{m}$ taken as the input of the second op-amp:

$$
v_{o}=-\frac{R_{F 1}}{R_{1}} v_{m}=-\frac{200 \mathrm{k} \Omega}{20 \mathrm{k} \Omega} v_{m}=-10 v_{m}
$$

Since $v_{m}=-5 v_{1}: \quad \frac{v_{o}}{v_{1}}=-10(-5)=50$

Example 1-7 For the circuit, as shown in the following diagram, find the ratio $v_{o} / v_{i}$.

## Solution:

Applying KCL at node 1 :

$$
\frac{v_{1}-v_{i}}{R_{1}}+\frac{v_{1}-v_{o}}{R_{2}}+\frac{v_{1}-v_{a}}{R_{3}}=0
$$

Since $v_{1}=v_{+}=v_{-}=0$ for the first op-amp:


Using a voltage divider:

$$
v_{b}=\left(\frac{R_{4}}{R_{4}+R_{5}}\right) v_{o}
$$

Since $v_{a}=v_{+}=v_{-}=v_{b}$ for the second op-amp:

$$
-\frac{v_{i}}{R_{1}}=\frac{v_{o}}{R_{2}}+\frac{1}{R_{3}}\left(\frac{R_{4}}{R_{4}+R_{5}}\right) v_{o}
$$

Then:

$$
\frac{v_{o}}{v_{i}}=-\frac{1}{R_{1}\left[\frac{1}{R_{2}}+\frac{R_{4}}{R_{3}\left(R_{4}+R_{5}\right)}\right]}
$$

or,

$$
\frac{v_{o}}{v_{i}}=-\frac{R_{2} R_{3}\left(R_{4}+R_{5}\right)}{R_{1}\left(R_{3} R_{4}+R_{3} R_{5}+R_{2} R_{4}\right)}
$$

Example 1-8 For the circuit, as shown in the following diagram, determine the output voltage $v_{o}$ if the input voltage $v_{i}=1.2 \mathrm{~V}$.


## Solution:

These op-amps are in inverting configuration with $v_{m}$ designated as the output of the first op-amp.

$$
v_{m}=\left(1+\frac{R_{F, 1}}{R_{1,1}}\right) v_{i}=\left(1+\frac{400 \mathrm{k} \Omega}{100 \mathrm{k} \Omega}\right)(1.2 \mathrm{~V})=6 \mathrm{~V}
$$

Then, with $v_{0}$ designated as the input to the second op-amp and applying the superposition theorem, voltage at node $a$ due to $v_{m}$, we get:

$$
v_{a, m}=v_{m}\left(\frac{450 \mathrm{k} \Omega}{450 \mathrm{k} \Omega+150 \mathrm{k} \Omega}\right)=6 \times 0.75=4.5 \mathrm{~V}
$$

Again voltage at node $a$ due to $v_{0}$ :

$$
v_{a, o}=v_{o} \frac{150 \mathrm{k} \Omega}{150 \mathrm{k} \Omega+450 \mathrm{k} \Omega}=0.25 v_{o}
$$

But,

$$
v_{a, o}=v_{a, m}
$$

$$
\begin{array}{ll}
\text { or, } & 0.25 v_{o}=4.5 \mathrm{~V} \\
\therefore & v_{o}=\frac{4.5}{0.25}=18 \mathrm{~V}
\end{array}
$$

Example 1-9 The circuit, as given in the diagram, shows an ideal op-amp connected as a differential amplifier. Both the inverting and non-inverting terminals are used. Determine the expression for the output voltage $v_{o}$ as a function of $v_{i, 1}$ and $v_{i, 2}\left[v_{o}=f\left(v_{i, 1}, v_{i, 2}\right)\right]$. Then determine $v_{o}=f\left(v_{i, 1}, v_{i, 2}\right)$ if $R_{1}=R_{2}$.

## Solution:

For the non-inverting terminal at (+)ve node, KCL gives:

$$
\frac{V_{+}}{R_{2}}+\frac{v_{+}-v_{i, 2}}{R_{1}}=0
$$


or,

$$
\left(\frac{1}{R_{1}}+\frac{1}{R_{2}}\right) v_{+}=\frac{V_{i, 2}}{R_{1}}
$$

So that:

$$
v_{+}=\left(\frac{R_{2}}{R_{1}+R_{2}}\right) v_{i, 2}
$$

For the inverting terminal, at (-)ve node, KCL provides:

$$
\frac{v_{-}-v_{i, 1}}{R_{1}}+\frac{v_{-}-v_{o}}{R_{2}}=0
$$

or,

$$
\left(\frac{1}{R_{1}}+\frac{1}{R_{2}}\right) v_{-}=\frac{v_{i, 1}}{R_{1}}+\frac{v_{o}}{R_{2}}
$$

$v_{o}$ is given by:

$$
v_{o}=\left(\frac{R_{1}+R_{2}}{R_{1}}\right) v_{-}-\frac{R_{2}}{R_{1}} v_{i, 1}
$$

But,

$$
v_{+}=v_{-}
$$

$$
\begin{aligned}
\therefore \quad v_{o} & =\left(1+\frac{R_{2}}{R_{1}}\right)\left(\frac{R_{2}}{R_{1}+R_{2}}\right) v_{i, 2}-\frac{R_{2}}{R_{1}} v_{i, 1} \\
& =\frac{R_{2}}{R_{1}} v_{i, 2}-\frac{R_{2}}{R_{1}} v_{i, 1}
\end{aligned}
$$

So if, $\quad R_{1}=R_{2}$ :

$$
v_{o}=v_{i, 2}-v_{i, 1}
$$

Example 1-10 The following diagram shows an ideal op-amp that can be used as a strain gage, which is based on the fact that the value of resistance $\Delta R$ will change slightly when the resistor is bent or twisted. Determine the value of $\Delta R$ as a function of the input voltage $v_{i}$ and the two resistances $R_{a}$ and $R_{b}$.

## Solution:

Here, the node equation at 1 and 2 is given by:

$$
\frac{v_{-}-v_{i}}{R_{a}}+\frac{v_{2}-v_{o}}{R_{b}+\Delta R}=0
$$

and,

$$
\frac{v_{+}}{R_{b}}+\frac{v_{+}-v_{i}}{R_{a}}=0
$$



Then:

$$
v_{-}=\left(\frac{R_{b}+\Delta R}{R_{a}+R_{b}+\Delta R}\right) v_{i}+\left(\frac{R_{a}}{R_{a}+R_{b}+\Delta R}\right) v_{o}
$$

or,

$$
v_{-}=-\left(\frac{R_{a}}{R_{a}+R_{b}+\Delta R}-1\right) v_{i}+\left(\frac{R_{a}}{R_{a}+R_{b}+\Delta R}\right) v_{o}
$$

and,

$$
v^{+}=\left(\frac{R_{b}}{R_{a}+R_{b}}\right) v_{i}
$$

But,

$$
v_{-}=v_{+}
$$

$$
-\left(\frac{R_{a}}{R_{a}+R_{b}+\Delta R}-1\right) v_{i}+\left(\frac{R_{a}}{R_{a}+R_{b}+\Delta R}\right) v_{o}=\left(\frac{R_{b}}{R_{a}+R_{b}}\right) v_{i}
$$

$$
\left(\frac{R_{a}}{R_{a}+R_{b}+\Delta R}\right) v_{o}=\left(\frac{R_{b}}{R_{a}+R_{b}}+\frac{R_{a}}{R_{a}+R_{b}+\Delta R}-1\right) v_{i}
$$

After simplifying the previous expression we have:
$-R_{a} \Delta R v_{i}=R_{a}\left(R_{a}+R_{b}\right) v_{o}$
or, $\quad \Delta R=-\left(R_{a}+R_{b}\right) \frac{v_{o}}{v_{i}}$
Example 1-11 The circuit, as shown in the diagram, shows how an ideal op-amp can be put together using resistors that have relatively small resistance values. If $R_{1}=2000 \Omega$, determine the value of a single feedback resistor to produce a gain of -1200 , and then with $R_{1}=2000$ $\Omega$ and $R_{b}=50 \Omega$, determine the value of $R_{a}$ to provide a gain of -1200 .


## Solution:

This ideal op-amp is in the inverting configuration.
If $R_{1}=2000 \Omega$ and $v_{o} / v_{i}=-1200$, then:

$$
R_{F}=-R_{1} \frac{v_{o}}{v_{i}}=-2000 \times(-1200)=2.4 \mathrm{M} \Omega
$$

With $v_{+}=v_{-}=0$ :

$$
i_{1}=\frac{v_{i}-v_{-}}{R_{1}}=\frac{v_{1}}{R_{1}}
$$

and because the ideal op-amp does not draw current:

$$
i_{2}=i_{1}=\frac{v_{1}}{R_{1}}
$$

The voltage at node $a$ will be:

$$
v_{a}=v_{1}-R_{a} i_{2}=0-R_{a} i_{2}=-\frac{R_{a}}{R_{1}} v_{i}
$$

Noting that $i_{3}$ flows upward:

$$
i_{3}=\frac{0-v_{a}}{R_{b}}=\left(\frac{R_{a}}{R_{1} R_{b}}\right) v_{i}
$$

An application of KCL at node $a$ gives:

$$
i_{4}=i_{2}+i_{3}=\frac{1}{R_{1}} v_{i}+\left(\frac{R_{a}}{R_{1} R_{b}}\right) v_{i}=\left(\frac{R_{a}+R_{b}}{R_{1} R_{b}}\right) v_{i}
$$

so that:

$$
v_{o}=v_{a}-R_{a} i_{4}=-\frac{R_{a}}{R_{1}} v_{i}-\left(\frac{R_{a}\left(R_{a}+R_{b}\right)}{R_{1} R_{b}}\right) v_{i}
$$

$$
v_{o}=-\frac{R_{a}}{R_{1}}\left(1+\frac{R_{a}+R_{b}}{R_{b}}\right) v_{i}
$$

Now if $v_{o} / v_{i}=-1200, R_{b}=50 \Omega$ and $R_{1}=2000 \Omega$ :
$-1200=-\frac{R_{a}}{200 \Omega}\left(1+\frac{R_{a}+50 \Omega}{50 \Omega}\right)$
Hence, we have: $\quad R_{a}=10,900 \Omega$
Notice that four resistors with valves less than $12,000 \Omega$ can be used to take the place of a single feedback resistor of $2.4 \mathrm{M} \Omega$.

Example 1-12 The following diagram illustrates the use of the op-amp as a negative impedance converter. Determine the input resistance.


## Solution:

In this case:

$$
R_{i n}=\frac{v_{i n}}{i_{d}}
$$

Since the ideal op-amp does not draw current at either input terminal and because $v_{+}=v_{-}$:

$$
i_{b}=\frac{v_{1}}{R_{1}}
$$

KCL at node 1 gives: $\quad i_{e}=i_{b}=\frac{v_{1}}{R_{1}}$
Again by KVL, we have: $\quad v_{0}=v_{i}+R_{F} i_{c}=v_{i}+\frac{R_{F}}{R_{1}} v_{i}=\left(1+\frac{R_{F}}{R_{1}}\right) v_{i}$

By Ohm's law:

$$
i_{d}=\frac{v_{i}-v_{0}}{R}=\frac{v_{i}}{R}-\frac{1}{R}\left(1+\frac{R_{F}}{R_{1}}\right) v_{i}=-\frac{R_{F}}{R R_{1}} v_{i}
$$

Hence, the input resistance is:

$$
R_{i n}=\frac{v_{i}}{i_{d}}=-\frac{R_{1}}{R_{F}} R
$$

Example 1-13 An ideal op-amp in the inverting configuration is to have a gain of -125 and input resistance as high as possible. If no resistance in the op-amp circuit is to have a value higher than $5 \mathrm{M} \Omega$, how is this design achieved using just two resistors?

## Solution:

Here $R_{i n}$ is as high as possible, thus:

$$
R=R_{1}=\text { high }
$$



With gain $G=-\frac{R_{F}}{R_{1}}, R_{F}$ should be set at $5 \mathrm{M} \Omega$. Thus $R_{f}=5 \mathrm{M} \Omega$.

$$
\therefore \quad R_{1}=-\frac{R_{F}}{G}=-\frac{5 \mathrm{M} \Omega}{-125}=40000 \Omega
$$

Example 1-14 In the cascade of ideal op-amps, as shown in the following diagram, if $v_{i}=2 \mathrm{~V}$ and $v_{o}=30 \mathrm{~V}$, determine the value of $R$.


## Solution:

Observe that the first op-amp is in a non-inverting configuration, and the rest are in an inverting configuration. With $v_{o 1}$ as the output of first op-amp and $v_{o 2}$ as the output of second op-amp, we have:

Thus,

$$
\begin{aligned}
& \frac{v_{o}}{v_{i}}=\left(\frac{v_{o 1}}{v_{i}}\right)\left(\frac{v_{o 2}}{v_{o 1}}\right)\left(\frac{v_{o}}{v_{o 2}}\right) \\
&=\left(1+\frac{R_{f, 1}}{R_{1,1}}\right)\left(-\frac{R_{f, 2}}{R_{1,2}}\right)\left(-\frac{R_{f, 3}}{R_{1,3}}\right) \\
& \frac{30}{2}=\left(1+\frac{100 \mathrm{k} \Omega}{50 \mathrm{k} \Omega}\right)\left(-\frac{100 \mathrm{k} \Omega}{R}\right)\left(-\frac{100 \mathrm{k} \Omega}{25 \mathrm{k} \Omega}\right)
\end{aligned}
$$

Upon solving we get:

$$
R=80 \mathrm{k} \Omega
$$

Example 1-15 Find the relationship between $v_{o}, v_{s 1}$ and $v_{s 2}$ in the circuit, as shown in the following diagram.


## Solution:

Using the superposition theorem and with $v_{s 1}=0$ :

$$
\begin{gathered}
v_{2}=0\left(\text { voltage constraint applied to } A_{2}\right) \\
\left.v_{1}=-\frac{R_{1}}{R_{3}} v_{s 2} \text { (inverting amplifier }\right)
\end{gathered}
$$

Using superposition theorem again, and with $v_{2}=v_{1}$ and $v_{3}$ as ground referenced voltages:

$$
\begin{aligned}
v_{o}^{\prime} & =-\frac{R_{2}}{R_{1}} v_{1}+\left(1+\frac{R_{2}}{R_{3} \| R_{1}}\right) v_{s 2} \\
& =-\left(\frac{R_{2}}{R_{1}}\right)\left(\frac{R_{1}}{R_{3}}\right) v_{s 2}+\left(1+\frac{R_{2}\left(R_{1}+R_{3}\right)}{R_{1} R_{3}}\right) v_{s 2} \\
& =\left(1+\frac{R_{2}}{R_{1}}+\frac{2 R_{2}}{R_{3}}\right) v_{s 2}
\end{aligned}
$$

For $v_{s 2}=0$ and $v_{3}=0$ :

$$
\begin{aligned}
v_{2} & =v_{s 1} \\
v_{1} & =\left(1+\frac{R_{1}}{R_{3} \| R_{2}}\right) v_{s 2} \\
v_{o}^{\prime \prime} & =-\frac{R_{2}}{R_{1}} v_{s 1}-\frac{R_{2}}{R_{1}} v_{1} \\
& =-v_{s 1}\left(1+\frac{R_{2}}{R_{1}}+\frac{2 R_{2}}{R_{3}}\right)
\end{aligned}
$$

And with,

$$
\begin{aligned}
v_{o} & =v_{o}^{\prime}+v_{o}^{\prime \prime}: \\
& =\left(1+\frac{R_{2}}{R_{1}}+\frac{2 R_{2}}{R_{3}}\right)\left(v_{s 2}-v_{s 1}\right)
\end{aligned}
$$

Example 1-16 Find the $v_{1}$ and $v_{o}$ in terms of $v_{s 1}$ and $v_{s 2}$.


## Solution:

Using the superposition theorem and noticing that the cascade combination of U1 and the inverting circuit of U2 acts like an ideal op-amp with infinite open-loop gain:

$$
\begin{aligned}
& v_{o}^{\prime}=-K v_{s 1}\left(v_{s 2}=0,\right. \text { inverting amplifier) } \\
& v_{o}^{\prime \prime}=v_{s 2} \\
& =\frac{K R}{R+K R}\left(1+\frac{K R}{R}\right) \quad \text { (voltage division and non-inverting amplifier) } \\
& \\
& =K v_{s 2} \\
& v_{o}
\end{aligned}=v_{o}^{\prime}+v_{o}^{\prime \prime} .
$$

Since $v_{o}=-K v_{1}: \quad v_{1}=\frac{v_{o}}{-K}=v_{s 1}-v_{s 2}$
Example 1-17 Find $I_{s}$ in terms of $v_{c}$.


## Solution:

Using voltage division and the voltage and current constraints for $A_{1}$ we get:

$$
v_{1}=2 v_{L}(\text { referenced to ground })
$$

Using Ohm's law:

$$
I_{1}=\frac{v_{\mathrm{c}}-v_{L}}{R}
$$

and,

$$
I_{2}=\frac{v_{c}-v_{L}}{R}=\frac{v_{L}}{R}
$$

Applying KCL at node $A$ :

$$
\begin{aligned}
I_{s} & =I_{1}+I_{2} \\
& =\frac{v_{c}}{R}
\end{aligned}
$$

The circuit is a voltage-controlled current source. It is independent of $Z_{L}$ and is a function of $v_{c}$ and R .

Example 1-18 Using the op-amps, as shown in the diagram, find:
(a) $I_{s}$ in terms of $v_{c}$
(b) The necessary circuit changes to reverse the actual direction of $I_{s}$


## Solution:

(a) Because of the input voltage constraint $v_{1}=v_{c}$ of the op-amps, and applying Ohm's law to $R_{1}$ :

$$
I_{1}=\frac{v_{c}}{R_{1}}
$$

Due to the input current constraint of the op-amps, and because the source current $I_{s}$ and the drain current $I_{D}$ of a JFET transistor are equal:

$$
\begin{array}{ll} 
& I_{1}=I_{s}=I_{D} \\
\therefore & I_{\mathrm{s}}=\frac{v_{c}}{R_{1}}
\end{array}
$$

The JFET is a depletion mode device; $V_{G S}$ will be negative for the direction of $I_{s}$ shown. The output of the amplifier (or the gate voltage) will be at a value less positive than the source voltage ( or $v_{c}$ ).
(b) To reverse the actual direction of $I_{s}$ replace Q 1 , an $n$-channel device by a $p$-channel device, return $R_{L}$ to $V^{-}$, and reverse the polarity of $v_{c}$.
Example 1-19 Find $v_{o} / v_{s}$ for the circuit, as shown in the diagram. What mathematical function does the circuit perform for $\omega \ll 1 / R_{1} C$ ?


## Solution:

Using the superposition theorem and treating $v_{s}$ as two equal-valued sources:

$$
\begin{gathered}
v_{o}=-\frac{R_{2}}{R_{3}} v_{s}-\left(\frac{R_{2}}{R_{1}+\frac{1}{s C}}\right) v_{s} \\
v_{o}=-\frac{R_{2}}{R_{3}} v_{s}-\left\lfloor\frac{\left(\frac{R_{2}}{R_{1}}\right) s}{s+\frac{1}{R_{1} C}}\right\rfloor v_{s}
\end{gathered}
$$

For $\omega \ll \frac{1}{R_{1} C}$ :

$$
v_{o}=-\frac{R_{2}}{R_{3}} v_{s}-s C R_{2} v_{s}
$$

The output voltage is a function of the input voltage and its derivative.

Example 1-20 Find the relationship between $v_{0}$ and the inputs $I_{s 1}$ and $I_{s 2}$.

## Solution:

Because the non-inverting input of U1 is at the ground and because of the voltage constraints of U1 and U2, the inputs of U1 and U 2 are at zero volts.

Applying the current constraint to the inverting input of U 2 and the Ohm's law:

$$
v_{2}=-I_{s 2} R_{1}
$$

tApplying the current constraint and Ohm's law:

$$
I_{3}=-\frac{v_{2}}{R_{1}}=I_{s 2}
$$



Applying KCL to node $A$ :

$$
I_{4}=I_{s 1}-I_{3}=I_{s 1}-I_{s 2}
$$

Using Ohm's law:

1-44 Basic Electronics

$$
v_{o}=-\left(I_{s 1}-I_{s 2}\right) R_{2}=R_{2}\left(I_{s 2}-I_{s 1}\right)
$$

The output voltage of the circuit is proportional to the difference between the input currents.
Example 1-21 Using the following diagram, determine:
(a) $\omega_{0}$ (b) $\mathrm{K} \quad$ (c) The minimum value of K that will sustain oscillation


## Solution:

(a) The frequency of oscillation is obtained from loop 1. The loop gain is obained from loop 2. The frequency where the loop gain is one.
Loop gain:

$$
L_{G}(\mathrm{~s})=\frac{v_{o}}{v_{\alpha}}
$$

Using the op-amps input constraints and Ohm's law:

$$
\begin{gathered}
I_{1}=-\frac{v_{o}}{K R} \\
V_{A}=I_{1} \frac{1}{s C}=-\frac{v_{o}}{s K R C} \\
I_{A}=\frac{V_{A}}{R}
\end{gathered}
$$

Using KVL, KCL and Ohm's law:

$$
\begin{gathered}
I_{3}=I_{1}+I_{2}=I_{1}+\frac{V_{A}}{R}=-\frac{v_{o}}{K R}-\frac{v_{o}}{s K R^{2} C} \\
V_{B}=V_{A}+I_{3} \frac{1}{s C}
\end{gathered}
$$

$$
\begin{aligned}
& I_{5}=I_{3}+I_{4}=I_{3}+\frac{V_{B}}{R} \\
& V_{\alpha}=V_{B}+I_{5} \frac{1}{S C}
\end{aligned}
$$

Using the expression for $I_{5}$ in terms of $v_{o}$, solving for $L_{G}(s)$, and replacing $s$ by $j \omega$ :

$$
\frac{v_{o}}{v_{\alpha}}(j \omega)=\frac{K \omega^{2} R^{2} C^{2}}{4+j\left[3 \omega R C-\frac{1}{(\omega R C)}\right]}
$$

For $L_{G}\left(j \omega_{o}\right)=1: \quad \omega_{o}=\frac{1}{\sqrt{3} R C}$
(b) For loop gain, $v_{o} / v \alpha=1$ :

$$
K=12
$$

(c) The minimum value of K , which is necessary to sustain the oscillation, is 12 .

Example 1-22 The circuit, as shown in the following diagram is a simulated inductor. Find $L_{E q}$ uation


## Solution:

The U1 circuit is non-inverting amplifier where:

$$
V_{2}=\frac{s R C+1}{s R C} V_{1}
$$

Using superposition theorem for the U2 circuit:

$$
\begin{aligned}
V_{3} & =-V_{2}+2 V_{1} \\
& =\frac{s R C-1}{s R C} V_{1}
\end{aligned}
$$

Using Ohm's law and the input current constraint for U2:

1-46 Basic Electronics

$$
I_{1}=\frac{V_{1}-V_{3}}{R}=\frac{V_{1}}{s R^{2} C}
$$

The network's input impedance is:

$$
\frac{V_{1}}{I_{1}}=s\left(R^{2} C\right)=s L_{e q}
$$

where, $L_{e q}=R^{2} C$
Example 1-23 Find $T(s)=V_{o} / V_{s}$ for the above circuit. Determine the relationships between $R_{1}, R_{2}$, $R_{3}$ and $R_{4}$ for $T(s)$ to have an LP response, an HP response and an AP response.


## Solution:

$T(s)$ is found by splitting $V_{s}$ into two equal valued sources and using superposition theorem:

$$
\begin{aligned}
V_{o}^{\prime} & =-\frac{V_{s}\left(R_{2} / R_{1}\right)}{1+s R_{2} C} \\
V_{o}^{\prime \prime} & =-V_{s} \frac{R_{3}}{R_{3}+R_{4}} \frac{s R_{1} R_{2} C+R_{1}+R_{2}}{s R_{1} R_{2} C+R_{1}} \\
V_{o} & =V_{o}^{\prime}+V_{o}^{\prime \prime} \\
& =V_{s} \frac{-R_{2}\left(s R_{2} C+1\right) K\left(s R_{2} C+1\right)\left(s R_{1} R_{2} C+R_{1}+R_{2}\right)}{\left(s R_{2} C+1\right)\left(s R_{1} R_{2} C+R_{1}\right)}
\end{aligned}
$$

where, $\quad K=\frac{R_{4}}{R_{3}+R_{4}}$
Solving for $T(s)$ produces:

$$
T(s)=\frac{R_{3}}{R_{3}+R_{4}} \frac{s+\left\{\left[\frac{1}{\left(K_{1} C\right)}\right]\left(\frac{R_{1}}{R_{2}}-\frac{R_{3}}{R_{4}}\right)\right\}}{s+\frac{1}{\left(R_{2} C\right)}}
$$

For an LP response, $R_{3}=0$. For an HP response, $R_{1} R_{4}=R_{2} R_{3}$ and for an LP response, $R_{2} R_{3}=2 R_{1} R_{4}$.

## 1-7 REAL-LIFE APPLICATIONS

The op-amp is the basic component of analog computers. The typical uses of op-amp include providing amplitude changes in oscillators, active filter circuits and amplifier circuits of electronic instruments. In analog computers it is used to solve mathematical equations, simulate physical systems and to control physical process. The programming of analog computer is to arrange op-amps in different modes to solve mathematical, logical problems of certain equations. Mathematical functions for the solution of equation include integration, differentiation, summation, subtraction, etc. Op-amp is also used in many electronic devices as an amplifier, voltage multiplier, etc. Calculators, phase changer circuits also use the op-amp. It should be kept in mind that the op-amp is only used for low-power devices. It cannot be used in high-power applications.

## POINTS TO REMEMBER

1. The operational amplifier is a differential amplifier.
2. Important properties of ideal op-amp:
(a) Gain of an ideal op-amp is infinite.
(b) Output voltage is zero when input voltages are same or when both are zero.
(c) Input resistance infinite.
(d) Output resistance is zero.
(e) CMRR must be infinity.
(f) Infinite bandwidth.
3. Offset voltage occurs due to the mismatch of op-amp internal transistor.
4. Common-mode rejection ratio (CMRR) is defined as the ratio of the differential voltage gain $A_{d}$ to the common-mode voltage gain $A_{c m}$.
5. Slew rate (SR) is defined as the maximum rate of change of output voltage per unit of time and is expressed in volts per micro seconds.

## IMPORTANT FORMULAE

1. Output voltage of a non-inverting amplifier is given by:

$$
v_{o}=\left(1+\frac{R_{F, 1}}{R_{1,1}}\right) v_{i}
$$

2. Output of an inverting amplifier is given by:

$$
V_{o}=-\left(\frac{R_{F}}{R_{1}}\right) V_{\text {in }}
$$

3. Output of an adder is given by:

$$
=\frac{A_{d}}{A_{c m}}
$$

$$
V_{o}=-\left(\frac{R_{F}}{R_{a}} V_{a}+\frac{R_{F}}{R_{b}} V_{b}+\frac{R_{F}}{R_{c}} V_{c}\right)
$$

4. The common-mode rejection ratio is given by:

CMRR $=\frac{\text { Differential voltage gain }}{\text { Common mode voltage gain }}$
5. Slew rate is given by:

$$
S R=\left.\frac{d V_{o}}{d t}\right|_{\text {maximum }} \mathrm{V} / \mu \mathrm{s}
$$

6. Differentiator output is given by:

$$
v_{o}=-R_{F} C_{1} \frac{d v_{i n}}{d t}
$$

7. Integrator output is given by:

$$
v_{o}=-\frac{1}{R_{1} C_{F}} \int_{0}^{t} v_{\text {in }} d t+c
$$

## OBJECTIVE QUESTIONS

1. Op-amp is a/an:
(a) Differential amplifier
(b) Oscillator
(c) Rectifier
(d) None of the above
2. Op-amp operates at a:
(a) High voltage ( $\sim 100 \mathrm{KV}$ )
(b) Medium voltage ( $\sim 220$ Volt)
(c) Low voltage ( $\sim 12$ Volt)
(d) Very high voltage ( $\sim 10$ mili Volt)
3. Voltage gain of an ideal op-amp is:
(a) Infinite
(b) Very high
(c) Low
(d) Very low
4. Bandwidth of an ideal op-amp is:
(a) Infinite
(b) Very high
(c) Low
(d) Very low
5. Output Impedance of an ideal op-amp is:
(a) Infinite
(b) Very high
(c) Low
(d) Zero
6. Input impedance of an ideal op-amp is:
(a) Infinite
(b) Very high
(c) Low
(d) Zero
7. CMRR of an ideal op-amp is:
(a) Infinite
(b) Very high
(c) Low
(d) Very low
8. Slew rate of an ideal op-amp is:
(a) Infinite
(b) Very high
(c) Low
(d) Very low
9. Op-amp is a:
(a) Voltage-controlled voltage source (VCVS)
(b) Voltage-controlled current source (VCCS)
(c) Current-controlled voltage source (CCVS)
(d) Current-controlled current source (CCCS)
10. Op-amp uses:
(a) Only + ve voltage
(b) Only - ve voltage
(c) Dual supply, i.e., $\pm V_{C C}$
(d) None of the above
11. Virtual ground of an op-amp is:
(a) The terminal is grounded directly
(b) The terminal is not physically grounded but terminal voltage is zero as the other terminal is connected to the ground due to op-amp properties
(c) Both (a) and (b)
(d) None of the above
12. Op-amp uses:
(a) Negative feedback
(b) Positive feedback
(c) No feedback
(d) None of the above
13. Common-mode gain signifies:
(a) That the ability to reject the common mode signals like noise, interference
(b) Increase in the noise
(c) Increase in the distortion
(d) All of the above
14. Slew rate is defined as the:
(a) Maximum rate of change of output voltage with time
(b) Minimum rate of change of output voltage with time
(c) Moderate rate of change of output voltage with time
(d) None of the above
15. Op-amp integrator uses:
(a) Capacitor as feedback element
(b) Resistor as feedback element
(c) Inductor as feedback element
(d) A simple wire as feedback element
16. Match the following table columns w.r.t an integrator:

## Input signal waveform

(a) Square wave

## Integrator output waveform

(i) Modified parabola
(b) Triangular wave
(c) Saw-tooth wave
(d) Step function
(ii) Triangular wave
(iii) Parabolic
(iv) Ramp function
17. Match the following table columns w.r.t a differentiator:

## Input signal waveform

## Differentiator output waveform

(a) Sine
(i) Square wave
(b) Square wave
(ii) Pulse train
(c) Triangular wave
(d) Saw-tooth wave
(iii) Cosine
(iv) Step function
18. The high input impedance of an IC op-amp is achieved by using:
(a) FET
(b) CE transistor stages
(c) MOSFET.
(d) Darlington connection
19. The closed-loop gain of an inverting op-amp is:
(a) Equal to unity
(b) Greater than unity
(c) Less than unity
(d) Zero
20. The open-loop gain of an op-amp is:
(a) Large
(b) Zero
(c) Small
(d) Anything

## REVIEW QUESTIONS

1. What is an operational amplifier? Provide the circuit symbol of an op-amp.
2. (a) List the characteristics of an ideal op-amp.
(b) Explain clearly how an op-amp can be used as: (i) a summing amplifier (ii) an integrator.
3. Explain with the help of a diagram, how two supply voltages $+V$ and $-V$ are obtained from a single dual power supply.
4. Why is the gain of an amplifier circuit independent of the gain of the op-amp employed?
5. In circuit analysis of an ideal op-amp with feedback, what values are assumed for $V_{i}$ and $I_{i}$ ? Why?
6. What is differential amplifier? Explain with a diagram, the action of a differential amplifier.
7. What is meant by CMRR? Explain the significance of a relatively large value of CMRR.
8. Explain why open-loop op-amp configurations are not used in linear applications.
9. Explain clearly, how an op-amp can be used for the following applications:
(a) Inverting amplifier
(b) Differentiator
(c) Integrator
(d) Summing amplifier

Provide appropriate diagrams.
10. List the differences between the integrator and the differentiator.
11. Explain how an op-amp is checked by using it as a buffer.
12. Explain virtual ground.
13. The gain of a buffer amplifier is unity. Explain this statement.
14. Write the ideal values for each of the following parameters. There are three voltage sources $V_{1}, V_{2}$ and $V_{3}$. It is required to obtain the sum of these signals without the change in the magnitude and sign. Write a suitable circuit and explain its operation.
15. What is the difference between open-loop and closed-loop gains of an op-amp?
16. Show the internal block schematic of an op-amp while mentioning the role of each stage.
17. Define the following terms for an op-amp:
(a) CMRR
(b) Slew rate
(c) Virtual ground
(d) Schmitt trigger
(e) Voltage-to-current converter
(f) Current-to-voltage converter
18. Explain how a triangular wave can be generated by using op-amp.
19. Describe the use of an op-amp as a stable multi-vibrator.
20. What is a regenerative comparator?
21. Draw a schematic diagram of a scale changer and explain its working principle.
22. Describe the significance of virtual ground.

## PRACTICE PROBLEMS

1. Calculate the voltage gain of an inverting amplifier, given that $R_{l}=8 \mathrm{k} \Omega$ and $R_{f}=56 \mathrm{k} \Omega$.
2. For an inverting amplifier, $R_{1}=2 \mathrm{k} \Omega$ and $R_{f}=1 \mathrm{M} \Omega$. Determine the following circuit values:
(a) $A_{v}$
(b) $R_{i}$
(c) $R_{o}$
3. For inverting amplifier, let $R_{f}=250 \mathrm{k} \Omega$, $R_{\mathrm{I}}=10 \mathrm{k} \Omega$ and $V_{i}=0.5 \mathrm{~V}$. Calculate:
(a) $I$
(b) The voltage across $R_{f}$
(c) $V_{o}$
4. Design an inverting amplifier with a gain of -5 and an input resistance of $10 \mathrm{k} \Omega$.
5. Calculate the output voltage of an inverting amplifier, if $R_{I}=50 \mathrm{k} \Omega, R_{f}=500 \mathrm{k} \Omega$ and $V_{i}=20.4 \mathrm{~V}$.
6. Calculate the output voltage of non-inverting amplifier, if $R_{I}=50 \mathrm{k} \Omega, R_{f}=500 \mathrm{k} \Omega$ and $V_{i}=0.4 \mathrm{~V}$.
7. Calculate the value of the feedback resistor given that $A_{v}=-100$ and $R_{I}=1 \mathrm{k} \Omega$, in the case of an inverting amplifier.
8. Design an amplifier with a gain of +10 .
9. Calculate the voltage gain of non-inverting amplifier 0 input is 0 mV .
10. Calculate the output voltage of a three input adder for the following values: $R_{1}=20 \mathrm{k} \Omega, R_{2}=40 \mathrm{k} \Omega, R_{3}=60 \mathrm{k} \Omega$ and $R_{f}=100 \mathrm{k} \Omega, V_{I}=20 \mathrm{mv}, V_{2}=$ 40 mV and $V_{3}=60 \mathrm{mV}$.
11. Calculate the output voltage of an adder for the following values: $R_{I}=250 \mathrm{k} \Omega$, $R_{2}=500 \mathrm{k} \Omega, R_{3}=1 \mathrm{M} \Omega, V_{I}=-3 \mathrm{~V}$, $V_{2}=3 \mathrm{~V}$ and $V_{3}=2 \mathrm{~V}$.
12. In the subtractor circuit $R_{I}=5 \mathrm{k} \Omega$, $R_{f}=10 \mathrm{k} \Omega, V_{I}=4 \mathrm{~V}$ and $V_{2}=5 \mathrm{~V}$. Find the value of output voltage.
13. Calculate the output voltage of subtractor circuit if $R_{I}=2 \mathrm{k} \Omega, R_{f}=10 \mathrm{k} \Omega, V_{I}=3 \mathrm{~V}$ and $V_{2}=6 \mathrm{~V}$.
14. The input of the differentiator is a sinusoidal voltage of peak value 5 mV and frequency 1 kHz . Find the output if $R=100 \mathrm{k} \Omega$ and $C=1 \mathrm{~F}$.
15. A $10 \mathrm{mV}, 5 \mathrm{kHz}$ sinusoidal signal applied to the input of an op-amp integrator for which $R=100 \Omega$ and $C=1$ F. Find the output voltage.
16. Design an adder using an op-amp to get the output expression as:

$$
V_{o}=-\left(0.1 V_{1}+V_{2}+20 V_{3}\right)
$$

where, $V_{1}, V_{2}$ and $V_{3}$ are the inputs.

## SUGGESTED READINGS

1. Singh, J. 1994. Semiconductor Devices: An Introduction. New York, NY: McGraw-Hill.
2. Streetman, B.G. and S. Banerjee. 2000. Solid State Electronic Devices. New Delhi: Pearson Education.
3. Millman, Jacob and Christos C. Halkias. 1986. Integrated electronics: Analog and Digital Circuits and Systems. New Delhi: McGraw Hill Book Company.
4. Pierret, R. F and G.W. Neudeck. 1989. Modular Series on Solid State Devices. Boston, M.A.: Addison Wesley.
5. Singh, B.P. and Rekha Singh. 2006. Electronic Devices and Integrated Circuits. New Delhi: Pearson Education.

This page is intentionally left blank.

## 2

## Diode Fundamentals

## Outline

2-1 Introduction
2-2 Formation of the $p-n$ Junction
2-3 Energy Band Diagrams
2-4 Concepts of Junction Potential
2-5 Modes of the $p-n$ Junction

2-6 Derivation of the I-V Characteristics of a
$p-n$ Junction Diode

## 2-7 Linear Piecewise Models

2-8 Breakdown Diode

## Objectives

This chapter introduces the reader to the first non-linear element in the whole field of electronics, namely the diode. William Shockley first demonstrated the diode in his famous paper on this topic, and discussed the formation of the $p-n$ junction and the energy band diagram together with the basic concept of built-in potential. In analog electronics the modes of operation of the $p-n$ junction is very important. The fundamental concepts of the junction capacitance, the I-V characteristics and linear piecewise models have been introduced for better understanding. Breakdown diodes that are very important components in power electronics have been discussed along with Zener and Avalanche breakdown.

## 2-1 INTRODUCTION

The origin of a wide range of electronic devices being used can be traced back to a simple device, the $p-n$ junction diode. The $p-n$ junction diode is formed when a p-type semiconductor impurity is doped on one side and an n-type impurity is doped on the other side of a single crystal. All the macro effects of electronic devices, i.e., wave shaping, amplifying or regenerative effects, are based on the events occurring at the junction of the $p-n$ device. Most modern devices are a modification or amalgamation of $p-n$ devices in various forms. Prior to the era of semiconductor diodes, vacuum tubes were being extensively used. These were bulky, costly and took more time to start conducting because of the thermo-ionic emission. The semiconductor diodes and the allied junction devices solved all these problems. The $p-n$ junction forms the basis of the semiconductor devices in general. This chapter starts with a discussion on the formation of the $p-n$ junction diode and the corresponding energy band diagrams explicating their fundamental importance in the field of solid state electronics.


Figure 2-1 A semiconductor $p-n$ junction

## 2-2 FORMATION OF THE p-n JUNCTION

When donor impurities are introduced into one side and acceptors into the other side of a single crystal semiconductor through various sophisticated microelectronic device-fabricating techniques, a $p-n$ junction is formed. The $p-n$ junction is thus formed by an intimate contact, as shown in Figure 2-1. The presence of a concentration gradient between two materials in such intimate contact results in a diffusion of carriers that tends to neutralize this gradient. This process is known as the diffusion process.

The nature of the $p-n$ junction so formed may, in general, be of two types:
(i) A step-graded junction
(ii) A linearly-graded junction

In a step-graded semiconductor junction, the impurity density in the semiconductor is constant. In a linearly-graded junction, the impurity density varies linearly with distance away from the junction.

## 2-3 ENERGY BAND DIAGRAMS

The discussion in this section is based on the realistic assumption that a junction is made up of uniformly doped $p$-type and $n$-type crystals forming a step-graded junction. The variations in the expressions due to the other types of junctions will be mentioned later on.

## 2-3-1 The $p-n$ Junction at Thermal Equilibrium

It is assumed that the discontinuity at the junction surfaces is confined within a narrow region of length $L$, as shown in Figures 2-2(b) and 2-2(c), and that on either side of the junction the non-degenerate carrier concentrations are uniform, on planes parallel to the junction surface. Figure 2-2(a) exhibits the location of Fermi energy in $p$ - and $n$-type semiconductors just before contact. Figure 2-2(b) shows the formation of the $p-n$ junction after contact, which is based on the fact that the Fermi energy becomes invariant with respect to distance.

Figure 2-2(c) shows the energy band diagram of the $p-n$ junction under the condition of thermal equilibrium. A $p-n$ junction is said to be in thermal equilibrium when it is at a uniform temperature and no external disturbances, such as light or a bias voltage, are acting on it leading to a steady state charge and potential distribution. The carrier concentrations on either side away from the junction are given by:


Figure 2-2(a) $\quad p$-type and $n$-type semiconductors just before contact


Figure 2-2(b) Band structure of $p-n$ junction


Figure 2-2(c) The energy band diagram of a $p-n$ junction under the condition of thermal equilibrium

$$
\begin{array}{lll}
n_{n} \approx N_{d} & p_{n} \approx \frac{n_{i}^{2}}{N_{d}} & (\text { For } n \text {-type }) \\
p_{p} \approx N_{a} & n_{p} \approx \frac{n_{i}^{2}}{N_{a}} & (\text { For } p \text {-type }) \tag{2-1b}
\end{array}
$$

where $p_{n}$ is the hole concentration in $n$-type semiconductors, $n_{p}$ is the electron concentration in $p$-type semiconductors; $n_{n}$ and $p_{p}$ are the electron and hole concentrations in $n$ - and $p$-type semiconductors respectively. The behaviour of these carriers in a junction is intimately related to the potential formulation of the junction.

## 2-4 CONCEPTS OF JUNCTION POTENTIAL

## 2-4-1 Space-Charge Region

The non-uniform concentration of holes and electrons at the junction gives rise to a diffusive flow of carriers. Since the electron density is higher in the $n$-type crystal than in the $p$-type crystal, electrons flow from the $n$-type to the $p$-type and simultaneously, due to reversibility, the holes flow from the $p$-type to the $n$-type. The result of this migration of carriers is that the region near the junction of the $n$-type is left with a net positive charge (only ionized donor atoms) while that of the $p$-type is left with a net negative charge (only ionized acceptor atoms). This diffusive mechanism of migration of the carriers across the junction creates a region devoid of free carriers, and this region is called the space-charge region, the depletion region or the transition region. Thus, in the neighbourhood of the junction we will find a space charge that is a net charge. It is to be noted that the space charge, both negative and positive, must be equal, which effectively means that the opposite they must be numerically equal. It may be noted that the number of free carriers is particularly significant near the edges of the space-charge region.

The junction, as noted above, has three major properties: (i) There is a space charge and an electric field across the junction, which in turn indicates that the junction is pre-biased (i.e., there exists a built-in potential, a very important concept, which will be discussed shortly); (ii) The impure atoms maintaining the space charge are immobile in the temperature range of interest (at very high temperatures, the impurities become mobile). The pre-biased condition can be maintained indefinitely; (iii) The presence of any free electron or hole is strictly forbidden.

## 2-4-2 Built-in and Contact Potentials

This diffusive flow process results in a space-charge region and an electric field. The resulting diffusion current cannot build up indefinitely because an opposing electric field is created at the junction. The homogeneous mixing of the two types of carriers cannot occur in the case of charged particles in a $p-n$ junction because of the development of space charge and the associated electric field $E_{0}$. The electrons diffusing from the $n$-type to the $p$-type leave behind uncompensated donor ions in the $n$-type semiconductor, and the holes leave behind uncompensated acceptors in the $p$-type semiconductors. This causes the development of a region of positive space charge near the $n$-side of the junction and negative space charge near the $p$-side. The resulting electric field is directed from positive charge towards negative charge. Thus, $E_{0}$ is in the direction opposite to that of the diffusion current for each type of carrier. Therefore, the field creates a drift component of current from $n$ to $p$, opposing the diffusion component of the current. Since no net current can flow across the junction at equilibrium, the current density due to the drift of carriers in the $E_{0}$ field must exactly cancel the current density due to diffusion of carriers. Moreover, since there can be no net build-up of electrons or holes on either side as a function of time, the drift and diffusion current densities must cancel for each type of carrier.

Therefore, the electric field $E_{0}$ builds up to the point where the net current density is zero at equilibrium. The electric field appears in the transition region of length $L$ about the junction, and there is an equilibrium potential difference $V_{0}$ across $L$ (known as contact potential). In the electrostatic potential diagram, there is a gradient in potential in the direction opposite to $E_{0}$. In accordance with the following fundamental relation:

$$
E_{0}(x)=-\frac{d V(x)}{d x}
$$

the electric field is zero in the neutral regions outside $L$. The contact potential appearing across $L$ under condition of zero external bias is a built-in potential barrier, in that it is necessary for the maintenance of equilibrium at the junction. It does not imply any external potential. $V_{0}$ is an equilibrium quantity, and no net current can result from it. In general, the contact potential is the algebraic sum of the built-in potential and the applied voltage. The variations in the contact potential under the condition of applied bias are given in the subsequent sections.

The field is in a direction that opposes further migration of carriers. Since there can be no current flow in the steady state equilibrium condition, the tendency for the diffusion current density is exactly balanced by the tendency for drift current density due to the transition region field. The presence of the field $E_{0}$ in the transition region (space-charge region) implies the formation of a potential barrier $V_{d}$ for the charge carriers. Assuming that the field is confined within the space-charge region $L$, the potential barrier $V_{d}$ and the field $E_{0}$ are related by:

$$
\begin{equation*}
V_{d}=\left|\left.\right|_{x} ^{x} \int_{n}^{x} E_{0} d x\right| \tag{2-2}
\end{equation*}
$$

It should be noted that a voltmeter cannot measure this electrostatic potential since the internal field is set up to oppose the diffusion current and also since the built-in potential is cancelled exactly by the potential drop across the contact. The barrier energy corresponding to barrier potential $V_{d}$ is expressed as $E_{B}=e V_{d}$, as shown in Figure 2-2(c). The value of $E_{B}$ can be changed by doping change. The value of $E_{B}$ is different for different semiconductors.

## 2-4-3 Effect of Doping on Barrier Field

The width of the depletion region is inversely proportional to the doping strength, as a larger carrier concentration enables the same charge to be achieved over a smaller dimension. It should be noted that the depletion charge for different doping is not constant. The barrier field is normally independent of the doping concentration except under conditions of heavy doping, which may alter the band-gap itself, thereby modifying the barrier field. The value of $V_{d}$ in terms of the hole and electron concentrations can be derived in the following manner.

At thermal equilibrium, the non-degenerate electron concentrations for the $n$-type and $p$-type can be written as:

$$
\begin{align*}
& n_{n}=N_{c} e^{-\left(E_{c n}-E_{f n}\right) / k_{B} T}  \tag{2-3a}\\
& n_{p}=N_{c} e^{-\left(\begin{array}{cc}
E & -E_{f p}
\end{array}\right)^{/ k_{B} T}} \tag{2-3b}
\end{align*}
$$

where $E_{c n}, E_{c p}, E_{f n}$, and $E_{f p}$ are the conduction and Fermi level energies of the $n$-type and $p$-type semiconductors, respectively, and $N_{c}$ is the effective density-of-states. From Equations (2-3) and (2-1), the Fermi levels are given by:

$$
\begin{gather*}
E_{f n}=E_{c n}-k_{B} T \ln \frac{N_{c}}{N_{d}}  \tag{2-4a}\\
E_{f p}=E_{c p}-k T \ln \frac{N_{c} N_{a}}{n_{i}^{2}} \tag{2-4b}
\end{gather*}
$$

At equilibrium condition, the Fermi level must be constant throughout the entire crystal. Otherwise, because of the availability of lower energy levels, a flow of carriers would result. The Fermi levels,
therefore, must line up at the equilibrium. This extremely important theorem, which is the key in drawing the energy-band diagrams of various junction semiconductor devices, will now be proved.

## FOR ADVANCED READERS

## Invariance of Fermi Level at Thermal Equilibrium

Let us consider the existence of the energy level $E$ that is identical in the two materials, 1 and 2, which are in physical contact with each other as shown in Figure 2-3. Therefore, the electron in material 1 with energy $E$ are able to move in material 2 with the same energy $E$ without any expenditure of energy. Besides, the electrons must be available at energy $E$ in material 1, and there must be allowed empty energy states at energy $E$ in material 2.

Under the condition of a thermal equilibrium there is no current. Therefore, there is no net charge transfer and consequently there is also no net transfer of energy. Thus, for each energy $E$ the opposite transfer of electrons from material 2 to material 1 must exactly balance any transfer of electrons from mate-


Figure 2-3 The contact equilibrium diagram of two materials rial 1 to material 2.

At energy $E$, the rate of transfer of electrons from material 1 to material 2 is proportional to the number of filled states at $E$ in material 1 multiplied by the number of empty states at in material 2. By using the product law of probability, the rate of transfer of electrons $\left(R_{12}\right)$, from material 1 to material 2 is given by:

$$
\begin{equation*}
R_{12}=\left[C_{1} N_{1}(E) f_{1}(E)\right] \times\left\{N_{2}(E)\left[1-f_{2}(E)\right]\right\} \tag{2-5}
\end{equation*}
$$

where, $C_{1}$ is a constant and $f(E)$ is the well-known Fermi-Dirac distribution function. Similarly, the rate of transfer of electrons from material 2 to material $1\left(R_{21}\right)$ can be expressed as:

$$
\begin{equation*}
R_{21}=\left[C_{1} N_{2}(E) f_{2}(E)\right] \times\left\{N_{1}(E)\left[1-f_{1}(E)\right]\right\} \tag{2-6}
\end{equation*}
$$

At the thermal equilibrium, these rates must be equal and thus we can write:

$$
\begin{equation*}
\left[N_{1}(E) f_{1}(E)\right] \times\left\{N_{2}(E)\left[1-f_{2}(E)\right]\right\}=\left[N_{2}(E) f_{2}(E)\right] \times\left\{N_{1}(E)\left[1-f_{1}(E)\right]\right\} \tag{2-7a}
\end{equation*}
$$

Dividing both sides by $N_{1}(E) N_{2}(E) f_{1}(E) f_{2}(E)$ we get:

$$
\begin{equation*}
\frac{1}{f_{2}(E)}-1=\frac{1}{f_{1}(E)}-1 \tag{2-7b}
\end{equation*}
$$

Since $N_{1}(E) N_{2}(E) f_{1}(E) f_{2}(E)$ is not equal to zero and results in $f_{1}(E)=f_{2}(E)$ :

$$
\begin{equation*}
\left[1+e^{\left(E-E_{F 1}\right) / k_{B} T}\right]^{-1}=\left[1+e^{\left(E-E_{F 2}\right) / k_{B} T}\right]^{-1} \tag{2-8}
\end{equation*}
$$

We can now conclude that $E_{F 1}=E_{F 2}$, which indicates that there is no discontinuity in the equilibrium Fermi level across materials in intimate contact. Thus, mathematically $E_{F}$ is a constant with respect to distance in this case. From differential calculus, we know that if $C$ is a constant with respect to a particular variable (say $\beta$ ) then:

Then, in this case we can write that: $\quad \frac{d E_{F}}{d x}=0$

## 2-4-4 Formulation of Built-in Potential

For the $n$-type material, $E_{F}$ is near $E_{c}$, while for the $p$-type material, $E_{F}$ is near $E_{v}$. Therefore, in order for $E_{F}$ to satisfy these two conditions simultaneously while keeping itself invariant, the energy bands must get themselves modified as shown in Figures 2-2(b) and 2-2(c) respectively. Thus:

$$
\begin{equation*}
E_{F n}=E_{F p}=E_{F} \tag{2-10}
\end{equation*}
$$

and,

$$
\begin{equation*}
e V_{d}=E_{c p}-E_{c n} \tag{2-11}
\end{equation*}
$$

At equilibrium, the ratio of Equations (2-3a) to (2-3b) yields:

$$
\begin{equation*}
\frac{n_{n}}{n_{p}}=e^{\left(E_{c p}-E_{c n}\right) k_{B} T}=e^{e V_{d} / k_{B} T} \tag{2-12}
\end{equation*}
$$

Similarly, the ratio of the holes in the two regions is:

$$
\begin{equation*}
\frac{p_{p}}{p_{n}}=e^{e V_{d} / k_{B} T} \tag{2-13}
\end{equation*}
$$

Equations (2-12) and (2-13) are referred to as Boltzmann equations and from them $V_{d}$ can be determined in terms of the electron and hole concentrations:

$$
\begin{equation*}
V_{d}=\frac{k_{B} T}{e} \ln \frac{n_{n}}{n_{p}}=\frac{k_{B} T}{e} \ln \frac{p_{p}}{\bar{p}_{n}} \tag{2-14}
\end{equation*}
$$

From Equations (2-14) and (2-1):

$$
\begin{equation*}
V_{d} \approx \frac{k_{B} T}{e} \ln \frac{N_{a} N_{d}}{n_{i}^{2}} \tag{2-15a}
\end{equation*}
$$

The barrier potential can be further expressed in terms of the conductivities of the $p$-type and $n$-type semiconductors:

$$
\begin{equation*}
V_{d} \approx \frac{k_{B} T}{e} \ln \frac{\sigma_{n} \sigma_{p}}{\mu_{n} \mu_{p} e^{2} n_{i}^{2}} \tag{2-15b}
\end{equation*}
$$

where, $N_{d} e \mu_{n}=\sigma_{n}$ and $N_{a} e \mu_{p}=\sigma_{p}$ have been used.

Assuming only the presence of heavy holes, under the condition of non-degenerate hole concentration, the Einstein relation for holes can be written as:

$$
\begin{equation*}
\frac{\mu_{p}}{D_{p}}=\frac{e}{k_{B} T} \tag{2-16}
\end{equation*}
$$

In order to appreciate the order of magnitude of the diffusion and drift currents in $p-n$ junctions at thermal equilibrium, consider a typical junction where the electron density may drop from $n_{n}=10^{17} \mathrm{~cm}^{-3}$ to $n_{p}=10^{10} \mathrm{~cm}^{-3}$ within a transition region $L=10^{-4} \mathrm{~cm}$. The electron gradient $d n / d x=$ $\left(10^{17}-10^{10}\right) / 10^{-4} \mathrm{~cm}^{-4} \cong 10^{17} / 10^{-4} \mathrm{~cm}^{-4} \approx 10^{21} \mathrm{~cm}^{-4}$, and hence, the electron diffusion current density for germanium is:

$$
\begin{equation*}
J_{n}=-e D_{n} \frac{d n}{d x}=1.6 \times 10^{4} \mathrm{amp} / \mathrm{cm}^{2} \tag{2-17}
\end{equation*}
$$

This very large magnitude of electron current is almost completely cancelled by an equal electron drift current in the opposite direction. A similar state of affairs exists for the holes. Since such an enormous current cannot exist inside the junction, the balance of the built-in field and the concentration gradient prevents the net motion of carriers at equilibrium. For small currents in the non-equilibrium case we should expect that this particular balance would remain essentially the same at the junction.

## Solved Examples

Example 2-1 (a) The resistivities of the two sides of a step-graded germanium diode are $1.5 \Omega-\mathrm{cm}$ ( $p$-side) and $1 \Omega$-cm ( $n$-side). Calculate the height of the potential-energy barrier. (b) Repeat Part (a) for silicon $p-n$ junction.

## Solution:

(a)

$$
\begin{gathered}
\rho=\frac{1}{\sigma}=\frac{1}{N_{A} \mu_{p}}=2 \Omega-\mathrm{cm} \\
N_{A}=\frac{1}{1.5 \times 1.6 \times 10^{-19} \times 1800}=2.31 \times 10^{15} / \mathrm{cm}^{3}
\end{gathered}
$$

Similarly,

$$
N_{D}=\frac{1}{1 \times 1.6 \times 10^{-19} \times 3800}=1.65 \times 10^{15} / \mathrm{cm}^{3}
$$

The height of the potential energy barrier is:

$$
V_{0}=0.026 \times \ln \frac{1.65 \times 10^{15} \times 2.31 \times 10^{15}}{\left(2.5 \times 10^{13}\right)^{2}}=0.226 \mathrm{eV}
$$

(b)

$$
\begin{aligned}
N_{A} & =\frac{1}{1.5 \times 1.6 \times 10^{-19} \times 500}=8.33 \times 10^{15} / \mathrm{cm}^{3} \\
& =\frac{1}{2 \times 1.6 \times 10^{-19} \times 1300}=2.4 \times 10^{15} / \mathrm{cm}^{3}
\end{aligned}
$$

Then,

$$
V_{0}=0.026 \times \ln \frac{2.4 \times 10^{15} \times 8.33 \times 10^{15}}{\left(1.5 \times 10^{10}\right)^{2}}=0.655 \mathrm{eV}
$$

## 2-5 MODES OF THE $p-n$ JUNCTION

There are two modes of switching of a $p-n$ junction diode.
(i) Forward-biased $\boldsymbol{p}-\boldsymbol{n}$ junction: When the positive terminal of a battery is connected to the $p$ type side and the negative terminals to the $n$-type side of a $p-n$ junction, the junction allows a large current to flow through it due to the low resistance level offered by the junction. In this case the junction is said to be forward-biased. A forward-biased $p-n$ junction is shown in the Figure 2-4(a). This shows the decrease of barrier energy by $e V_{a}$ amount.
(ii) Reverse-biased $\boldsymbol{p}-\boldsymbol{n}$ junction: When the terminals of the battery are reversed i.e., when the positive terminal is connected to the $n$-type side and the negative terminal is connected to the $p$-type side, the junction allows a very little current to flow through it due to the high resistance level offered by the junction. Under this condition, the $p-n$ junction is said to be reverse-biased. A reverse-biased $p-n$ junction is shown in Figure 2-4(b).

In this case, the voltage applied to the junction causes the holes in the $p$-type side and the electrons in the $n$-type side to move away from the junction. This increases the width of the depletion region and the barrier energy $(\mathrm{eV})$ gives the amount of increase in the barrier energy where $V_{a}$ is the magnitude of the applied voltage. Due to the increase in the barrier energy, a negligible number of majority carriers will be able to cross the junction and the current will be practically zero. But the minority carriers, which travel down the potential barrier, remain unaffected and give a small current. This current is called the reverse saturation current $\left(I_{S}\right)$. The reverse saturation current increases with the temperature of the diode, but is independent of the applied reverse voltage, the increasing temperature breaks the covalent bonds in the semiconductor.

## 2-5-1 The p-n Junction with External Applied Voltage

If an external voltage $V_{a}$ is applied across the $p-n$ junction, the height of the potential barrier is either increased or diminished as compared to $V_{a}$, depending upon the polarity of the applied voltage.


Figure 2-4 Energy band diagram of a $p-n$ junction under an externally applied voltage: (a) forward-biased condition (b) reverse-biased condition

The energy band distribution, with applied external voltage, is shown in Figure 2-4. For these nonequilibrium conditions, the Fermi level can no longer be identified. In order to describe the behaviour of the $p-n$ junction, quasi-Fermi levels are introduced as shown by the dashed lines in Figure 2-4.

If the polarity of the applied voltage is such that the $p$-type region is made positive with respect to the $n$-type, the height of the potential barrier is reduced, thereby making it relatively easier for the majority carriers, holes or electrons to surmount the barrier. The reduction in the height of the potential barrier is equal to the applied voltage as shown in Figure 2-4(a), under the condition that the voltage drop across the body of the semiconductor and the ohmic drop at the contacts are negligible. Usually the majority carrier densities are much higher than the intrinsic density in both the $n$ - and $p$-types making the injected minority carrier concentration much less than the majority carrier. These injected carriers, which become minority carriers, have a much higher concentration in the neighbourhood of the junction than the minority carriers present far away from the junction. The gradient in the minority-carrier concentration causes a diffusive flow of carriers and hence, an electric current under the forward-biased condition. The magnitude of the current clearly increases with increase in the forward applied voltage.

## 2-5-2 Rectifying Voltage-Current Characteristics of a $p-n$ Junction

If the polarity of the applied voltage is such that the $p$-type region is made negative with respect to the $n$-type, the height of the potential-barrier is increased. Under this reverse-biased condition, it is relatively harder for the majority of the carriers to surmount the potential-barrier. The increase in the potential-barrier height is essentially equal to the applied voltage as shown in Figure 2-4(b).

Because of the increase in barrier height, the increased field helps in the motion of the minority carriers from the $p$-type to the $n$-type, and vice versa. Hence, the minority-carrier concentration near the junction is reduced from its equilibrium value. Since the minority-carrier concentration in this case is much less than the equilibrium value, the increase in applied reverse voltage has a negligible effect on the magnitude of the reverse current.

Under an external applied voltage, the carrier concentrations near the junction corresponding to Equations (2-12) and (2-13) are:

$$
\begin{align*}
& \frac{n_{n}}{n_{p}}=e^{(e k B T)(V d \pm V a)}  \tag{2-18a}\\
& \frac{p_{\mathrm{p}}}{p_{\mathrm{n}}}=e^{(e k B T)(V d \pm V a)} \tag{2-18b}
\end{align*}
$$

where, the sign of the applied voltage is included in Equation (2-18). In other words, the plus and minus signs are for the reverse-biased and the forward-biased conditions, respectively (see Figure 2-4).

From Equations (2-12), (2-13) and (2-18), the injected or extracted minority-carrier concentrations near the junction can be written as:

$$
\begin{align*}
& p_{n}\left(x_{n}\right)=p_{p} e^{-\left(\mathrm{e} / k_{B} T\right)\left(V_{d} \mp V_{a}\right)}=n_{p} e^{(\mathrm{e} / k B T) V_{a}}  \tag{2-19}\\
& n_{p}\left(x_{p}\right)=n_{n} e^{-\left(\mathrm{e} / k_{B} T\right)\left(V_{d} \mp V_{a}\right)}=n_{p} e^{(\mathrm{e} / k B T) V_{a}} \tag{2-20}
\end{align*}
$$

Note that in Equations (2-19) and (2-20), the plus sign is for the forward-biased case where minority carriers are injected. The minus sign is for the reverse-biased case where minority carriers are extracted.


Figure 2-5 Electron and hole carriers at the boundaries of a $p-n$ junction under an externally applied voltage

The concentration of the carriers on the boundaries, for the usual cases, $N_{a} \gg n_{i}$ and under an external applied voltage $V$ is shown in Figure 2-5. It should be noted that in the foregoing discussion it is assumed that the applied voltage is small and well below the breakdown voltage. Figure 2-5 is a key diagram, which can be used in deriving various important equations of diodes and transistors.

## 2-5-3 The Junction Capacitance

In this section, we will examine the calculation of the width of the transition region, the expression for the capacitance across the junction, and the variation of the field in the space-charge region, respectively. For this we will consider two types of idealized junctions, which are approximated closely in practice. These are: (i) the abrupt or step, junction, which results from the alloying technique, and (ii) the graded junction, which results from the crystal-growing technique.

## Abrupt junction

Shown in Figure 2-6(a) is the charge density of a step junction under the assumption that on the $p$ side and the $n$-side of the transition region close to the junction, the charge densities are $e N_{a}$ and $e N_{d}$, respectively. For simplicity, the actual charge density is idealized as shown in Figure 2-6(b).

Assuming one-dimensional geometry, the Poisson equation in the depletion region is given by:

$$
\begin{equation*}
\frac{d^{2} V}{d x^{2}}=-\frac{\rho}{\bar{\varepsilon}}=-\frac{e}{\varepsilon}\left(N_{d}-N_{a}\right) \quad\left(\text { For } x_{p}<x<x_{n}\right) \tag{2-21}
\end{equation*}
$$

where, $\varepsilon$ and $\rho$ are the semiconductor dielectric permittivity and the volume charge density respectively. For $x_{p}<x<0$, Equation (2-21) can be written as:

$$
\begin{align*}
& -\frac{d E_{0}}{d x}=\frac{d^{2} V}{d x^{2}}=\frac{e N_{a}}{\varepsilon}  \tag{2-22}\\
& -E_{0}=\frac{e N_{a}}{\varepsilon} x+C_{1} \tag{2-23}
\end{align*}
$$

The boundary condition restricts us that at $x=-x_{p}, E_{0}=0$ which implies the assumption that the voltage drops in the bulk of the semiconductor are negligible. Thus, substituting $C_{1}=x_{p} e N_{a} / \varepsilon$ in Equation (2-23) yields:

$$
\begin{equation*}
-E_{0}=\frac{d V}{d x}=\frac{e N_{a}}{\varepsilon}\left(x+x_{p}\right) \tag{2-24}
\end{equation*}
$$



Figure 2-6 The profiles of charge density, potential, and electric field in an abrupt junction
which shows that the electric field versus distance is a linear plot with a negative slope. Integrating Equation (2-24) gives:

$$
\begin{equation*}
V=\frac{e N_{a}}{\varepsilon}\left(\frac{x^{2}}{2}+x x_{p}\right)+C_{2} \tag{2-25}
\end{equation*}
$$

We may choose $V=0$ at $x=0$, as shown in Figure 2-6(e), since the choice of the reference for the potential is arbitrary. Hence, Equation (2-25) can be written as:

$$
\begin{equation*}
V=\frac{e N_{a}}{\varepsilon}\left(\frac{x^{2}}{2}+x x_{p}\right) \tag{2-26}
\end{equation*}
$$

At $x=-x_{p}$, Equation (2-26) is: $\quad V \equiv V_{1}=-\frac{e N_{a} x_{p}{ }^{2}}{2 \varepsilon}$

Similarly, at $x=x_{n}: \quad V \equiv V_{2}=-\frac{e N_{d} x_{n}{ }^{2}}{2 \varepsilon}$
Thus, the total voltage $V_{T}$ is given by:

$$
\begin{equation*}
V_{T}=V_{2}-V_{1}=\frac{e}{2 \varepsilon}\left(N_{a} x_{p}^{2}+N_{d} x_{n}^{2}\right) \tag{2-29}
\end{equation*}
$$

It may be noted that in Equation (2-29), $V_{T}$ is the difference between the contact potential and the applied voltage. The total space-charge neutrality requires that the positive and negative chargedensity areas must be equal. Mathematically, we can write:

$$
\begin{equation*}
|Q|=e A N_{d} x_{n}=e A N_{a} x_{p} \tag{2-30}
\end{equation*}
$$

where, $A$ is the junction area. Hence, Equation (2-29) can be expressed in terms of either $x_{n}$ or $x_{p}$ :

$$
\begin{equation*}
V_{T}=\frac{e x_{p}^{2} N_{a}}{2 \varepsilon}\left(1+\frac{N_{a}}{N_{d}}\right)=\frac{e x_{n}^{2} N_{d}}{2 \varepsilon}\left(1+\frac{N_{d}}{N_{a}}\right) \tag{2-31}
\end{equation*}
$$

Thus, from Equation (2-31) the depletion region widths in the $p$-type and $n$-type are:

$$
\begin{align*}
& x_{p}=\left(\frac{2 \varepsilon}{e N_{a}} \frac{V_{T} N_{d}}{N_{d}+N_{a}}\right)^{1 / 2}  \tag{2-32a}\\
& x_{n}=\left(\frac{2 \varepsilon}{e N_{d}} \frac{V_{T} N_{a}}{N_{a}+N_{d}}\right)^{12} \tag{2-32b}
\end{align*}
$$

The maximum field can be determined from Equation (2-24):

$$
\begin{equation*}
E_{0_{\max }}=-\left.\frac{d V}{d x}\right|_{x=0}=-\frac{e N_{a} x_{p}}{\varepsilon}=-\frac{e N_{d} x_{n}}{\varepsilon} \tag{2-33}
\end{equation*}
$$

Since there is a voltage-dependent charge associated with the depletion region, this indicates the existence of a junction capacitance, $C_{j}$. The $C_{j}$ can be mathematically defined as:

$$
\begin{equation*}
C_{j}=\frac{d Q}{d V_{T}}=\frac{d Q}{d x_{n}} \frac{d x_{n}}{d V_{T}}=\frac{d Q}{d x_{p}} \frac{d x_{p}}{d V_{T}} \tag{2-34}
\end{equation*}
$$

But from Equation (2-30):

$$
\begin{equation*}
\frac{d Q}{d x_{p}}=e A N_{a} \tag{2-35}
\end{equation*}
$$

and from Equation (2-32a): $\quad \frac{d x_{p}}{d V_{T}}=\frac{1}{2}\left[\frac{2 \varepsilon N_{d} V_{T}}{e N_{a}\left(N_{d}+N_{a}\right)}\right]^{-1 / 2}\left[\frac{2 \varepsilon N_{d}}{e N_{a}\left(N_{d}+N_{a}\right)}\right]^{-1 / 2}$

Hence, the junction capacitance is given by:

$$
\begin{equation*}
C_{j}=\left(\frac{A e \varepsilon}{2} \times \frac{N_{a} N_{d}}{N_{a}+N_{d}}\right)^{1 / 2} V_{T}^{-1 / 2} \tag{2-37a}
\end{equation*}
$$

where,

$$
\begin{gather*}
C_{j}=K_{1} V_{T}^{-1 / 2}=K_{1}\left(V_{d}-V_{a}\right)^{-1 / 2}  \tag{2-37b}\\
K_{j} \equiv A\left(\frac{e \varepsilon N_{a} N_{d}}{N_{a}+N_{d}}\right)^{1 / 2}
\end{gather*}
$$

where, $V_{a}$ and $V_{d}$ are the applied and diffusion built-in voltages, respectively. Equation (2-37) can also be expressed in the well known form of the familiar parallel-plate capacitance, namely:

$$
\begin{equation*}
C=\frac{\varepsilon A}{\left|x_{p}\right|^{+}\left|x_{n}\right|}=\frac{\varepsilon A}{L} \tag{2-37c}
\end{equation*}
$$

The expression for capacitance derived above is referred to as the transition capacitance-also known as junction or space-charge capacitance-and exists primarily at the reverse-biased junction. It should be noted that physics of transition capacitance of a diode is totally different from that of the well known parallel plate capacitor of basic electrical science despite their striking similarity.

## Solved Examples

Example 2-2 Boron is implanted in an $n$-type $\operatorname{Si}\left(N_{d}=10^{16} \mathrm{~cm}^{-3}\right)$, forming an abrupt $p-n$ junction with the square-cross sectional area $4 \times 10^{-4} \mathrm{~cm}^{2}$ and the accepter concentration $\left(N_{A}\right)$ on the $p$-side is $5 \times 10^{18} \mathrm{~cm}^{-3}$. Find out the width of the depletion zone at 300 K .

## Solution:

The height of the barrier energy is:

$$
\begin{aligned}
V_{0}= & \frac{k_{B} T}{e} \ln \frac{N_{A} N_{d}}{n_{i}^{2}}=0.0259 \ln \frac{5 \times 10^{34}}{2.25 \times 10^{20}} \\
& =0.0259 \ln \left(2.22 \times 10^{14}\right)=0.86 \mathrm{~V}
\end{aligned}
$$

We know that:

$$
\begin{gathered}
W=\left[\frac{2 \varepsilon V_{0}}{e}\left(\frac{1}{N_{A}}+\frac{1}{N_{d}}\right)\right]^{1 / 2} \\
{\left[2 \times \frac{\left(11.8 \times 8.85 \times 10^{-14} \times 0.86\right)}{1.6 \times 10^{-19}}\left(0.2 \times 10^{-18}+10^{-16}\right)\right]^{1 / 2}} \\
=1.059 \times 10^{-5} \mathrm{~cm}
\end{gathered}
$$

Example 2-3 An Si $p-n$ junction is formed from $p$-material doped with $10^{22}$ acceptors $/ \mathrm{m}^{3}$ and $n$ material doped with donors $/ \mathrm{m}^{3}$. Find the thermal voltage and barrier voltage at $30^{\circ} \mathrm{C}$.

## Solution:

$$
\begin{aligned}
& \mathrm{T}=(273+30) \mathrm{K}=303 \mathrm{~K} \\
& \begin{aligned}
V_{T}= & \frac{k_{B} T}{e}=\frac{1.38 \times 10^{-23}(303)}{1.6 \times 10^{-19}} \\
& =26.1 \mathrm{mV} \\
n_{i}^{2} & =\left(1.5 \times 10^{16}\right)^{2} \\
& =2.25 \times 10^{32} \\
V_{0} & =V_{T} \ln \left(\frac{N_{A} N_{D}}{n_{i}^{2}}\right) \\
V_{0} & =V_{T} \ln \left(\frac{10^{22} \times 1.2 \times 10^{21}}{2.25 \times 10^{32}}\right) \\
& =0.635 \mathrm{~V}
\end{aligned}
\end{aligned}
$$

Example 2-4 Calculate the barrier potential for a Si junction at: (a) $70^{\circ} \mathrm{C}$ and (b) $0^{\circ} \mathrm{C}$ if its value at $25^{\circ} \mathrm{C}$ is 0.7 V .

## Solution:

Given: $t_{\mathrm{i}}=25^{\circ} \mathrm{C}, t_{2}=70^{\circ} \mathrm{C}$
(a) We know that $\Delta V=-0.002 \Delta t$

$$
\begin{aligned}
& =-0.002\left(t_{2}-t_{1}\right) \\
& =-0.002(70-25)=-0.69 \mathrm{~V}
\end{aligned}
$$

Thus the barrier potencial at $100^{\circ} \mathrm{C}, V_{B}=0.7+(-0.09)=0.61 \mathrm{~V}$
(b) $\Delta t=(0-25)=-25^{\circ} \mathrm{C}$
$\Delta V=-0.002 \times(-25)=0.05 \mathrm{~V}$
The barrier potential at $0^{\circ} \mathrm{C}, V_{\mathrm{B}}=0.7+0.05=0.75 \mathrm{~V}$

## Graded junction

The idealized net charge density for the graded junction may be expressed as:

$$
\begin{equation*}
p=e a x \quad|x|<x_{p} \tag{2-38}
\end{equation*}
$$

where $a$ is the charge-density gradient in the transition region.
The Poisson equation for this case is:

$$
\begin{equation*}
\frac{d^{2} V}{d x^{2}}=-\frac{e A x}{\varepsilon} \quad|x|<x_{p} \tag{2-39}
\end{equation*}
$$

Integrating Equation (2-39), we obtain:

$$
\begin{equation*}
-E_{0} \equiv \frac{d V}{d x}=-\frac{e a x}{2 \varepsilon}+C_{1} \tag{2-40}
\end{equation*}
$$

From the boundary condition:

$$
\begin{equation*}
E_{0} \equiv-\frac{d V}{d x}=0 \quad \text { at } x=x_{n} \quad \text { and } \quad-x_{p} \tag{2-41}
\end{equation*}
$$

The charge neutrality condition requires that:

$$
\begin{equation*}
x_{n}=x_{p} \tag{2-42}
\end{equation*}
$$

Therefore, we shall use only $x_{p}$ in the following equation. From Equations (2-41) and (2-42), we may write:

$$
\begin{equation*}
\frac{d V}{d x}=\frac{e A}{2 \varepsilon}\left(-x^{2}+x_{p}^{2}\right) \tag{2-43}
\end{equation*}
$$

Integrating Equation (2-43) again, we obtain:

$$
\begin{equation*}
V=\frac{e A}{2 \varepsilon}\left(-\frac{x^{3}}{3}+x x_{p}^{2}\right)+C_{2} \tag{2-44}
\end{equation*}
$$

Arbitrarily choosing $V=0$ at $x=0$, Equation (2-44) becomes:

$$
\begin{equation*}
V=\frac{e A}{2 \varepsilon}\left(-\frac{x^{3}}{3}+x x_{p}^{2}\right) \tag{2-45}
\end{equation*}
$$

The total voltage, $V_{T}$, can be written as:

$$
\begin{align*}
& V_{T}=V\left(x_{p}\right)-V\left(-x_{p}\right)  \tag{2-46a}\\
& V_{T}=\frac{2 e a x_{p}^{3}}{3 \varepsilon} \tag{2-46b}
\end{align*}
$$

From Equation (2-46b) the width of the transition region in the $n$ - or $p$-type is:

$$
\begin{equation*}
\left|x_{n}\right|=\left|x_{p}\right|=\frac{l}{2}=\left(\frac{3 \varepsilon}{2 e a}\right)^{1 / 3} V_{T}^{1 / 3} \tag{2-47}
\end{equation*}
$$

The maximum electric field from Equation (2-43) is:

$$
\begin{equation*}
E_{0 \max }=-\frac{e a x_{p}^{2}}{2 \varepsilon} \tag{2-48}
\end{equation*}
$$

To find the junction capacitance, the charge on either side of the depletion region is given by:

$$
\begin{equation*}
|Q|=\frac{1}{2} e a x_{p}^{2} A \tag{2-49}
\end{equation*}
$$

From Equations (2-48) and (2-49): $\quad|Q|=\frac{1}{2} e a A\left(\frac{3 \varepsilon}{2 a e}\right)^{2 / 3} V_{T}^{2 / 3}$
Therefore:

$$
\begin{align*}
C_{j} & =\frac{d Q}{d V_{T}}=A\left(\frac{e a \varepsilon^{2}}{12}\right)^{1 / 3} V_{T}^{1 / 3}  \tag{2-51a}\\
\text { or, } \quad C_{j} & =K_{2} V_{2}^{1 / 3}=K_{2}\left(V_{d}-V_{a}\right)^{1 / 3} \tag{2-51b}
\end{align*}
$$

where, $\quad K_{2} \equiv A\left(\frac{e a \varepsilon^{2}}{12}\right)^{1 / 3}$
Equation (2-51) can also be expressed as:

$$
\begin{equation*}
C_{j}=\frac{\varepsilon A}{2\left|x_{p}\right|}=\frac{\varepsilon A}{L} \tag{2-51c}
\end{equation*}
$$

From Equations (2-37) and (2-51) it is seen that this junction capacitance is proportional to $V_{T}^{1 / 2}$ in the stepjunction case, while it is proportional to $V_{T}^{1 / 3}$ in the graded-junction case. The voltage-variable-capacitance property of the $p-n$ junction is utilized to maximum advantage in several practical applications. One such application is as a voltage-tuneable element in resonant circuits; other


Figure 2-7 Plot of the junction capacitance as a function of the applied reverse potential for the abrupt $p-n$ junction applications are in the field-effect transistor. The non-linear voltage dependence of the junction capacitance also finds application in harmonic generation and in parametric amplification. A $p-n$ junction designed for use as a voltage-variable-capacitance is called a varactor, or sometimes a varicap. The capacitance versus voltage curve of a typical $p-n$ junction is shown in Figure 2-7.

## Solved Examples

Example 2-5 (a) Prove that for an Si alloy $p-n$ junction (with $N_{A} \ll N_{D}$ ), the depletion layer capacitance in picofarads per square centimetre is given by:

$$
C_{T}=2.9 \times 10^{-4}\left(\frac{N_{A}}{V_{j}}\right)^{1 / 2}
$$

(b) If the resistivity of the $p$-material is $3 \Omega \mathrm{~cm}$, the barrier height $V_{o}$ is 0.4 V , the applied reverse voltage is 4.5 V , and the cross-sectional area is circular of 40 mils diameter, find $\mathrm{C}_{T}$.

Solution:
(a) We have, $C_{T}=\frac{\varepsilon A}{W}$, where $W$ is given by $W=\left(\frac{2 \varepsilon V_{j}}{q N_{A}}\right)^{1 / 2}$
or,

$$
\frac{C_{T}}{A}=\frac{\varepsilon}{W}=\frac{\varepsilon}{\left(2 \varepsilon V_{j}\right)^{1 / 2}}\left(q N_{A}\right)^{1 / 2}=\sqrt{\frac{q \bar{\varepsilon}}{2}} \times \sqrt{\frac{N_{A}}{V_{j}}}
$$

For Si:

$$
\varepsilon=\frac{12}{36 \Pi \times 10^{11}} \mathrm{~F} / \mathrm{cm}
$$

Thus,

$$
\left(\frac{q \varepsilon}{2}\right)^{1 / 2}=\left(\frac{1}{2} \times 1.6 \times 10^{-19} \times \frac{12}{36 \pi} \times 10^{-11}\right)^{1 / 2}=2.9 \times 10^{-16}
$$

$$
\begin{array}{ll}
\text { and, } & C_{T}=2.9 \times 10^{-16}\left(\frac{N_{A}}{V_{j}}\right)^{1 / 2} \mathrm{~F} / \mathrm{cm}^{2} \\
\text { or, } & C_{T}=2.9 \times 10^{-4}\left(\frac{N_{A}}{V_{j}}\right)^{1 / 2} \mathrm{pF} / \mathrm{cm}^{2}
\end{array}
$$

(b) $A=\frac{\pi D^{2}}{4}=\frac{\pi}{4}\left(40 \times 10^{-3} \text { in } \times 2.54 \mathrm{~cm} / \mathrm{in}\right)^{2}=8.11058 \times 10^{-3} \mathrm{~cm}^{2}$

$$
\frac{1}{N_{A} \mu_{p} q}=3
$$

or,

$$
\begin{gathered}
N_{A}=\frac{1}{3.5 \times 1.6 \times 10^{-19} \times 500}=4.18 \times 10^{15} / \mathrm{cm}^{3} \\
W^{2}=\frac{V_{0}-V_{d}}{14.13 \times 10^{10}} \mathrm{~m}^{2}
\end{gathered}
$$

Hence,

$$
C_{T}=\left(2.9 \times 10^{-4}\right) \times\left[\left(\frac{4.18 \times 10^{15}}{4.9}\right)^{1 / 2}\right] \times\left(8.14 \times 10^{-3}\right)=68.94 \mathrm{pF}
$$

Example 2-6 The reverse-biased diodes are frequently employed as electrically controllable variable capacitors. The transition capacitance of an abrupt junction diode is 20 pF at 5 V . Compute the decrease in capacitance for a 1.5 V increase in bias.

## Solution:

We know that for an abrupt junction diode $C_{T}=\frac{\lambda}{V^{1 / 2}}$, where $\lambda=$ constant and $V$ is the reverse-bias voltage across the diode. When, $V=5 \mathrm{~V}, C_{T}=20 \mathrm{pF}$.

$$
\therefore \quad \lambda=20 \times \sqrt{5}
$$

When,

$$
V=6.5 \mathrm{~V}, C_{T}=\frac{20 \times \sqrt{5}}{\sqrt{6.5}}=17.57 \mathrm{pF}
$$

This corresponds to a decrease 2.43 pF .
Example 2-7 Calculate the barrier capacitance of a Ge $p-n$ junction whose area is 1.5 mm by 1.5 mm and whose space-charge thickness is $2 \times 10^{-4} \mathrm{~cm}$. The dielectric constant of Ge is 16 .

## Solution:

We have,

$$
C_{T}=\frac{\varepsilon A}{W} \quad \text { where, for } \mathrm{Ge} \quad \varepsilon=\frac{16}{36 \pi \times 10^{11}} \mathrm{~F} / \mathrm{cm}
$$

$$
\therefore \quad C_{T}=\left(\frac{16}{36 \pi \times 10^{11}}\right) \times\left(\frac{1.5 \times 10^{-1} \times 1.5 \times 10^{-1}}{2 \times 10^{-4}}\right)=159.3 \mathrm{pF}
$$

Example 2-8 The zero-voltage barrier height at a Ge alloy $p-n$ junction is 0.2 V . The concentration of acceptor atoms in the p side is much smaller than the concentration of donor atoms in the n material, and $N_{\mathrm{A}}=2.5 \times 10^{20}$ atoms $/ \mathrm{m}^{3}$. (a) calculate the width of the depletion layer for an applied reverse voltage of 10 V ; (b) calculate the width of the depletion layer for an applied reverse voltage
of 0.1 V ; (c) calculate the width of the depletion layer for an applied forward bias of 0.1 V ; and (d) if the cross-sectional area of the diode is 1 , evaluate the space-charge capacitance corresponding to the values of applied voltage in (a) and (b).

## Solution:

We know that:

$$
V_{0}-V_{d}=\frac{e N_{A}}{2 \varepsilon} W^{2}=\frac{1.6 \times 10^{-19} \times 2.5 \times 10^{20}}{2 \times \frac{16}{36 \pi \times 10^{9}}} W^{2}
$$

Therefore:
or,

$$
\begin{gathered}
V_{0}-V_{d}=\frac{1.6 \times 10^{-19} \times 2.5 \times 10^{20}}{2 \times \frac{16}{36 \pi \times 10^{9}}} W^{2} \\
W^{2}=\frac{V_{0}-V_{d}}{14.13 \times 10^{10}} \mathrm{~m}^{2}
\end{gathered}
$$

Hence,
(a) $W=\left(\frac{10.2}{14.13} \times 10^{-10}\right)^{1 / 2}=\left(8.5 \times 10^{-6}\right) \mathrm{m}=8.5 \mu \mathrm{~m}$
(b) $\quad W=\left(\frac{0.3}{14.13} \times 10^{-10}\right)^{1 / 2}=\left(1.45 \times 10^{-6}\right) \mathrm{m}=1.45 \mu \mathrm{~m}$
(c) $W=\left(\frac{0.1}{14.15} \times 10^{-10}\right)^{1 / 2}=\left(0.84 \times 10^{-6}\right) \mathrm{m}=0.84 \mu \mathrm{~m}$
(d) We know that: $C_{T}=\frac{\varepsilon A}{W}$

For (a):

$$
C_{T}=\frac{\varepsilon A}{W}=\frac{16 \times 1 \times 10^{-6}}{36 \pi \times 10^{9} \times 8.5 \times 10^{-6}}=16.65 \mathrm{pF}
$$

For (b):

$$
C_{T}=\frac{\varepsilon A}{W}=\frac{0.1415 \times 10^{-9}}{1.45}=97.6 \mathrm{pF}
$$

## 2-5-4 The Varactor Diode

"Varactor" is actually an abbreviated form of "variable reactor". One property of a $p-n$ junction is that the width of the junction depletion region (and hence the depletion capacitance) is a function of the applied voltage, which is utilized in this application, as shown in Figure 2-8. In general, let us consider a $p^{+} n$ junction where the doping profile in the $n$-region is given by:

$$
N_{D}(x)=N_{D 0}\left(\frac{x}{x_{0}}\right)^{n}
$$



Figure 2-8 The schematic diagram of the varactor diode
where, $N_{D 0}$ and $n$ are the constants for a particular doping profile, and $x$ is the distance from the $p-n$ junction in the $n$-region. Then, following the usual procedure of integrating Poisson equation twice using appropriate boundary conditions, the depletion region width is obtained as a function of the applied reverse bias $V_{T}$ as:

$$
L \alpha\left(V_{N}+V_{T}\right)^{\frac{1}{(n+2)}}
$$

Neglecting $V_{b i}$ when a large reverse bias is applied, the depletion capacitance is given by:

$$
C_{j}=\frac{A \varepsilon_{5}}{L} \alpha\left(V_{T}\right)^{\frac{-1}{(n+2)}}
$$

For an abrupt junction $n=0$, and therefore, the depletion capacitance $C_{J}$ is proportional to $V_{T}^{-1 / 2}$. Similarly, it can be shown that for a linearly graded junction $(n=1), \mathrm{C}_{J}$ will be proportional to $V_{T}^{-1 / 3}$. These two cases have individually been proved in the previous section. The voltage sensitivity $d C_{j}$ $/ d v$ is found to be greater for an abrupt junction.

Using a hyper-abrupt junction, where the doping profile is tailored specifically to obtain a value of $n<0$, can further enhance the sensitivity. A special case is seen for $n=-3 / 2$ as shown in Figure $2-9$. In this case, the depletion capacitance variation can be expressed as $C_{J} \propto V_{T}^{-2}$. If this varactor is used with an inductance $L$ in a resonant circuit, the resonant frequency of the circuit is given by:

$$
f_{r}=\frac{1}{2 \pi \sqrt{L C}} \alpha V_{T}
$$

In other words, the resonant frequency of the circuit can be varied linearly by changing the applied reverse voltage. This property is widely used for tuning in the radio TV receivers.

It may be noted at this point that there is another type of capacitance, known as the diffusion or storage capacitance, which can be briefly explained. For a forward bias, a capacitance, which is much larger than the transition capacitance $C_{T}$, comes into play. The origin of this larger capacitance lies in


Figure 2-9 The doping profiles used in varactor diode
the injected charge stored near the junction outside the transition region. It is convenient to introduce an incremental capacitance, defined as the rate of change of the injected charge with voltage called the diffusion or storage capacitance $C_{D}$ as mentioned earlier. Thus, we can write:

$$
C_{D}=\frac{d Q}{d V}=\tau \frac{d I}{d V}, \quad \text { where, } \tau \text { is the lifetime of minority current. }
$$

We know that:

$$
I=I_{s}\left(e^{\frac{e V}{\eta k_{B} T}}-1\right)
$$

So,

$$
\frac{d I}{d V}=\frac{I_{s}\left(e^{\frac{V}{\eta V_{T}}}\right)}{\eta V_{T}}
$$

Replacing $I_{s}\left(e^{\frac{V}{\eta_{T}}}\right)$ by $\left(I+I_{s}\right)$ we get: $\quad \frac{d I}{d V}=\frac{I+I_{s}}{\eta V_{T}}$
Since,

$$
I \gg I_{s}
$$

Therefore,

$$
\frac{d I}{d V}=\frac{I}{\eta V_{T}}
$$

Substituting this value of $d I / d V$ in the basic equation of $C_{D}$ we get:

$$
C_{D}=\frac{\tau I}{\eta V_{T}}
$$

Therefore, the diffusion capacitance is proportional to the current $I$. We assume that the diode current $I$ is generated due to holes only. Contradicting this assumption will gives us the diffusion capacitance $C_{D}(p)$ due to holes only and a similar expression can be obtained for $C_{D}(n)$ due to electrons. The total diffusion capacitance can then be obtained as the sum of $C_{D}(p)+C_{D}(n)$.

## 2-6 DERIVATION OF THE I-V CHARACTERISTICS OF A p-n JUNCTION DIODE

Let us consider the fact that the drift component of the current is negligible.

$$
\begin{equation*}
D_{p} \frac{d^{2} p}{d x^{2}}=\frac{p-p_{n}}{\tau_{p}} \tag{2-52}
\end{equation*}
$$

Equation (2-52) can be written as: $\quad \frac{d^{2}\left(p-p_{n}\right)}{d x^{2}}=\frac{p-p_{n}}{L_{p}^{2}}$
where, $L_{p}=\sqrt{D_{p} \tau_{p}}$ is the diffusion length and $p_{n}$ is the equilibrium density of holes in the $n$-region far away from the junction.

The solution of the ordinary differential Equation (2-53) is:

$$
\begin{equation*}
p-p_{n}=C_{1} \exp \left(-\frac{x}{L_{p}}\right)+C_{2} \exp \left(\frac{x}{L_{p}}\right) \tag{2-54}
\end{equation*}
$$

where, $C_{1}$ and $C_{2}$ are two arbitrary constants of integration to be determined from the boundary conditions (see Figure 2-5). The boundary conditions in this case are:

$$
\begin{array}{ll}
x=x_{n}: & p=p_{n} \exp \left(\frac{e V}{k_{B} T}\right) \\
x=\infty: & p=p_{n} \tag{2-56}
\end{array}
$$

By using Equations (2-54) and (2-56) we get $C_{2}=0$
Again by using Equations (2-54) and (2-55), together with the condition $C_{2}=0$, we get the expression of $C_{1}$ as:

$$
\begin{equation*}
C_{1}=p_{n}\left[\exp \left(\frac{e V}{k_{B} T}\right)-1\right] \exp \left(\frac{x_{n}}{L_{p}}\right) \tag{2-57b}
\end{equation*}
$$

Substituting the values of constants $C_{1}$ and $C_{2}$ in Equation (2-54) we get:

$$
\begin{equation*}
p-p_{n}=p_{n}\left[\exp \left(\frac{e V}{k_{B} T}\right)-1\right] \exp \left(\frac{x_{n}-x}{L_{p}}\right) \tag{2-58a}
\end{equation*}
$$

The current density of holes in $n$-type semiconductors along the $x$ direction by diffusion is given by:

$$
\begin{equation*}
J_{p}(x)=-e D_{p} \frac{d p}{d x} \tag{2-58b}
\end{equation*}
$$

Using Equations (2-58a) and (2.58b) we get:

$$
\begin{equation*}
J_{p}(x)=+e \frac{D_{p} p_{n}}{L_{p}}\left[\exp \left(\frac{e V}{k_{B} T}\right)-1\right] \exp \left(\frac{x_{n}-x}{L_{p}}\right), \quad x \geq x_{n} \tag{2-59}
\end{equation*}
$$

Equation (2-59) shows that the minority-carrier flow (hole current) is decreasing exponentially with distance from the junction in the $n$-region. Since the total diode current must be constant, under steady-state condition i.e., the equilibrium condition, the majority carrier flow (electron current) is increasing exponentially with distance from the junction.

The hole current density at the edge of the transition region i.e, at $x=x_{n}$, from Equation (2-59) is given as:

$$
\begin{equation*}
J_{p}\left(x_{n}\right)=+e \frac{D_{p} p_{n}}{L_{p}}\left[\exp \left(\frac{e V}{k_{B} T}\right)-1\right] \tag{2-60}
\end{equation*}
$$

In the same manner, from Equation (1-119), and with the boundary conditions as shown in Figure $2-5$, we can have the following equation for electrons in the $p$-type:

$$
\begin{equation*}
J_{n}(x)=+e \frac{D_{n} n_{p}}{L_{n}}\left[\exp \left(\frac{e V}{k_{B} T}\right)-1\right] \exp \left(\frac{x+x_{p}}{L_{n}}\right), \quad x \leq-x_{p} \tag{2-61}
\end{equation*}
$$

The hole current density at the edge of the transition region, i.e, $x=-x_{p}$ can be written from Equation (2-61) as:

$$
\begin{equation*}
J_{n}\left(-x_{p}\right)=+e \frac{D_{n} n_{p}}{L_{n}}\left[\exp \left(\frac{e V}{k_{B} T}\right)-1\right] \tag{2-62}
\end{equation*}
$$

Since the transition region width $L$ is almost always much smaller than the diffusion length, we can assume that the recombination in the transition region can be neglected. This assumption has been found to be valid in most cases. Thus, we can write:

$$
\begin{equation*}
J_{n}=\left(-x_{p}\right)=J_{n}\left(x_{n}\right) \quad \text { and } \quad J_{p}\left(x_{n}\right)=J_{p}\left(-x_{p}\right) \tag{2-63}
\end{equation*}
$$

The total diode-current density is given by:

$$
\begin{align*}
& J=J_{n}\left(x_{n}\right)+J_{p}\left(x_{n}\right)=J_{n}\left(-x_{p}\right)+J_{p}\left(x_{n}\right)  \tag{2-64}\\
& J=e\left(\frac{D_{p} p_{n}}{L_{p}}+\frac{D_{n} n_{p}}{L_{n}}\right)\left[\exp \left(\frac{e V}{k_{B} T}\right)-1\right] \tag{2-65}
\end{align*}
$$

The total direct current of the diode, with a cross-sectional junction area $A$, is:

$$
\begin{gather*}
I=A J_{s}\left[\exp \left(\frac{e V}{k_{B} T}\right)-1\right]=I_{s}\left[\exp \left(\frac{e V}{k_{B} T}\right)-1\right]  \tag{2-66}\\
I_{s} \equiv A J_{s} \equiv A e\left(\frac{D_{p} p_{n}}{L_{p}}+\frac{D_{n} n_{p}}{L_{n}}\right) \tag{2-67}
\end{gather*}
$$

where,
Equation (2-66) is the dc equation of an ideal $p-n$ junction diode. The plot of the voltage-current characteristics of the diode, for forward-bias and reverse-bias, is shown in Figure 2-10.

It should be noted that because of the higher concentration of holes in the p-region the hole current is much larger than the electron current.


Figure 2-10 Actual and theoretical I-V characteristics of a typical semiconductor diode

## Solved Examples

## Example 2-9

(a) Prove that the reverse saturation current in a $p-n$ diode can be written as:

$$
I_{0}=A e\left(\frac{D_{p}}{L_{p} N_{D}}+\frac{D_{n}}{L_{n} N_{A}}\right) n_{i}^{2}
$$

(b) Starting with the expression for $I_{0}$ found in part (a), verify that the reverse saturation current is given by:

$$
I_{0}=A V_{T}\left(\frac{b \sigma_{i}^{2}}{(1+b)^{2}}\right)\left(\frac{1}{L_{P} \sigma_{N}}+\frac{1}{L_{N} \sigma_{P}}\right)
$$

Here, $\quad b=\frac{\mu_{n}}{\mu_{p}} \quad$ and $\quad \sigma_{i}=n_{i} e\left(\mu_{n}+\mu_{p}\right)$

## Solution:

(a) From Equation (2-67), we can write that the reverse saturation current $I_{0}$ is given by:

$$
I_{0}=A e\left(\frac{D_{p} p_{n}}{L_{p}}+\frac{D_{n} n_{p}}{L_{n}}\right)
$$

We know that:

$$
p_{n}=\frac{n_{i}^{2}}{N_{D}} \quad \text { and } \quad n_{p}=\frac{n_{i}^{2}}{N_{A}}
$$

Substituting these two in the equation for saturation current we get:

$$
\begin{equation*}
I_{0}=A e\left(\frac{D_{p}}{L_{p} N_{D}}+\frac{D_{n}}{L_{n} N_{A}}\right) n_{i}^{2} \tag{1}
\end{equation*}
$$

(b) We know from the Einstein relation under the condition of carrier non-degeneracy that:

$$
D_{n}=\mu_{n} V_{T}, \quad V_{T}=\frac{k_{B} T}{e} \quad \text { and } \quad D_{p}=\mu_{p} V_{T}
$$

Substituting the values of $D_{n}$ and $\mu_{n}$ in the equation for saturation current, we get

$$
\begin{aligned}
I_{0}= & A e V_{T}\left(\frac{\mu_{p}}{L_{p} N_{D}}+\frac{\mu_{n}}{L_{n} N_{A}}\right) n_{i}^{2} \\
& =A e V_{T} \mu_{n} \mu_{p}\left(\frac{1}{L_{p} N_{D} \mu_{n}}+\frac{1}{L_{n} N_{A} \mu_{p}}\right) n_{i}^{2} \\
& =A e^{2} V_{T} \mu_{n} \mu_{p}\left(\frac{1}{e L_{p} N_{D} \mu_{n}}+\frac{1}{e L_{n} N_{A} \mu_{p}}\right) n_{i}^{2} \\
& =A e^{2} V_{T} \frac{\mu_{n} \mu_{p}}{\left(\mu_{n}+\mu_{p}\right)^{2}}\left(\frac{1}{\sigma_{p} L_{n}}+\frac{1}{\sigma_{n} L_{p}}\right) n_{i}^{2}\left(\mu_{n}+\mu_{p}\right)^{2} \\
& =A e^{2} V_{T} \frac{\left(\mu_{n} / \mu_{p}\right)}{1+\left(\frac{\mu_{n}}{\mu_{p}}\right)^{2}}\left(\frac{1}{\sigma_{p} L_{n}}+\frac{1}{\sigma_{n} L_{p}}\right) n_{i}^{2}\left(\mu_{n}+\mu_{p}\right)^{2}
\end{aligned}
$$

Since, $\sigma_{i}=n_{i} e\left(\mu_{n} \mu_{p}\right)$ and by the question $b=\mu_{n} / \mu_{p}$, we can write that:

$$
I_{0}=A V_{T}\left(\frac{b \sigma_{i}^{2}}{(1+b)^{2}}\right)\left(\frac{1}{L_{p} \sigma_{n}}+\frac{1}{L_{N} \sigma_{p}}\right)
$$

Example 2-10 Find the reverse saturation point of current for a Si $p-n$ junction diode at a room temperature of $27^{\circ} \mathrm{C}$. The cross sectional area is $1.5 \mathrm{~mm}^{2}, \sigma_{n}=0.1(\mathrm{ohm} \mathrm{cm})^{-1}, \sigma_{p}=3.0(\mathrm{ohm} \mathrm{cm})^{-1}$ and $L_{n}=L_{p}=0.15 \mathrm{~cm}$. Use the other physical data if required.

## Solution:

We know that:

$$
\begin{gathered}
b=\frac{\mu_{n}}{\mu_{p}}=\frac{3800}{1800}=2.11, \quad A=1.5 \times 10^{-6} \mathrm{~m}^{2}, \quad V_{T}=0.026 \mathrm{eV} \\
L_{p} \sigma_{n}=0.15 \times 0.1=0.015 \Omega^{-1}, \quad L_{n} \sigma_{p}=0.15 \times 3.0=0.45 \Omega^{-1}
\end{gathered}
$$

We know that:

$$
\sigma_{i}=\left(\mu_{n}+\mu_{p}\right) n_{i} e=(3800+1800) \times 2.5 \times 10^{15} \times 1.6 \times 10^{-19}=2.24(\Omega \mathrm{~m})^{-1}
$$

In this case:

$$
L_{n} \sigma_{p}=L_{p} \sigma_{n}=3 \times 10^{-4}
$$

Therefore, using the results of Equation (2-67), we get:

$$
\begin{aligned}
& I_{0}=\frac{1.5 \times 10^{-16} \mathrm{~m}^{2} \times 0.026 \mathrm{~V} \times 2.11 \times(2.24)^{2}}{(3.11)^{2}(\Omega \mathrm{~m})^{2}}\left(\frac{1}{0.45}+\frac{1}{0.015}\right) \Omega \\
&=2.94 \mu \mathrm{~A}
\end{aligned}
$$

Example 2-11 Consider a $p-n$ diode operating under low-level injection. Assuming that the minority current is due entirely to diffusion show that the electric field in the $n$-side is given by:

$$
\varepsilon(x)=\frac{I_{T}+\left(D_{n} / D_{p}-1\right) I_{p n}(x)}{e n_{n} \mu_{n} A}
$$

where, $I_{p n}(x)$ is the minority diffusion current in the $n$-side of the diode, $I_{T}$ is the total current which is constant and independent of $x$ and the other notations have the usual meanings.

## Solution:

The minority (hole) diffusion current in the $n$-side of the diode is $I_{p n}(x)=-A e D_{p} d p / d x$. The majority (electron) current in the $n$-side consists of two parts: majority diffusion current and majority drift current. So total majority (electron) current is:

$$
I_{\text {majority }}=\operatorname{Aen}_{n} \mu n \xi(x)-\frac{D_{n}}{D_{p}} I_{p n}(x) \quad \text { where } \xi(x) \text { is the electric field. }
$$

Therefore, since we neglect the minority drift current, the total current $I_{T}$ which is constant and independent of $x$ can be written as

Solving for $\xi(x)$ we find:

$$
\begin{gathered}
I_{T}=\operatorname{Aen}_{n} \mu_{n} \xi(x)-\frac{D_{n}}{D_{p}} I_{p n}(x)+I_{p n}(x) \\
\xi(x)=\frac{I_{\mathrm{T}}+\left(\frac{D_{n}}{D_{p}}-1\right) I_{p n}(x)}{\operatorname{Aen}_{n} \mu_{n}}
\end{gathered}
$$

Example 2-12 Using the result $I_{0}=A V_{T} \frac{b \sigma_{i}^{2}}{(1+\mathrm{b})^{2}}\left(\frac{1}{L_{p} \sigma_{n}}+\frac{1}{L_{n} \sigma_{p}}\right)$, find the reverse saturation current for a $p$-Si $p-n$ junction diode at room temperature, 300 K . Assume that the cross-sectional area $A=5.0 \mathrm{~mm}^{2}, L_{n}=L_{p}=0.01 \mathrm{~cm}$ and $\sigma_{n}=\sigma_{p}=0.01 \Omega \mathrm{~cm}^{-1}$.

## Solution:

$$
\begin{gathered}
A=5 \times 10^{-6} \mathrm{~m}^{2} \quad \text { and } \quad b=\frac{1300}{500}=2.6 \\
L_{p} \sigma_{n}=10^{-2} \times 10^{-2}(\Omega)^{-1}=L_{n} \sigma_{p} \\
\sigma_{i}=1.5 \times 10^{10}(1300+500)\left(1.6 \times 10^{-19}\right)=4.32 \times 10^{-6}(\Omega-\mathrm{cm})^{-1}
\end{gathered}
$$

Then,

$$
\begin{aligned}
I_{0} & =5 \times 10^{-2} \mathrm{~cm}^{2} \times 0.026 \times \frac{2.6}{(3.6)^{2}} \times \frac{\left(4.32 \times 10^{-6}\right)^{2}}{(\Omega-\mathrm{cm})^{2}} \times\left(2 \times 10^{4}\right) \Omega \\
& =97.25 \mathrm{pA}
\end{aligned}
$$

Example 2-13 Find the ratio of the reverse saturation current in Ge to that in Si , using the result:

$$
I_{0}=A V_{T} \frac{b \sigma_{i}^{2}}{(1+b)^{2}}\left(\frac{1}{L_{p} \sigma_{n}}+\frac{1}{L_{n} \sigma_{p}}\right)
$$

Assume $L_{n}=L_{p}=0.1 \mathrm{~cm}$ and $\sigma_{n}=\sigma_{p}=1.0(\Omega \mathrm{~cm})^{-1}$ for Ge , whereas the corresponding values are 0.01 cm and $0.01(\Omega \mathrm{~cm})^{-1}$ for Si .

## Solution:

Let:

$$
\begin{gathered}
Y=\frac{I_{0}}{A V_{T}}=\frac{b \sigma_{i}^{2}}{(1+b)^{2}}\left(\frac{1}{L_{p} \sigma_{n}}+\frac{1}{L_{n} \sigma_{p}}\right) \\
b=\frac{\mu_{n}}{\mu_{p}}=\frac{1300}{500}=2.6
\end{gathered}
$$

$$
\sigma_{i}=1.5 \times 10^{10}(1300+500)\left(1.6 \times 10^{-19}\right)=4.32 \times 10^{-6}(\Omega-\mathrm{cm})^{-1}
$$

Then,

$$
Y_{\mathrm{Si}}=\frac{2.6 \times\left(4.32 \times 10^{-6}\right)^{2}}{(3.6)^{2}}\left(2 \times 10^{4}\right)=7.49 \times 10^{-8}\left(\Omega-\mathrm{cm}^{2}\right)^{-1}
$$

For Ge:

$$
b=\frac{\mu_{n}}{\mu_{p}}=\frac{3800}{1800}=2.11
$$

$$
\sigma_{i}=2.5 \times 10^{13}(3800+1800)\left(1.6 \times 10^{-19}\right)=2.24 \times 10^{-2}(\Omega-\mathrm{cm})^{-1}
$$

Then,

$$
Y_{\mathrm{Ge}}=\frac{2.11 \times\left(2.24 \times 10^{-2}\right)^{2}}{(3.11)^{2}}\left(2 \times 10^{2}\right)=2.189 \times 10^{-2}\left(\Omega-\mathrm{cm}^{2}\right)^{-1}
$$

Therefore,

$$
\frac{Y_{\mathrm{Ge}}}{Y_{\mathrm{Si}}}=\frac{2.189 \times 10^{-2}}{7.49 \times 10^{-8}}=0.29 \times 10
$$

## Key Points

(i) Equation (2-66) has been derived under the following assumptions:

- Only one-dimensional flow of current has been assumed
- The recombination mechanism has been neglected in the transition region
- The injected minority carrier density is much less than the normally present majority carrier density
- The majority carrier density is much higher than the intrinsic carrier density of both $p$ - and $n$-type semiconductor
- Both $p$ - and $n$-type semiconductors are essentially non-degenerate
- The carrier dispersion relations of both types of semiconductors are strictly parabolic
(ii) Figure 2-10 gives the plot of the current $I$ versus the voltage $V$, as described by Equation (2-69). This plot is termed the current-voltage characteristic or the volt-ampere characteristic of the $p-n$ junction diode. The practical I-V characteristics of a $p-n$ junction diode, as obtained by measurements, will deviate from the ideal model characteristics Equation (2-66) in the manner shown in Figure 2-10. The deviation in the forward region is due to the voltage drops across the semiconductor bulk. The applied voltage will cause less current than predicted by the theoretical model since the drops were neglected.

It should be noted that in the derivation of the diode equation it was assumed that the forward applied voltage was small, so that the injected minority-carriers were much less than the majority-carrier concentration normally present in the extrinsic semiconductor. In other words, we have assumed low-level injection. If the low-level-injection condition is violated, the electric field outside the depletion region cannot be neglected and the differential equation to be solved is no longer a linear differential equation. Fortunately, in many transistor applications the applied forward voltage is small, so that the low-levelinjection assumption is valid. In the presence of non-ideality, Equation (2-66) assumes the form:

$$
\begin{equation*}
I=I_{s}\left(e^{\frac{e V}{\eta K_{B}^{T}}}-1\right) \tag{2-68}
\end{equation*}
$$

where, $\eta$ is a dimensionless number and is known as non-ideality factor, which depends on the band structure of the material. When $V$ is positive, the junction is forward-biased, and when $V$ is negative, the junction is reverse-biased. It has been observed from Figure 2-9 that at a particular value of the reverse voltage $\left(V_{B}\right)$, the reverse current increases suddenly. When the forward bias $V$ is less than a value $V_{B}$, the current is very small. As $V$ exceeds $V_{B}$, the current increases very sharply. The voltage $V_{B}$ is known as the break point, offset, threshold or cutin voltage of the diode. $V_{B}=0.2 \mathrm{~V}$ for Ge diodes and $V_{B}=0.6 \mathrm{~V}$ for Si diodes.

## Solved Examples

Example 2-14 The current flowing in a certain $p-n$ junction diode at room temperature is $9 \times 10^{-7}$ A, when the large reverse voltage is applied. Calculate the current flowing, when 0.1 V forward bias is applied.

## Solution:

Given:

$$
I_{0}=9 \times 10^{-7} \mathrm{~A}, V_{\mathrm{F}}=0.1 \mathrm{~V}
$$

Current flowing through the diode under forward-bias is given by:

$$
\begin{aligned}
I & =I_{0}\left(e^{V / \eta V_{T}}-1\right) \\
& =I_{0}\left(e^{40 V_{F}}-1\right) \\
& =9 \times 10^{-7}\left(e^{40 \times 0.1}-1\right)=9 \times 10^{-7}\left(e^{4}-1\right) \\
& =48.15 \mu \mathrm{~A}
\end{aligned}
$$

Example 2-15 The saturation current density of a $p-n$ junction $G e$ diode is $500 \mathrm{mAm}^{-2}$ at 350 K . Find the voltage that would have to be applied across the junction to cause a forward current density of $10^{5} \mathrm{Am}^{-2}$ to flow.

## Solution:

Given:

$$
J_{0}=500 \mathrm{~mA} / \mathrm{m}^{2}, \quad T=350 \mathrm{~K}, \quad J=10^{5} \mathrm{Am}^{-2}
$$

We know that:

$$
I=I_{0}\left(e^{e V \eta K T}-1\right)
$$

Dividing by the area of the diode, we have an expression for current density:

$$
\begin{aligned}
& J=J_{0}\left(e^{e V / \eta K T}-1\right) \\
& \text { or, } \quad e^{e V / \eta K T}=\frac{J}{J_{0}}+1=\frac{10^{5}}{500 \times 10^{-3}}+1=2 \times 10^{5} \\
& \therefore \quad \frac{e V}{\eta K T}=\log _{e}\left(2 \times 10^{5}\right)=2.303 \log _{10}\left(2 \times 10^{5}\right) \\
& = \\
& \\
& \quad 12.20827 \\
& V=\frac{12.208 \times \eta K T}{e} \\
& V=\frac{12.208 \times 1.38 \times 10^{-23} \times 350}{1.6 \times 10^{-19}}=0.3685 \mathrm{~V}
\end{aligned}
$$

Example 2-16 A Si diode has a saturation current of 0.15 pA at $20^{\circ} \mathrm{C}$. Find it's current when it is forward-biased by 0.55 V . Find the current in the same diode when the temperature rises to $100^{\circ} \mathrm{C}$.

## Solution:

At $T=20^{\circ} \mathrm{C}$ :

$$
\begin{aligned}
V_{T} & =\frac{k_{B} T}{e}=\frac{1.38 \times 10^{-23}(273+20)}{1.6 \times 10^{-19}} \\
& =0.02527 \mathrm{~V}
\end{aligned}
$$

Assuming $\eta=1$ :

$$
\begin{array}{rl}
I & =I_{s}\left(e^{V / \eta V T}-1\right) \\
= & 1.5 \times 10^{-13}\left(e^{0.55 / 0.02527}-1\right) \\
= & 0.4245 \mathrm{~mA} \\
V_{T}=\frac{k_{B} T}{e}=\frac{1.38 \times 10^{-23}(273+100)}{1.6 \times 10^{-19}} \\
=0 & 0.03217 \mathrm{~V}
\end{array}
$$

Now $100-20=80$ and $80 / 10=8$.
Therefore, $I_{s}$ doubles 8 times, i.e., increased by a factor $2^{8}=256$.
So at $100^{\circ} \mathrm{C}$ :

$$
\begin{aligned}
I_{s} & =1.5 \times 256 \times 10^{-13} \mathrm{~A} \\
I & =1.5 \times 256 \times 10^{-13}\left(e^{0.55 / 0.032}-1\right) \\
I & =0.0011 \mathrm{~A}
\end{aligned}
$$

Example 2-17 The saturation currents of the two diodes are 2 and $4 \mu \mathrm{~A}$. The breakdown voltages of the diodes are the same and are equal to 100 V . Calculate the current and voltage for each diode if $V=90 \mathrm{~V}$ and $V=110 \mathrm{~V}$.

## Solution:

$$
I_{01}=2 \mu \mathrm{~A} \quad \text { and } \quad I_{02}=4 \mu \mathrm{~A}, \quad V_{z 1}=V_{z 2} 100 \mathrm{~V}
$$

We have, $I=I_{0}\left(e^{V / \eta V_{T}}-1\right)$. Therefore, $V=\eta V_{T} \operatorname{In}\left(1+\frac{I}{I_{0}}\right)$. We assume that the diodes are Si diodes so
that $\eta=2$.
When $V=90 \mathrm{~V}$ : None of the diodes will break down and $I$ is determined by the diode with the smallest $I_{0}$, i.e., $D_{1}$. Thus, $I=1 \mu \mathrm{~A}$ and for $D_{2}, I=-1 \mu \mathrm{~A}$.

$$
\therefore \quad V_{2}=\eta V_{T} \ln \left(1+\frac{I}{I_{0}}\right)=2 \times 0.026 \ln \left(1-\frac{2}{4}\right)=-36 \mathrm{mV}
$$

and,

$$
V_{1}=-89.964 \mathrm{~V}
$$

When $V=110 \mathrm{~V}$ : As the applied voltage $V$ is increased to $110 \mathrm{~V}, D_{1}$ will break down, while $D_{2}$ will be reverse-biased. Thus, $I=I_{02}=2 \mu \mathrm{~A}, V_{1}=-100 \mathrm{~V}$ and $V_{2}=-10 \mathrm{~V}$

Example 2-18 (a) For what voltage will the reverse current in a $p-n$ junction Ge diode reach $90 \%$ of its saturation value at room temperature?
(b) What is the ratio of the current for a forward bias of 0.05 V to the current for the same magnitude of reverse-bias?
(c) If the reverse saturation current is $15 \mu \mathrm{~A}$, calculate the forward currents for voltages of 0.1 V , 0.2 V , and 0.3 V , respectively.

## Solution:

(a) We have, $V_{T}=\frac{T}{11,600}=0.026 \mathrm{~V}$ at room temperature.

Using the formula, $I=I_{0}\left(e^{V V T}-1\right)$ we have:

$$
\begin{array}{lc} 
& -0.9 I_{0}=I_{0}\left(e^{V / 0.026}-1\right) \\
\text { or, } & e^{V 0.026}=0.1 \\
\text { or, } & V=(0.026)(-2.3)=-0.060 \mathrm{~V}
\end{array}
$$

(b) $\frac{e^{50 / 26}-1}{e^{-50 / 26}-1}=\frac{e^{1.92}-1}{e^{-1.92}-1}=\frac{6.82-1}{0.147-1}=-6.83$

For $V=0.1$ :

$$
\begin{aligned}
& I=15\left(e^{100 / 26}-1\right)=15\left(e^{3.84}-1\right)=682.5 \mu \mathrm{~A}=0.682 \mathrm{~mA} \\
& \quad V=0.2, I=15\left(e^{200 / 26}-1\right)=15\left(e^{7.68}-1\right)=32550 \mu \mathrm{~A}=32.55 \mathrm{~mA} \\
& V=0.3, I=15\left(e^{300 / 26}-1\right)=15\left(e^{11.52}-1\right)=1.515 \times 10^{6} \mu \mathrm{~A}=1.515 \mathrm{~A}
\end{aligned}
$$

Example 2-19 (a) Calculate the anticipated factor by which the reverse saturation current of a Ge diode is multiplied when the temperature is increased from 25 to $70^{\circ} \mathrm{C}$.
(b) Repeat part (a) for an Si diode in the range $25-150^{\circ} \mathrm{C}$.

## Solution:

(a) $I_{0}\left(70^{\circ} \mathrm{C}\right)=I_{0}\left(25^{\circ} \mathrm{C}\right) \times 2^{(70-50) / 10}=I_{0}\left(25^{\circ} \mathrm{C}\right) \times 2^{4.5}=45 I_{0}\left(25^{\circ} \mathrm{C}\right)$
(b) $I_{0}\left(150^{\circ} \mathrm{C}\right)=I_{0}\left(25^{\circ} \mathrm{C}\right) \times 2^{12.5}=5700 I_{0}\left(25^{\circ} \mathrm{C}\right)$

Example 2-20 It is predicted that, for Ge , the reverse saturation current should increase by $0.15^{\circ} \mathrm{C}^{-1}$. It is found experimentally in a particular diode that at a reverse voltage of 10 V , the reverse current is $5 \mu \mathrm{~A}$ and the temperature dependence is only $0.07^{\circ} \mathrm{C}^{-1}$. What is the leakage resistance shunting the diode?

## Solution:

The diode is connected in parallel with a resistance $R$ and the parallel combination is placed in series with the diode with a series with a reverse voltage 10 V . Let the current through diode be $I_{0}$ and the current through $R$ be $I_{R}$. Let the main current be $I$ so that the application of Kirchoff's current law gives:

$$
\begin{equation*}
I=I_{0}+I_{R} \tag{1}
\end{equation*}
$$

$I_{R}$ is independent of $T$.
Hence:

$$
\begin{equation*}
\frac{d I}{d T}=\frac{d I_{0}}{d T} \tag{2}
\end{equation*}
$$

It is given that:

$$
\begin{equation*}
\frac{1}{I_{0}} \frac{d I_{0}}{d T}=0.15 \quad \text { and } \quad \frac{I}{I} \frac{d I}{d T}=0.07 \tag{3}
\end{equation*}
$$

Using Equation (2), we have:

$$
\frac{d I_{0}}{d T}=(0.15) I_{0}=(0.07) I=\frac{d I}{d T}
$$

or,

$$
\begin{equation*}
(0.07) I=(0.15) I_{0} \tag{4}
\end{equation*}
$$

Multiplying Equation (1) by 0.15 and subtracting Equation (4) from Equation (1), we obtain:

$$
\begin{gathered}
0.08 I=0.15 I_{R} \quad \text { or, } I_{R}=\frac{0.08}{0.15} I \quad \text { or, } \quad I_{R}=\frac{40}{15} \mu \mathrm{~A} \\
R=\frac{10 \times 15}{40}=3.75 \mathrm{M} \Omega
\end{gathered}
$$

Example 2-21 A diode is mounted on a chassis in such a manner that, for each degree of temperature rise above ambient, 0.1 mW is thermally transferred from the diode to its surroundings. (The thermal resistance of the mechanical contact between the diode and its surroundings is $0.15 \mathrm{~mW} /{ }^{\circ} \mathrm{C}$.) The ambient temperature is $25^{\circ} \mathrm{C}$. The diode temperature is not to be allowed to increase by more than $10^{\circ} \mathrm{C}$ above ambient. If the reverse saturation current is $5 \mu \mathrm{~A}$ at $25^{\circ} \mathrm{C}$ and increases at the rate $0.07^{\circ} \mathrm{C}^{-1}$, what is the maximum reverse-bias voltage which may be maintained across the diode?

## Solution:

Since the maximum permissible diode temperature is $35^{\circ} \mathrm{C}$, this must be the temperature at which we have thermal equilibrium. Thus:

$$
P_{\text {out }}=0.15 \mathrm{~mW} /{ }^{\circ} \mathrm{C} \times(35-25)^{\circ} \mathrm{C}=1.5 \mathrm{~mW}
$$

We know that the reverse saturation current approximately doubles for every $10^{\circ} \mathrm{C}$ rise in temperature. Thus at $35^{\circ} \mathrm{C}$, we can write:

$$
\begin{array}{lc} 
& I_{0}(35)=2 I_{0}(25)=10 \mu \mathrm{~A} \\
\therefore & P_{\mathrm{in}}=V \times I_{0}=1.5 \mathrm{~mW} \\
\text { or, } & \mathrm{V}=150 \mathrm{~V}
\end{array}
$$

Example 2-22 A Si diode operates at a forward voltage of 0.4 V . Calculate the factor by which the current will be multiplied when the temperature is increased from $25^{\circ} \mathrm{C}$ to $150^{\circ} \mathrm{C}$.

## Solution:

At the temperature of $150^{\circ} \mathrm{C}$, i.e., 423 K :

$$
V_{T}=\frac{423}{11,600}=0.0364 \mathrm{~V}
$$

We know that:

$$
I_{0}(T)=I_{01} \times 2^{\frac{\left(T-T_{0}\right)}{10}}
$$

At $150^{\circ} \mathrm{C}$ :

$$
I_{0}(150) I_{0}(25) \times 2^{12.5}=5792 I_{0}(25)
$$

Using $n=2$ for Si , we obtain form the diode equation:

$$
I=5792\left(\mathrm{e}^{0.4 / 0.0728}-1\right) I_{0}(25)
$$

or,

$$
I=5792 \times 242 \times I_{0}(25)
$$

On the other hand, at $25^{\circ} \mathrm{C}$ :

$$
I=I_{0}(25)\left(\mathrm{e}^{0.4 / 0.0514}-1\right)=2400 I_{0}(25)
$$

Hence,

$$
\frac{I(150)}{I(25)}=584
$$

At $25^{\circ} \mathrm{C}$ and $V=0.4 \mathrm{~V}, I(25)=0.01 \mathrm{~mA}$. At $150^{\circ} \mathrm{C}$ and $V=0.4 \mathrm{~V}, I(150)=2.42 \mathrm{~mA}$
or,

$$
\frac{I(150)}{I(25)}=242
$$

Example 2-23 (a) Consider a grown junction for which the uncovered charge density $\rho$ varies linearly with distance. If $\rho=a x$, prove that the barrier voltage $V_{j}$ is given by:

$$
V_{j}=\frac{a W^{3}}{12 \varepsilon}
$$

(b) Verify that the barrier capacitance $C_{T}$ is given by:

$$
C_{T}=\frac{\varepsilon A}{W}
$$

## Solution:

(a) From Poisson's equation:

$$
\frac{d^{2} V}{d x^{2}}=-\frac{\rho}{\varepsilon}=-\frac{a x}{\varepsilon} ; \quad \frac{d V}{d x}=-\frac{a x^{2}}{2 \varepsilon}+C_{1}
$$

Since, at $x=-\frac{W}{2}$ :

$$
\frac{d V}{d x}=0 ; \quad C_{1}=\frac{a W^{2}}{8 \varepsilon}
$$

(Assuming electric field does not extend outside the depletion region)
or,

$$
\frac{d V}{d x}=-\frac{a x^{2}}{2 \varepsilon}+\frac{a W^{2}}{8 \varepsilon}
$$

or,

$$
V=-\frac{a x^{3}}{6 \varepsilon}+\frac{a W^{2}}{8 \varepsilon} x+C_{2}
$$

Since, at $x=-\frac{W}{2}: \quad V=0 ; C_{2}=\frac{a x^{3}}{6 \varepsilon}-\frac{a W^{2}}{8 \varepsilon} x=-\frac{a W^{3}}{48 \varepsilon}+\frac{a W^{3}}{16 \varepsilon}=\frac{a W^{3}}{24 \varepsilon}$
At $x=+\frac{W}{2}: \quad V=V_{j}=-\frac{a W^{3}}{48 \varepsilon}+\frac{a W^{3}}{16 \varepsilon}+\frac{a W^{3}}{24 \varepsilon}=\frac{a W^{3}}{12 \varepsilon}$
(b) $Q=\int_{0}^{W / 2} A \rho d x=\int_{0}^{W / 2} \operatorname{Aaxdx}=\frac{A a}{2}\left(\frac{W}{2}\right)^{2}=\frac{A a W^{2}}{8}$

$$
C_{T}=\frac{d Q}{d V}=\frac{A a W}{4} \frac{d W}{d V}
$$

From Part (a):

$$
d V=\frac{a W^{2}}{4 \varepsilon} d W
$$

$$
\therefore \quad C_{T}=\frac{A a W}{4} \frac{4 \varepsilon}{a W^{2}}=\frac{\varepsilon A}{W}
$$

Example 2-24 Given a forward-bias Si diode with $I=1 \mathrm{~mA}$. If the diffusion capacitance is $C_{D}$ $=1.5 \mu \mathrm{~F}$, what is the diffusion length $L_{p}$ ? Assume that the doping of the $p$-side is much greater than that of the $n$-side.

## Solution:

We know that:

$$
C_{D}=\frac{L_{p}^{2}}{D_{p}} \frac{I}{\eta V_{T}}
$$

or,

$$
L_{p}^{2}=\frac{C_{D} D_{p} \eta V_{T}}{I}
$$

$L_{p}^{2}=\frac{C_{D} D_{p} \eta V_{T}}{I}$
or, $\quad L_{p}^{2}=\frac{1.5 \times 10^{-6} \times 13 \times 2 \times 0.026}{1 \times 10^{-3}}=1014 \times 10^{-6}$
$\therefore \quad L_{p}=31.84 \times 10^{-3} \mathrm{~m}$
(iii) The $p-n$ junction diode when operated in this portion of the characteristic is termed as a breakdown diode. It should be clearly understood that the term breakdown does not mean that the diode has been corrupted or burnt out. It is only a temporary mechanism, which can be restored when the reverse applied voltage is increased in the positive direction. In the forward-bias mode the forward current increases slowly with the increase of applied voltage till the voltage reaches a certain value called saturation voltage. After this, the current rises very sharply but the voltage remains constant.
(iv) Substituting $e=1.6 \times 10^{-19} \mathrm{C}, k_{B}=1.38 \times 10^{-23} \mathrm{~J} / \mathrm{K}$, and $T=300 \mathrm{~K}$ (i.e., at room temperature) in Equation (2.68), we get:

$$
\begin{equation*}
I=I_{s}\left(e^{\frac{39 \mathrm{~V}}{\eta}}-1\right) \tag{2-69}
\end{equation*}
$$

Neglecting the voltage drops in the bulk $p$-type and $n$-type regions, the voltage $V$ is approximately the voltage applied across the diode terminals.

When $V$ is positive and sufficiently high, the term unity in Equation (2-69) can be neglected, so that the current $I$ increases exponentially with the voltage $V$. When the diode is reverse biased we have $I=-I_{s}$. Thus, the reverse current is independent of the applied bias and its magnitude equals the reverse saturation current. The range of forward current for the diode operation is higher than the reverse saturation current. The forward current is in the range of milli-ampere, but the reverse current is in the range of microampere or less.

We have $\eta=1$ for Si diodes and $\eta=1$ for Ge diodes, therefore, for a given forward bias (larger than $V_{B}$ ) the current for a Si diode is less than that for a Ge diode.
(v) A study of the $I-V$ characteristics reveals two different regions: a non-linear region for low values of applied voltage and an almost linear region for high values of voltage. This leads us to give two different expressions for diode resistance. The non-linear region can be assumed to be made up of piecewise linear regions of extremely short voltage intervals where Ohm's law is valid.

The slope of the $I-V$ characteristic of the $p-n$ diode defines the dynamic or the ac resistance $r_{a c}$ of the diode, as shown in Figure 2-11(a). Thus, for a change of voltage $d V$, the corresponding change in current is $d I$. The corresponding $r_{a c}$ is defined as:


Figure 2-11 (a) Dynamic resistance calculation from $I-V$ characteristics of a $p-n$ junction diode (b) Static or dc resistance calculation from $I-V$ characteristics of a $p-n$ diode

$$
\begin{equation*}
r_{a c}=\frac{d V}{d I}=\frac{V_{2}-V_{1}}{I_{2}-I_{1}} \tag{2-70}
\end{equation*}
$$

From Equation (2-69), we obtain: $\quad r_{a c}=\frac{d V}{d I}=\frac{\eta}{39\left(I+I_{\mathrm{s}}\right)}$
$r_{a c}$ is not a constant and is determined by the operating voltage. The ratio between the voltage $V$ across the junction and the current $I$ flowing through the junction is called the static or the dc resistance $r_{d c}$ of the diode which can be mathematically written from Figure 2-11(b) as:

$$
\begin{equation*}
r_{d c}=\frac{V}{I} \tag{2-72}
\end{equation*}
$$

$r_{d c}$ is not a constant but varies significantly with the applied voltage as shown in Figure 2-11(b).
For a reverse-bias, such that, $|39 \mathrm{~V} / \eta| \approx 1$, the dynamic resistance is extremely large. For a Ge diode at room temperature, the forward ac resistance is $r_{a c}=26 / I$.

## Solved Examples

Example 2-25 Find the static resistance of a $p-n$ junction germanium diode if the temperature is $27^{\circ} \mathrm{C}$ and $I_{0}=20 \mu \mathrm{~A}$ for an applied voltage of 0.2 V .

## Solution:

Given:

$$
I_{0}=20 \mu \mathrm{~A}, V_{F}=0.2 \mathrm{~V}, t=27^{\circ} \mathrm{C}
$$

The forward current through the diode:

$$
\begin{aligned}
I & =I_{0}\left[e^{V / \eta V_{T}}-1\right] \\
& =20 \times 10^{-6}\left(e^{40 V_{F}}-1\right)=20 \times 10^{-6}\left(e^{40 \times 0.2}-1\right) \\
& =59.59915 \mathrm{~mA}
\end{aligned}
$$

Static resistance: $\quad r_{\mathrm{dc}}=\frac{0.0343}{80 \times 10^{-6}} e^{0.2 / 0.0343}=0.14625 \mathrm{M} \Omega$
Example 2-26 An ideal germanium diode has a reverse saturation current of $80 \mu$ A at a temperature of $125^{\circ} \mathrm{C}$. Find the dynamic resistance at that temperature for a 0.2 V bias in: (a) the forward direction and (b) the reverse direction.

## Solution:

Given:

$$
t=125^{\circ} \mathrm{C} \quad \text { or } \quad T=398 \mathrm{~K}, I_{0}=80 \mu \mathrm{~A}, \eta=1, V_{F}=0.2 \mathrm{~V}
$$

(a) Volt equivalent of the temperature:

$$
V_{T}=\frac{T}{11,600}=\frac{398}{11,600}=0.0343 \mathrm{~V}
$$

Diode current is given by:

$$
I=I_{0}\left[e^{V_{F} \eta V_{T}}-1\right]
$$

Differentiating with respect to $V: \quad \frac{d I}{d V}=\frac{I_{0}}{V_{T}} e^{V_{F} / V_{T}}$
or,

$$
\begin{aligned}
\frac{I}{R_{a c}} & =\frac{I_{0}}{V_{T}} e^{V_{F} / V_{T}} \\
R_{a c} & =\frac{V_{T}}{I_{0}} e^{-V_{F} / V_{T}} \\
& =\frac{0.0343}{80 \times 10^{-6}} e^{-0.200 .0343}=1.258 \Omega
\end{aligned}
$$

(b) Dynamic resistance in reverse direction:

$$
\begin{aligned}
R_{a c} & =\frac{V_{\mathrm{T}}}{I_{0}} e^{V_{F} V_{T}} \\
& =\frac{0.0343}{80 \times 10^{-6}} e^{0.20 .0343}=0.14625 \mathrm{M} \Omega
\end{aligned}
$$

Example 2-27 The reverse-bias saturation current for a $p-n$ junction diode is $1.5 \mu \mathrm{~A}$ at 300 K . Determine its ac resistance at 150 mV forward-bias.

## Solution:

We know that,

$$
\begin{aligned}
r_{a c} & =d V / d I \\
& =\frac{1}{\frac{d I}{d V}}=\frac{1}{\left(I_{0} / k_{B} T\right) \exp \left(V / V_{T}\right)}
\end{aligned}
$$

But at temperature of 300 K :

$$
\begin{aligned}
k_{B} T & =8.62 \times 10^{-5} \times 300 \\
& =25.86 \times 10^{-3} \\
r_{a c} & =\frac{25.86 \times 10^{-3}}{1.5 \times 10^{-6} \times \exp (0.15 / 0.02586)}
\end{aligned}
$$

$$
=\frac{25.86 \times 10^{3}}{495.69}=52.169 \mathrm{~W}
$$

Example 2-28 A diode reaches its maximum power rating of 2.5 W when operating in the forward mode at the forward voltage of 900 mV . Calculate: (a) the maximum allowable forward current $I_{f(\max )}$ (b) the forward diode resistance $R_{f}$

## Solution:

(a)

$$
I_{f(\max )}=\frac{P_{\max }}{v_{f}}=\frac{2.5 \mathrm{~W}}{0.9 \mathrm{~V}}=2.75 \mathrm{~A}
$$

(b)

$$
R_{j}=\frac{P_{\max }}{I_{\max }^{2}}=\frac{2.5}{2.2^{2}}=0.5165 \Omega
$$

Example 2-29 (a) The resistivities of the two sides of a step-graded germanium diode are $2 \Omega-\mathrm{cm}$ ( $p$-side) and $1 \Omega-\mathrm{cm}$ ( $n$-side). Calculate the height of the potential-energy barrier. (b) Repeat Part (a) for silicon $p-n$ junction.

## Solution:

(a)

$$
\rho=\frac{1}{\sigma}=\frac{1}{N_{A} e \mu_{p}}=2 \Omega-\mathrm{cm}
$$

or,

$$
N_{A}=\frac{1}{2 \times 1.6 \times 10^{-19} \times 1800}=1.74 \times 10^{15} / \mathrm{cm}^{3}
$$

Similarly,

$$
N_{D}=\frac{1}{1 \times 1.6 \times 10^{-19} \times 3800}=1.65 \times 10^{15} / \mathrm{cm}^{3}
$$

Therefore the height of the potential energy barrier is:

$$
V_{0}=0.026 \times \ln \frac{1.65 \times 10^{15} \times 1.74 \times 10^{15}}{\left(2.5 \times 10^{13}\right)^{2}}=0.22 \mathrm{eV}
$$

(b)

$$
\begin{aligned}
& N_{A}=\frac{1}{2 \times 1.6 \times 10^{-19} \times 500}=6.25 \times 10^{15} / \mathrm{cm}^{3} \\
& N_{D}=\frac{1}{1 \times 1.6 \times 10^{-19} \times 1300}=4.8 \times 10^{15} / \mathrm{cm}^{3} \\
\therefore \quad & V_{0}=0.026 \times \ln \frac{4.8 \times 10^{15} \times 6.25 \times 10^{15}}{\left(1.5 \times 10^{10}\right)^{2}}=0.667 \mathrm{eV}
\end{aligned}
$$

Example 2-30 An ideal Ge $p-n$ junction diode has at a temperature of $125^{\circ} \mathrm{C}$ a reverse saturation current of $35 \mu \mathrm{~A}$. At a temperature of $125^{\circ} \mathrm{C}$ find the dynamic resistance for a 0.2 V bias in: (a) the forward direction (b) the reverse direction.

## Solution:

(a) At the temperature of $125^{\circ} \mathrm{C}$, that is 398 K ,

$$
V_{T}=\frac{398}{11,600}=0.0343 \mathrm{~V}
$$

For Germanium we know that $\eta=1$.
Thus, $I=I_{0}(125)\left(e^{V / V_{T}(125)}-1\right) \approx I_{0}(125)\left(e^{V / V_{T}(125)}\right)$ since $\frac{V}{V_{T}(125)} \gg 1$.
Differentiating with respect to $V$ :

$$
\frac{1}{r}=\frac{d I}{d V}=\frac{I_{0}(125)}{V_{T}(125)} e^{V V_{T}(125)}=\frac{35.0 \times 10^{-6}}{34.3 \times 10^{-3}} e^{5.83}=0.348
$$

or, $\quad r=2.873 \Omega$
(b) $\frac{I}{r}=\frac{d I}{d V}=\frac{I_{0}(125)}{V_{T}(125)} e^{-V V_{T}(125)}=3.185 \times 10^{-6} \mathrm{mho}$
or, $\quad r=0.314 \mathrm{M} \Omega$

## 2-7 LINEAR PIECEWISE MODELS

The $p-n$ junctions are unilateral in nature, i.e., they conduct current in only one direction. Thus, we can consider an ideal diode as a short circuit when forward-biased and as an open circuit when reversebiased. Forward-biased diodes exhibit an offset voltage $\left(V_{y}\right)$ that can be approximated by the simple equivalent circuit with a battery in series with an ideal diode. The series battery in the model keeps the ideal diode turned off for applied voltage less than $V$; the actual diode characteristic is improved by adding a series resistance $(r)$ to the equivalent circuit. The equivalent diode model, as shown in Figure 2-12, is called the piecewise linear equivalent model.

The approximate characteristics are linear over specific voltage and current ranges. This approximated characteristic of the device by a straight-line segment is shown in Figure 2-13.


Figure 2-12 Linear piecewise models of a diode for different order of approximations


Figure 2-13 I-V characteristics of $p-n$ junction diode


Figure 2-14 Reverse-biased $p-n$ junction


Figure 2-15 Reverse breakdown in a $p-n$ junction

It is obvious from Figure 2-13 that the straight line segments do not result in an exact duplication of the actual characteristics, especially in the knee region. From a practical point of view, the resulting segments are sufficiently close to the actual curve to establish an equivalent circuit that will provide an excellent first approximation to the actual behaviour of the device.

Thus, in the linear piecewise model we neglect the bending of the curve at the knee region, making an idealistic assumption compared to a switch.

## 2-8 BREAKDOWN DIODE

Breakdown diodes are $p-n$ junction diodes operated in the reverse-bias mode, as shown in Figure 2-14.

This breakdown occurs at a critical reverse-bias voltage $\left(V_{b r}\right)$. At this critical voltage the reverse current through the diode increases sharply, and relatively large currents flow with little increase in voltage, as shown in Figure 2-15. These diodes are designed with sufficient powerdissipation capabilities to work in the breakdown region. The following two mechanisms can cause reverse breakdown in a junction diode.

## 2-8-1 Zener Breakdown

Zener breakdown occurs when a sufficiently large reverse-bias is applied across a $p-n$ junction diode. The resulting electric field at the junction imparts a very large force on a bound electron, enough to dislodge it from its covalent bond. The breaking of the covalent bonds produces a large number of EHP (electron-hole pairs). Consequently the reverse current becomes very large. This type of breakdown phenomena is known as Zener breakdown.


Figure 2-16(a) Energy band diagram of a Zener diode


Figure 2-16(b) Reverse bias with electron tunneling from $p$ to $n$ leads to Zener breakdown

An essential criterion for the Zener mechanism to occur is the existence of a sufficiently thin depletion region, enabling the applied potential to create a high field at the junction, unlike an ordinary diode. This needs high doping and the Zener breakdown voltage tends to zero on increasing the doping. Figure 2-16(a) exhibits the energy band diagram of a Zener diode.

Zener breakdown occurs in a narrow depletion region due to which quantum mechanical tunneling takes place. It is purely a quantum mechanical process, (with no classical analogy) which states that particles with lower energy compared to the barrier energy in front of them can penetrate to the other side of the barrier, thus having a tunneling effect. When the reverse-bias is increased, the valance band of the $p$-side slowly moves up over the conduction band of the $n$-side and the tunneling probability increases as the number of filled states of the $p$-side moves up over $n$-side. Electron tunneling from the $p$-type valence band to the $n$-type conduction band produces a reverse current known as the Zener effect. Figure 2-16(b) shows the energy band diagram under reverse-biased condition with electron tunneling from $p$ to $n$ causing Zener breakdown.

The Zener breakdown voltage decreases with increasing temperature; the temperature coefficient of the Zener breakdown voltage is negative. Figure 2-16(c) exhibits the I-V curve for the Zener diode.

## 2-8-2 Avalanche Breakdown

In a reverse-biased junction, the minority-carriers drift across the depletion region. On their way across this region, they occasionally have collisions with atoms in the lattice. With


Figure 2-16(c) I-V characteristics
a large enough field, a carrier drifting across the depletion region is accelerated to the point where it has enough energy to knock a valance electron free from its host atom during a collision. The field then separates the electron and hole of this newly created EHP and we now have three mobile carriers instead of one. This process is called avalanche multiplication. The multiplication can become quite large if the carriers generated by this collision also acquire to create more carriers, thereby initiating a chain reaction. Once the process starts, the number of multiplication that can occur from a single collision increases rapidly with further increase in the reverse-bias, so the terminal current grows rapidly, and we say that the junction breaks down. This is called avalanche breakdown.

Under the condition of low carrier concentration, the breakdown voltage is larger and avalanche multiplication is a dominant factor since the electric field required for Zener breakdown is much higher and the avalanche breakdown sets in before that can be achieved. In spite of the two different breakdown mechanisms, the breakdown diodes are commonly referred to as Zener diodes.

Under the condition of low doped semiconductors, the electron tunneling is negligible. The breakdown in such cases involves impact ionization of atoms by energetic carriers. For a large electric field $E_{O}$ inside the depletion region, an electron entering from the $p$-type semiconductor may acquire the energy needed to cause an ionizing collision with the lattice atom creating an EHP. A single such event results in multiplication of carriers; the original electron as well as the secondary electron are swept to the $n$-type semiconductor, while, the generated hole is swept to the $p$-type semiconductors as exhibited in Figure 2-17. A very high degree of multiplication can be achieved if the carriers generated within the depletion zone also have ionizing collisions with the lattice; that is, an incoming carrier creates a new EHP. Again, each new carrier creates an EHP, and the process continues. This is called avalanche process, since each incoming carrier can create a large number of new carriers resulting in an avalanche of carriers.

We shall present a simplified analysis of this avalanche multiplication of carriers. Let us assume that a charge carrier, while being accelerated through the depletion zone of width $L$, as shown in Figure 2-18 has a probability $P$ of creating an EHP by undergoing ionizing collision with the lattice. Then for $n_{i n}$ incoming electrons entering the depletion region from the $p$-region, $P n_{i n}$ secondary EHPs will be generated. Now these generated electrons move to the $n$-region while the generated holes travel to the $p$-region under the electric field. As the total distance traversed by this EHP is still W, they in turn generate new EHPs with the same probability. In all, assuming no recombination, the total number of electrons coming out of the depletion region in the $n$-region can be expressed as

$$
\begin{equation*}
n_{\mathrm{out}}=n_{\mathrm{in}}\left(1+P+P^{2}+\cdots\right) \tag{2-73}
\end{equation*}
$$

Therefore, by using the summation formula for an infinite geometric progression series, the multiplication factor is given by:


Figure 2-17 Avalanche breakdown in low doped semiconductor


Figure 2-18 Carrier multiplications in the depletion region due to impact ionization

$$
\begin{equation*}
M=\frac{n_{\text {out }}}{n_{\mathrm{in}}}=1+P+P^{2}+\cdots=\frac{1}{1-P} \tag{2-74}
\end{equation*}
$$

The probability of an ionizing collision as a carrier travels through the depletion region can also be expressed as:

$$
\begin{equation*}
P=\int_{0}^{L} \alpha d x \tag{2-75}
\end{equation*}
$$

where $\alpha$ is known as the ionization coefficient.
For the avalanche process to be self-sustaining, $M$ should be infinite and thus, we can write:

$$
\begin{equation*}
P=\int_{0}^{l} \alpha d x=1 \tag{2-76}
\end{equation*}
$$

where, the dependence of $\alpha$ on the electric field can, in general, be expressed as

$$
\begin{equation*}
\alpha=\alpha_{0} \exp \left[-\left(\frac{b}{E_{0}}\right)^{t}\right] \tag{2-77}
\end{equation*}
$$

where, the constants $\alpha_{0}, b$, and $t$ are characteristics of the particular semiconductor.
It must be pointed out that the present analysis is the oversimplified version of the reality and actually the ionization probability is related to the junction parameters in a much more complicated fashion. Qualitatively, we can expect the ionization probability to increase with increasing electric field and therefore, on the application of reverse-bias the ionization probability increases. A widely used empirical relation between the multiplication factor $M$ and the applied reverse voltage near breakdown $\left(V_{B R}\right)$ is given by:

$$
\begin{equation*}
M=\frac{1}{\left[1-\left(\frac{V}{V_{B R}}\right)^{t}\right]} \tag{2.78}
\end{equation*}
$$

where, $t$ varies between 3 and 6 depending on the semiconductor material. In general, the critical reverse voltage for breakdown increases with increasing values of band gap, since more energy is required for ionization in the case of larger band gap materials.


Figure 2-19 The I-V characteristics comparison between Zener and avalanche breakdown


Figure 2-20 Comparison of Zener breakdown of Ge and Si semiconductor diodes with respect to I-V curve

Table 2-1 Comparison between Zener and Avalanche breakdown

## Zener Breakdown

1. Narrow depletion region and quantum mechanical tunneling takes place.
2. Highly doped diode with reverse-bias is required.
3. Operates at low voltage up to few volts reverse-bias.
4. Impact ionization does not occur in this case.

Avalanche Breakdown

1. Higher depletion region width and electron tunneling is negligible.
2. Low doped diode with reverse-bias is sufficient.
3. Breakdown occurs at high reverse-bias from a few volts to thousands of volts.
4. This breakdown mechanism involves the impact ionization of host atoms by energetic carriers.

From the breakdown conditions described so far and the field dependence of the ionization coefficient, the critical electric field $E_{c}$ at which the avalanche process and breakdown occurs is given by:

$$
\begin{equation*}
V_{B R}=\frac{E_{c} l}{2}=\frac{\varepsilon_{s} E_{c}^{2}}{2 e N_{d}} \tag{2-79}
\end{equation*}
$$

Thus, we can infer from Equation (2-79) that for junctions where breakdown takes place due to the avalanche process, the breakdown voltage increases with reduction in the doping concentration. The comparison between Zener and avalanche breakdown with respect to the I-V characteristics has been shown in Figures 2-19 and 2-20 respectively.

## Solved Examples

Example 2-31 For a Zener shunt regulator if $V_{z}=10 \mathrm{~V}, R_{s}=1 \mathrm{k} \Omega, R_{L}=10 \mathrm{k} \Omega$, and the input voltage varies from 25 to 40 V . Find the maximum and minimum values of Zener current.

## Solution:

Given:

$$
\begin{gathered}
\mathrm{V}_{Z}=\mathrm{V}_{0}=10 \mathrm{~V}, \mathrm{R}_{s}=1 \mathrm{k} \Omega, \mathrm{R}_{L}=10 \mathrm{k} \Omega, \mathrm{~V}_{i}=25 \text { to } 40 \mathrm{~V} . \\
\mathrm{V}_{i(\min )}=25 \mathrm{~V} \quad \text { and } \quad \mathrm{V}_{i(\max )}=40 \mathrm{~V}
\end{gathered}
$$

Maximum value of Zener current:

$$
\begin{aligned}
I_{z}= & \frac{V_{l(\max )}-V_{z}}{R_{L(\min )}} \\
& =\frac{40-10}{1000}-5 \times 10^{-3}=25 \mathrm{~mA}
\end{aligned}
$$

Minimum value of Zener current is given by:

$$
\begin{aligned}
I_{z(\min )} & =\frac{V_{i(\min )}-V_{z}}{R_{s}}-I_{L(\max )} \\
& =\frac{25-10}{1000}-5 \times 10^{-3}=10 \mathrm{~mA} \quad\left(\because I_{L(\min )}=I_{L(\min )}=I_{L}\right)
\end{aligned}
$$

Example 2-32 A 5 V Zener diode has a maximum power dissipation of 250 mW . It maintains a constant voltage when the current through the diode does not fall below $10 \%$ of the maximum permissible current. A 15 V supply is given to the Zener through a series resistor $R$. Find the range for $R$ so that the Zener maintains its constant voltage. Find the new range when the diode is loaded by 50 W loads.

## Solution:

Maximum permissible current $=\frac{250 \times 10^{-3}}{5}=50 \mathrm{~mA}$

$$
10 \% \text { of } 50 \mathrm{~mA}=5 \mathrm{~mA}
$$

Maximum current through the diode to maintain constant voltage $=50-5=45 \mathrm{~mA}$
Example 2-33 In a $p^{+} n^{+}$diode, the doping concentration of the $n$-region is $2 \times 10^{15} \mathrm{~cm}^{-3}$. If the critical field at the avalanche breakdown is $1.5 \times 10^{5} \mathrm{Volt} / \mathrm{cm}$. Find out the breakdown voltage assuming the width of the $n$-region is $10 \mu \mathrm{~m}$.

## Solution:

For this junction diode the depletion region exists only in the $n$-region.
At breakdown the peak electric field is $\left|E_{P}\right|=1.5 \times 10^{5} \mathrm{~V} / \mathrm{cm}$
Therefore the width of the depletion region $W$ is given by:

$$
W=\frac{\left|E_{p}\right| \varepsilon}{e N_{D}}=\frac{1.5 \times 10^{5} \times 11.9 \times 8.854 \times 10^{-14}}{1.6 \times 10^{-19} \times 2 \times 10^{15}}=4.939 \mu \mathrm{~m}
$$

Therefore, the breakdown voltage:

$$
V_{B R}=\frac{\left|W E_{P}\right|}{2}=\frac{1.5 \times 10^{5} \times 4.939 \times 10^{-4}}{2}=37.04 \mathrm{~V}
$$

Example 2-34 (a) Prove that the magnitude of the maximum electric field $E_{m}$ at a step-graded junction with $N_{A} \gg N_{D}$ is given by:

$$
E_{m}=\frac{2 V_{j}}{W}
$$

(b) It is found that Zener breakdown occurs when $E_{m}=2 \times 10^{7} \mathrm{~V} / \mathrm{m}=E_{z}$. Prove that Zener voltage $V_{Z}$ is given by:

$$
V_{z}=\frac{\varepsilon E_{z}^{2}}{2 e N_{D}}
$$

## Solution:

(a) We have:

$$
E(x)=\frac{-e N_{D}}{\varepsilon}(x-W)
$$

Obviously, $E(x)$ is maximum at $x=0$.
Hence,

$$
\begin{gathered}
E_{\max }=\frac{e N_{D}}{\varepsilon} \mathrm{~W} \\
V_{j}=\frac{e N_{D}}{2 \varepsilon} \mathrm{~W}^{2}
\end{gathered}
$$

We have:

Thus,

$$
E_{\max }=\frac{2 V_{j}}{W}
$$

(b) We have:

$$
W=\left(\frac{2 \varepsilon}{\mathrm{e} N_{D}} V_{j}\right)^{1 / 2}
$$

Substituting this value in the result of part (a), we obtain:

$$
e_{\max }=\frac{2 V_{j}}{W}=\frac{2 V_{j}}{\left(\frac{2 \varepsilon}{e N_{D}} \mathrm{~V}_{j}\right)^{1 / 2}}=\frac{2 V_{j}^{1 / 2}}{\left(\frac{2 \varepsilon}{e N_{D}}\right)^{1 / 2}}
$$

Solving for $V_{j}$ we obtain: $\quad V_{j}=\frac{\varepsilon}{2 e N_{D}} E_{\max }^{2}=V_{0}-V_{d}=V_{z}$
Example 2-35 (a) Zener breakdown occurs in Ge at a field intensity of $2 \times 10^{7} \mathrm{~V} / \mathrm{m}$. Prove that the breakdown voltage is $V_{Z}=51 / \sigma_{p}$, where $\sigma_{p}$ is the conductivity of the $p$ material in $(\Omega \mathrm{cm})^{-1}$. Assume that $N_{A} \ll N_{D}$.
(b) If the $p$-material is essentially intrinsic, calculate $V_{Z}$.
(c) For a doping of 1 part in $10^{8}$ of $p$-type material, the resistivity drops to $3.9 \Omega \mathrm{~cm}$. Calculate $V_{Z}$.
(d) For what resistivity of the $p$-type material will $V_{Z}=1.5 \mathrm{~V}$ ?

## Solution:

(a) From Example 2-34, we can write:

$$
V_{z}=\frac{\varepsilon}{2 e N_{A}} E_{z}^{2}
$$

We know, $\sigma_{p}=\mathrm{N}_{A} \mathrm{e} \mu_{p}$

$$
\begin{gathered}
\text { or, } e N_{A}=\frac{\sigma_{p}}{\mu_{p}} \quad \text { Thus, } \quad V_{z}=\frac{\varepsilon E_{z}^{2} \mu_{p}}{2 \sigma_{p}} \\
V_{z}=\left(\frac{16}{36 \pi \times 10^{9}} \mathrm{~F} / \mathrm{m}\right) \times\left(\frac{4 \times 10^{14}}{2} \mathrm{~V}^{2} / \mathrm{m}^{2}\right) \times\left(1800 \frac{\mathrm{~cm}^{2}}{\mathrm{~V}-\mathrm{sec}}\right) \times\left(10^{-6} \frac{\mathrm{~m}^{3}}{\mathrm{~cm}^{3}}\right) \times \frac{1}{\sigma_{p}}(\Omega-\mathrm{cm}) \\
V_{z}=\frac{51}{\sigma_{p}} \text { where } \sigma_{p} \text { is in }(\Omega-\mathrm{cm})^{-1}
\end{gathered}
$$

(b)

$$
\sigma_{i}=\frac{1}{45}
$$

$$
\therefore \quad V_{z}=51 \times 45=2300 \mathrm{~V}
$$

(c)

$$
\sigma_{p}=\frac{1}{3.9}(\Omega-\mathrm{cm})^{-1}
$$

$$
\therefore \quad V_{z}=51 \times 3.9=198.9 \mathrm{~V}
$$

(d) From part (a), $I=6 \times 10^{-6}\left(e^{100 / 26}-1\right)=6 \times 10^{-6}(46.5-1)$

Example 2-36 (a) Two $p-n$ Ge diodes are connected in series opposing. A 5 V battery is impressed upon this series arrangement. Find the voltage across each junction at room temperature. Assume that the magnitude of the Zener voltage is greater than 5 V .
(b) If the magnitude of the Zener voltage is 4.9 V , what will be the current in the circuit? The reverse saturation current is $6 \mu \mathrm{~A}$.

## Solution:

The current is same in each diode but in one it is in the reverse direction. To obtain a forward current equal to the reverse saturation current requires a very small voltage. We have, $I=I_{0}\left(e^{V / \eta V_{\mathrm{T}}}-1\right)=I_{0}$. For Ge, $\eta=1$, andat $T=300 \mathrm{~K}, V_{T}=0.026 \mathrm{~V}$. Thus, $e^{\mathrm{V} / \mathrm{V}_{T}}=2$ or, $V=0.693 \times 0.026=0.018 \mathrm{~V}$.Hence, the voltage across the second diode is $5-0.018 \approx 4.98 \mathrm{~V}$. Since this voltage is in the reverse direction, current $I=$ $I_{0}\left(e^{4.980 .026}-1\right) \approx-I_{0}$. This confirms the above assumption that saturation current flows.
(b) If the Zener voltage is 4.9 V , then the voltage across the reverse-biased diode is 4.9 V . This leaves 0.1 V across the forward-biased diode. If $I_{0}=5 \mu \mathrm{~A}$, then

$$
I=6 \times 10^{-6}\left(e^{100 / 26}-1\right)=6 \times 10^{-6}(46.5-1)=273.6 \mu \mathrm{~A} .
$$

Example 2-37 The diode current of a $p-n$ junction diode is 0.5 mA . at 340 mV and again 15 mA at 465 mV . Assuming $k_{B} T / e=5 \mathrm{mV}$. find out the ideality factor.

## Solution:

We know that

$$
I=I_{s}\left(e^{\frac{e V}{\eta K_{B}^{T}}}-1\right)
$$

Since $e^{\frac{e V}{\eta K_{B} T}} \gg 1$, we can write $I=I_{s}\left(e^{\frac{e^{V}}{\eta K_{B} T}}\right)$

Therefore, according to the question we get:

$$
\frac{1.5 \mathrm{~mA}}{0.5 \mathrm{~mA}}=\frac{\exp \left(\frac{465}{25 \eta}\right)}{\exp \left(\frac{340}{25 \eta}\right)}
$$

or,

$$
30=\exp \left(\frac{5}{\eta}\right)
$$

or,

$$
\frac{5}{\eta}=2.303 \log _{10}(30)
$$

or,

$$
\eta=\frac{5}{3.4}=1.47
$$

Example 2-38 A series combination of a 12 V avalanche diode and a forward-biased Si diode is to be used to construct a zero-temperature-coefficient voltage reference. The temperature coefficient of the Si diode is $-1.7 \mathrm{mV} /{ }^{\circ} \mathrm{C}$. Express in percent per degree centigrade the required temperature coefficient of the Avalanche diode.

## Solution:

For the Si diode, the temperature coefficient $=-1.7 \mathrm{mV} /{ }^{\circ} \mathrm{C}$. If the series combination is to have a zero-temperature coefficient, then the temperature coefficient of the avalanche diode must be at the biasing current $+1.7 \mathrm{mV} /{ }^{\circ} \mathrm{C}$. In percentage, temperature coefficient:

$$
\frac{1.7 \times 10^{-3} \mathrm{~V}}{12 \mathrm{~V}}(100 \%)=0.0142 \% /{ }^{\circ} \mathrm{C}
$$

Example 2-39 (a) The avalanche diode regulates at 60 V over a range of diode currents from 5 to 40 mA . The supply voltage $V=200 \mathrm{~V}$. Calculate $R$ to allow voltage regulation from a load current $I_{L}=0$ up to $I_{\max }$, the maximum possible value of $I_{L}$. What is $I_{\max }$ ?
(b) If $R$ is set as in part (a) and the load current is set at $I_{L}=25 \mathrm{~mA}$, what are the limits between which $V$ may vary without loss of regulation in the circuit?

## Solution:

(a) For $I_{L}=0$ and $V_{0}=60$, we have $I_{D}=I_{T}=\frac{200-60}{\mathrm{R}} \leq 40 \mathrm{~mA}$
or,

$$
R \geq \frac{140}{40} \times 10^{3}=3.5 \mathrm{~K}
$$

For $I_{L}=I_{\max }$ :

$$
\begin{gathered}
I_{D} \leq 5 \mathrm{~mA}, R=3.5 \mathrm{~K}, I_{T}=40 \mathrm{~mA} \\
I_{\max }=40-5=35 \mathrm{~mA}
\end{gathered}
$$

Hence,
(b) Minimum current $I_{D}$ for good regulation is 5 mA . Hence, $I_{T}=25+5=30 \mathrm{~mA}$ and $V_{\max }=30$ $\times 3.5+60=165 \mathrm{~V}$. Maximum current $\mathrm{I}_{D}$ for good regulation is 40 mA . Hence, $\mathrm{I}_{T}=65 \mathrm{~mA}$ and $V_{\text {max }}=65 \times 3.5+60=287.5 \mathrm{~V}$.

## POINTS TO REMEMBER

1. When donor impurities are introduced into one side and acceptors into the other side of a single crystal of a semiconductor through various sophisticated microelectronic device-fabricating techniques a $p-n$ junction is formed.
2. A $p-n$ junction is said to be in thermal equilibrium when it is at a uniform temperature and no external disturbances, such as light or a bias voltage, are acting on it.
3. The thin layer on each side of the $p-n$ junction has no free electrons or holes. This thin layer is depleted of mobile carriers and is called depletion layer.
4. The nature of the $p-n$ junction so formed may be of two types:
(a) A step-graded junction: In a step-graded junction, the acceptor or the donor impurity density in the semiconductor is constant up to the junction.
(b) A linearly-graded: In a linearly-graded junction, the impurity density varies almost linearly with distance away from the junction.
5. The electric field between the acceptor and the donor ions is called a barrier. It is equivalent to a difference of potential called the barrier potential.
6. The width of the depletion region is inversely proportional to the doping strength, as a larger carrier concentration enables the same charge to be achieved over a smaller dimension.
7. The Fermi level is invariant at thermal equilibrium.
8. Connecting the positive terminal of the battery to the $p$-type and the negative terminal to the $n$-type of the $p-n$ junction is called for-ward-biasing.
9. Connecting the negative terminal of the battery to the $p$-type and the positive terminal to the $n$-type of the $p-n$ junction is called reverse-biasing.
10. In reverse-biased condition, the current that flows through the diode is called reverse saturation current. At absolute zero, this current is zero.
11. The forward-biased barrier potential is typically 0.7 V for silicon diode and 0.3 V for a germanium diode. These values increase slightly with forward current.
12. There is a very small current called reverse saturation current in a reverse-bias due to the thermally generated minority-carriers.
13. The voltage at which the forward current rises sharply is known as cut-in voltage.
14. The reverse saturation current is dependent on temperature. The reverse saturation current approximately doubles for every $10^{\circ} \mathrm{C}$ rise in temperature.
15. Reverse breakdown voltage for a diode is typically greater than 50 V .
16. An ideal diode is one which acts as a short circuit (zero resistance) when forward-biased and as an open circuit (infinite resistance) when reverse-biased.
17. The resistance offered by a doped semiconductor is called the bulk resistance.
18. Forward resistance (dc) of a diode is the ratio of the dc voltage across the diode to the resulting dc current flowing through it.
19. Dynamic resistance (ac) is the ratio of small change in forward voltage to the corresponding change in the diode current.
20. The Junction Capacitance is proportional to $V_{T}^{1 / 2}$ for step junction and to $V_{T}^{3 / 2}$ for graded junction cases respectively.
21. Zener diode is a $p-n$ junction diode, which is designed to sustain heavy current at the Zener breakdown region.
22. There are two mechanisms which give rise to the breakdown of a $p-n$ junction under reverse bias condition: (i) Avalanche breakdown (ii) Zener breakdown.
23. $I-V$ characteristics of a Zener diode is as shown:
24. Breakdown can be made very abruptly at accurately known values ranging from 2.4 V to 200 V with power ratings from 1 W to 50 W .
25. A Zener diode maintains a nearly constant voltage across its terminals over a specified range of Zener current.
26. Zener diodes are used as voltage regulators and limiters.
27. The tunnel diode is a negative-resistance semiconductor $p-n$ junction diode. The negative resistance is created by the tunnel effect of the electrons in the $p-n$ junction.

28. The doping of both the $p$ - and $n$-type regions of the tunnel diode is very high-impurity concentration of $10^{19}$ to $10^{20}$ atoms $/ \mathrm{cm}^{3}$ are used (which means both $n$-type and $p$-type semiconductors having parabolic energy bands are highly degenerate) - and the depletion layer barrier at the junction is very thin, in the order of $10^{-6} \mathrm{~cm}$.
29. Charge carriers recombination takes place at $p-n$-junction as electron crosses from the $n$-side and recombines with holes on the $p$-side. When the junction is forward-biased the free electron is in the conduction band and is at a higher energy level than hole located at valence band.

## IMPORTANT FORMULAE

1. Fermi level in $n$-side of a $p-n$ diode is given by:

$$
E_{f n}=E_{c n}-k_{B} T \ln \frac{N_{c}}{N_{d}}
$$

2. Fermi level in $p$-side of a $p-n$ diode is given by:

$$
E_{f p}=E_{c p}-k T \ln \frac{N_{c} N_{a}}{n_{i}^{2}}
$$

3. Fermi level invariance: $\frac{d E_{F}}{d x}=0$
4. Electric field in a abrupt junction is given by:

$$
-E_{0}=\frac{d V}{d x}=\frac{e N_{a}}{\varepsilon}\left(x+x_{p}\right)
$$

5. Total voltage in an abrupt junction is given by:

$$
V_{T}=V_{2}-V_{1}=\frac{e}{2 \varepsilon}\left(N_{a} X_{p}^{2}+N_{d} X_{n}^{2}\right)
$$

6. The width of the depletion regions in $p$-type region is given by:

$$
X_{p}=\left(\frac{2 \varepsilon}{e N_{a}} \frac{V_{T} N_{d}}{N_{d}+N_{a}}\right)^{\frac{1}{2}}
$$

7. The width of the depletion regions in $n$-type region is given by:

$$
x_{n}=\left(\frac{2 \varepsilon}{e N_{d}} \frac{V_{T} N_{a}}{N_{a}+N_{d}}\right)^{\frac{1}{2}}
$$

8. Maximum electric field is given by:

$$
E_{0 \max }=-\frac{d V}{d X}{ }_{x=0}=-\frac{e N_{a} \mathrm{x}_{p}}{\varepsilon}=-\frac{e N_{d} x_{n}}{\varepsilon}
$$

9. The junction capacitance is is given by:

$$
C_{j}=K_{1} V_{T}^{-\frac{1}{2}}=K_{1}\left(V_{d}-V_{a}\right)^{-\frac{1}{2}}
$$

10. The total voltage is given by: $V_{T}=\frac{2 e a x_{p}^{3}}{3 \varepsilon}$
11. The width of the transition region in the $n$ - or $p$-type is is given by:

$$
\left|x_{n}\right|=\left|x_{p}\right|=\frac{l}{2}=\left(\frac{3 \varepsilon}{2 e a}\right)^{\frac{1}{3}} V_{T}^{\frac{1}{3}}
$$

12. The maximum electric field is given by:

$$
E_{0 \max }=-\frac{e a x_{p}^{2}}{2 \varepsilon}
$$

13. The junction capacitance is given by:

$$
C_{j}=\frac{d Q}{d V_{T}}=A\left(\frac{e a \varepsilon^{2}}{12}\right)^{\frac{1}{3}} V_{T}^{\frac{1}{3}}
$$

14. The depletion capacitance in aVaractor diode is given by:

$$
C_{j}=\frac{A \varepsilon_{5}}{\mathrm{~L}} \alpha\left(V_{\mathrm{T}}\right)^{-1 /(n+2)}
$$

15. If varactor is used with an inductance $L$ in a resonant circuit, the resonant frequency of the circuit is given by:

$$
f_{r}=\frac{1}{2 \pi \sqrt{L C}} \alpha V_{\mathrm{T}}
$$

16. The total diode-current density in a semiconductor diode is given by:
$J=e\left(\frac{D_{p} p_{n}}{L_{p}}+\frac{D_{n} n_{p}}{L_{n}}\right)\left[\exp \left(\frac{e V}{k_{B} T}\right)-1\right]$
17. The total direct current of the diode, with a cross-sectional junction area $A$ is:

$$
\begin{aligned}
I & =A J_{s}\left[\exp \left(\frac{e V}{k_{B} T}\right)-1\right] \\
& =I_{s}\left[\exp \left(\frac{e V}{k_{B} T}\right)-1\right]
\end{aligned}
$$

18. Dynamic diode resistance is given by:

$$
r_{a c}=\frac{d V}{d I}=\frac{\eta}{39(I+I)}
$$

19. Barrier potential is given by:

$$
V_{B}=\frac{k T}{e} \log _{e}\left(\frac{n}{p}\right)
$$

20. Decrease in barrier potential is given by:

$$
\Delta V_{B}=-0.002 \times \Delta t
$$

21. Diffusion current density is given by:

$$
J_{\text {(diff) }}=-e D_{p} \frac{d p}{d x}+e D_{n} \frac{d n}{d x}
$$

22. Drift current density is given by:

$$
J_{(\text {diff })}=J_{p}+J_{n}
$$

23. Forward diode current: $I_{f}=I_{p}+I_{n}$
24. V-I characteristic of a diode:

$$
I=I_{0}\left(e^{V_{\eta} V_{T}}-1\right)=I_{0}\left(e^{V_{V / k T}}-1\right)
$$

25 . Volt equivalent temperature is given by:

$$
V_{T}=\frac{T}{11,600}
$$

26. Forward diode current is given by:

$$
I_{F}=I_{0} e^{\nu_{m} V_{T}}
$$

27. Diode reverse current is given by:

$$
I_{R}=I_{0}\left[e^{V_{n} V_{T}}-1\right]
$$

## OBJECTIVE QUESTIONS

## 1. In a $p-n$ junction diode:

(a) The depletion capacitance increases with increase in the reverse-bias.
(b) The depletion capacitance decreases with increase in the reverse-bias.
(c) The diffusion capacitance increases with increase in the forward-bias.
(d) The diffusion capacitance is much higher than the depletion capacitance when it is forward-biased.
2. A $p-n$ junction in series with a 100 ohms resistor is forward-biased so that a current of 100 mA flows. If the voltage across this combination is instantaneously reversed to 10 volt at $t=0$ the reverse current that flows through the diode at $t=0$ is approximately given by:
(a) 20 mA
(b) 100 mA
(c) 200 mA
(d) None of the above
3. The width of the depletion region is:
(a) Directly proportional to doping
(b) Inversely proportional to doping
(c) Independent of doping
(d) None of the above
4. The Fermi energy in $p-n$ junction at thermal equilibrium is:
(a) Proportional to distance
(b) Directly increases with the temperature
(c) Invariant with respect to distance
(d) None of the above
5. The depletion capacitance, $C_{j}$ of an abrupt $p-n$ junction with constant doping on either side varies with reverse bias, $V_{R}$, as:
(a) $C_{j} V_{R}^{3}$
(b) $C_{j} \mu V_{R}^{-2}$
(c) $C_{j} \alpha V_{R}^{-1 / 2}$
(d) None of the above
6. Gold is often diffused into silicon $p-n$ junction devices to:
(a) Is proportional to the square of the recombination rate
(b) Is proportional to the cube of the recombination rate
(c) Make silicon a direct gap semiconductor
(d) None of the above
7. In a forward-biased photo diode with increase in incident light intensity, the diode current:
(a) Increases
(b) Remains constant
(c) Decreases
(d) None of the above
8. The current through a $p-n$ junction diode with V volts applied to the $p$-region relative to the $n$-region (where $I_{o}$ is the reverse saturation current of the diode, $\eta$ the ideality factor, K the Boltzmann constant, $T$ the absolute temperature and $e$ the magnitude of charge on an electron) is:
(a) $\left(I_{0} \frac{-e V}{e^{m K T}-1}\right)$
(b) $I_{0}\left(1+e^{\frac{-e V}{m K T}}\right)$
(c) $I_{0}\left(1-e^{\frac{e V}{m K T}}\right)$
(d) $I_{0}\left[\exp \left(\frac{e V}{\eta K_{B} T}\right)-1\right]$
9. The varactor diode is:
(a) Voltage-dependent resistance
(b) Voltage-dependent capacitance
(c) Voltage-dependent inductor
(d) None of the above
10. The electric field in abrupt $p-n$ junction is:
(a) Linear function of distance
(b) Parabolic function of distance
(c) Independent of distance
(d) None of the above
11. In a linearly-graded $p-n$ junction the doping concentration:
(a) Changes abruptly at the junction
(b) Varies linearly with distance from junction
(c) Has a similar variation in junction capacitance with applied voltage
(d) (a), (b) and (c)
12. A $p-n$ junction, which is produced by recrystallisation on a base crystal, from a liquid phase of one or more components and the semiconductor is called:
(a) Doped junction (b)
(b) Alloy junction
(c) Fused junction
(d) None of these
13. Inanopencircuit $p-n j u n c t i o n$, theenergyband diagram of $n$-region shifts relative to that of p-diagram:
(a) Downward by $E_{0}$
(b) Upward by $E_{0}$
(c) Remains invariant
(d) Upward by $2 E_{0}$
14. The contact potential $V_{0}$ in a $p-n$ diode equals:
(a) $V_{T} \ln \frac{N_{A} N_{D}}{n_{i}^{2}}$
(b) $V_{T} \exp \left(\frac{n_{i}^{2}}{N_{A} N_{D}}\right)$
(c) $V_{T} \ln \frac{n_{i}^{2}}{N_{A} N_{D}}$
(d) $V_{T} \ln \left(N_{A} N_{D}\right)$
15. Each diode of full wave centre-tapped rectifier conducts for:
(a) $45^{\circ}$ only
(b) $180^{\circ}$ only
(c) $360^{\circ}$ complete period
(d) $270^{\circ}$ only
16. Bulk resistance of a diode is:
(a) The sum of resistance values of $n$-material and $p$-material
(b) The sum of half the resistance value of $n$-material and $p$-material
(c) Equivalent resistance of the resistance value of $p$ - and $n$-material is parallel
(d) None of the above
17. In unbiased $p-n$ junction, thickness of depletion layer is of the order of:
(a) $10^{-10} \mathrm{~m}$
(b) $50 \mu \mathrm{~m}$
(c) $0.5 \mu \mathrm{~m}$
(d) $0.005 \mu \mathrm{~m}$
18. In a diode circuit, the point where the diode starts conducting is known as:
(a) Cut-in point
(b) Cut-out point
(c) Knee point
(d) Cut-off point
19. A Zener diode should have:
(a) Heavily doped $p$ - and $n$-regions
(b) Lightly doped $p$ - and $n$-regions
(c) Narrow depletion region
(d) Both (a) and (c)
20. When a diode is forward-biased, the recombination of free electron and holes may produce:
(a) Heat
(b) Light
(c) Radiation
(d) All of the above
21. In a linear-graded junction, the width of the depletion layer varies as:
(a) $V_{j}$
(b) $V_{j}^{-2}$
(c) $3 \quad \sqrt{V_{j}}$
(d) None of the above
22. The transition capacitance in step-graded junction varies as:
(a) $C_{j} \alpha V_{R}^{3}$
(b) $C_{j} \alpha V_{R}^{-1 / 2}$
(c) $C_{j} \alpha V_{R}^{-1 / 3}$
(d) None of the above
23. The law of junction gives that in $p-n$ diode, the concentration of holes injected to $n$ region at the junction is given by:
(a) $n_{p o}{ }^{V / V T}$
(b) $n_{p o} \varepsilon^{-V / V T}$
(c) $p_{n o} \varepsilon^{8 / V T}$
(d) $p_{n o} \varepsilon^{-V / V T}$

Where $v$ is voltage applied at $p$ terminal relative to $n$ terminal, $n_{p o}$ and $P_{n o}$ are the thermal equilibrium concentration of electrons and holes in $p$ - and $n$-regions respectively.
24. In a forward-biased diode, with $N_{A} » N_{D}$, product of the diffusion capacitance $C_{D}$ and the dynamic diode resistance $r$ equals:
(a) $1 / \tau_{p}$
(b) $\tau_{p}$
(c) $\tau_{p}^{3}$
(d) $1 / \tau_{p}{ }^{3}$

Where $\tau_{p}$ is the lifetime of injected minoritycarrier holes.
25. In a forward-biased diode, with $N_{A} » N_{D}$, the following equation relates the diffusion current $I$, the injected excess minority carrier charge $Q$ and the file time of hole $\tau_{p}$ :
(a) $I=Q \tau_{p}$
(b) $I=Q^{2} / \tau_{P}$
(c) $I=Q / \tau_{P}$
(d) $I=\tau_{P}^{2}$
26. In a $p-n$ diode, for constant value of current at room temperature, $d_{v} / d_{t}$ varies approximately at the rate of:
(a) $-2.5 \mathrm{mV} /{ }^{\circ} \mathrm{C}$
(b) $-25 \mathrm{mV} /{ }^{\circ} \mathrm{C}$
(c) $2.5 \mathrm{mV} /{ }^{\circ} \mathrm{C}$
(d) $25 \mathrm{mV} /{ }^{\circ} \mathrm{C}$
27. Total space-charge neutrality is given by:
(a) $|Q|=e A N_{d} x_{n}=\frac{e}{A} N_{d} x_{p}$
(b) $|Q|=e A x_{n} / N_{d}=e A x_{p} / N_{D}$
(c) $|Q|=e A N_{d} x_{n}=e A N_{a} x_{p}$
(d) $|Q|=e A N_{d} x_{n}=e A N_{a} x_{p}^{2}$
28. Width of the depletion region in $p$-type is:
(a) $x_{p}=\left(\frac{2 \varepsilon}{e N_{a}} \frac{V_{T} N_{d}}{N_{d}-N_{a}}\right)^{\frac{1}{2}}$
(b) $x_{p}=\left(\frac{2 \varepsilon}{e N_{a}} \frac{V_{T} N_{d}}{N_{d}+N_{a}}\right)^{-\frac{1}{2}}$
(c) $x_{p}=\left(\frac{2 \varepsilon}{e N_{a}} \frac{V_{T} N_{d}}{N_{d}-N_{a}}\right)^{\frac{1}{2}}$
(d) $x_{p}=\left(\frac{2 \varepsilon}{e N_{a}} \frac{V_{T}}{N_{d}+N_{a}}\right)^{\frac{1}{2}}$
29. The width of the depletion region in $n$-type is given by:
(a) $x_{n}=\left(\frac{2 \varepsilon}{e N_{d}} \frac{V_{T} N_{d}}{N_{d}-N_{a}}\right)^{\frac{1}{2}}$
(b) $x_{n}=\left(\frac{2 \varepsilon}{e N_{d}} \frac{V_{T} N_{d}}{N_{a}+N_{d}}\right)^{\frac{1}{2}}$
(c) $x_{n}=\left(\frac{2 \varepsilon}{e} \frac{V_{T} N_{d}}{N_{a}+N_{d}}\right)^{\frac{1}{2}}$
(d) $x_{n}=\left(\begin{array}{ll}\frac{2 \varepsilon}{e N_{d}} & \frac{V_{T} N_{a}}{N_{a}-N_{d}}\end{array}\right)$
30. The reverse saturation current $I_{s}$ is given by:
(a) $I_{s} \equiv A J_{s} \equiv A e\left(\frac{D_{p}}{L_{p}}+\frac{D_{n}}{L_{n}}\right)$
(b) $I_{s} \equiv A J_{s} \equiv A \ln \left(\frac{D_{p} p_{n}}{L_{p}}-\frac{D_{n} n_{p}}{L_{n}}\right)$
(c) $I_{s} \equiv A J_{s} \equiv A\left(\frac{D_{p} p_{n}}{L_{p}}+\frac{D_{n} n_{p}}{L_{n}}\right)^{2}$
(d) $I_{s} \equiv A J_{s} \equiv A e\left(\frac{D_{p} p_{n}}{L_{p}}+\frac{D_{n} n_{p}}{L_{n}}\right)$

## REVIEW QUESTIONS

1. What is $p-n$ junction diode?
2. Explain process of formation $p-n$ junction diode.
3. What are the different natures of $p-n$ junction can be fabricated?
4. Draw the energy band diagram for an unbiased $p-n$ junction.
5. Why band bending occurs during the formation of a $p-n$ junction diode?
6. What is space charge? Write the properties of the junction.
7. For an unbiased $p-n$ junction sketch the variation of space-charge, electric field electrostatic potential and electron energy as function of distance across the junction.
8. What is the effect of doping on barrier potential?
9. Show that the Fermi level is invariant at thermal equilibrium.
10. Find out the expression of built in potential in terms of donor and accepter concentration.
11. What are basic difference between contact potential and built inpotential?
12. The barrier potential of a $p-n$ diode can not be measured with the help of voltmeter. Explain.
13. When a $p-n$ junction is said to be forwardbiased and reverse-biased? Explain with a figure.
14. Draw the energy band diagram for forwardbiased and reverse-biased $p-n$ junction diode.
15. What are an abrupt and a linearly-graded $p-n$ junction?
16. Draw and explain the I-V characteristics of $p-n$ junction.
17. Compare the $\mathrm{I}-\mathrm{V}$ characteristics of ideal and practical $p-n$ junction diode.
18. Compare cut-off voltage $\left(V_{\gamma}\right)$ of $\mathrm{Ge}, \mathrm{Si}$ and GaAs.
19. Derive the equation of $\mathrm{I}-\mathrm{V}$ characteristics of $p-n$ junction diode starting from continuity equation.
20. What is the origin of the reverse saturation current of a $p-n$ junction? Does the reverse saturation current change with the temperature and the applied reverse-bias?
21. Define and explain the dynamic or ac and static or dc resistance of $p-n$ diode. Do these resistances depend on temperature and biasing voltage?
22. Draw the linear piecewise model of $p-n$ junction.
23. What is junction capacitance and how it is formed in $p-n$ junction diode?
24. Find out the expressions of junction capacitance of $p-n$ junction diode.
25. Explain the working principle of varactor diode.
26. What is breakdown diode? Classify different types of breakdown diode.
27. Explain the working principle of Zener diode.
28. What is the difference between an ordinary semiconductor diode and a Zener diode?
29. Write down the use of Zener diode.
30. What is avalanche breakdown? How does avalanche multiplication occur?
31. What are the basic differences between Zener and avalanche breakdown?
32. Draw the V-I characteristics curves of Zener diode and Avalanche breakdown diode.
33. Compare the Zener breakdown between Si , Ge and GaAs.

## PRACTICE PROBLEMS

1. At a certain point in a certain junction at equilibrium, the electric field is $+8000 \mathrm{~V} / \mathrm{cm}$ and $n=10^{12} / \mathrm{cm}^{3}$.
(a) Calculate the density gradient for electrons at manager that point.
(b) Do the same for holes at that point.
2. A certain symmetric step $p-n$ junction has $N_{D}=10^{16} / \mathrm{cm}^{3}$ (donors only) on the left-hand side and $N_{A}=10^{16} / \mathrm{cm}^{3}$ (acceptors only) on the right-hand side. Using the depletion approximation, calculate, for equilibrium conditions,
(a) Contact potential $\Delta \psi_{0}$
(b) Depletion-layer thickness $X_{o}$ in $\mu \mathrm{m}$.
(c) Field at the junction $E_{O M}$ in kilovolts per centimetre.
3. For the junction of Problem 2, and continuing to use the depletion approximation, sketch dimensioned diagrams of:
(a) Charge-density profile
(b) Field profile
(c) Potential profile
4. Considering the spatial origin to be positioned at the metallurgical junction in the equilibrium sample of Problems 2 and 3:
(a) Calculate, the four current-density components at $x=0, J_{n \text {,drft }}, J_{p, \text { drftt }}, J_{n, \text { diff }}$ $J_{p, \text { diff }}$ using realistic carrier profiles, but
using $E_{O M}$ from the depletion approximation.
(b) Calculate both density-gradient values at $x=0$.
5. A certain asymmetric step junction has a doping on the left-hand side of $N_{1}=N_{D}-$ $N_{A}=10^{13} / \mathrm{cm}^{3}$ and on the right-hand side of $N_{2}=N_{A}-N_{D}=4 \times 10^{13} / \mathrm{cm}^{3}$. Using the depletion approximation, calculate, for the junction at equilibrium:
(a) Contact potential $\Delta \psi_{0}$
(b) Depletion-layer thickness $X_{o}$
(c) Electric field at the junction, $E_{O M}$
(d) Thickness of the depletion-layer portion on the $n$-type side, $X_{1}$
(e) Thickness of the depletion-layer portion on the $p$-type side, $X_{2}$
6. For the junction of Problem 5:
(a) Calculate the ratio $X_{1} / X_{2}$
(b) Explain why $\left(X_{1} / X_{2}\right)=\left(N_{2} / N_{1}\right)$
(c) Sketch a dimensioned diagram of the field profile.
(d) Calculate the potential drops $\Delta \psi_{1}$ and $\Delta \psi_{2}$ on the $n$-type and $p$-types sides, respectively.

7. Holes are being injected by a forward-biased junction under low level steady-state conditions at the left end of a long extrinsic- $n$-type silicon bar. In this problem you are only concerned with the $N$-region for $x>0$. The junction is several diffusion lengths to the left of the spatial origin, and $p_{N}{ }_{N}(0)$ is several times $p_{O N .}$ The total current density in the bar is $J$.
(a) Write an expression for $J(\infty)$, that is, current density where $x \gg L_{P}$. Make reasonable approximations.
(b) Given that $p^{\prime}{ }_{N}(x)=p^{\prime}{ }_{N}(0) e^{-x / L} p$, write an expression free of primed variables for the hole-density gradient as a function of $x$ for $x>0$.
(c) Write an expression for $J_{p \text {,diff }}(X)$ for $\mathrm{x}>$ 0.
(d) Write an expression for $J_{n \text {,diff }}(X)$ for $x>$ 0.
(e) Given that $J_{p, \text { diff }}(0)=0.092 J(\infty)$, find $E(0)$ in terms of $E(\infty)$.
8. You are given an $N^{+} P$ forward-biased junction.

The minority electron profile on the righthand side of the sample $n_{p}(x)$ versus $x$ is plotted above with reasonable accuracy using normalized linear coordinates. In the following diagram, the minority-carrier profiles on both sides of the junction are plotted using normalised semi log coordinates, with linear abscissa and logarithmic ordinate.

Given that $D_{n}=19.5 \mathrm{~cm}^{2} / \mathrm{s}$ on the right-hand side, find carrier lifetime on the $p$-type side.


9. Given the $N+P$ junction shown here with $N_{1}=10^{19} / \mathrm{cm}^{3}, N_{2}=10^{15} / \mathrm{cm}^{3}$, and $\tau_{2}=1 \mu \mathrm{~s}$ :

Side $1 \quad$ Side 2

(a) Find $J_{n}(0)$ for $V_{N p}=-0.04 \mathrm{~V}$.
(b) Find $J_{n}(0)$ for $V_{N p}=-0.4 \mathrm{~V}$.
(c) Repeat (a) and (b) with $\tau_{2}=100 \mu$ s and all else held constant.
(d) Repeat (a) and (b) with $N_{2}=10^{15} / \mathrm{cm}^{3}$ and all else held constant.
(e) Find $\Delta \psi$ for (a) and (b).
(f) Find an approximate value for $J_{n}(0)$ in b as a percentage of total current density $J$ in the sample, given $L_{p}=1 \mu \mathrm{~m}$ and $D_{p}=1.5 \mathrm{~cm}^{2} / \mathrm{s}$ in side 1 , and assuming negligible recombination in the spacecharge region.
(g) Assuming the junction to be ideal, find the reverse-current density for:

$$
V_{N P}=+100 \mathrm{~V},+10 \mathrm{~V},+1 \mathrm{~V}
$$

for the sample of (a) and (b).
10. Following is a reasonably accurate sketch of the numerical solution for an equilibrium symmetric step junction having $N=10^{13} /$ $\mathrm{cm}^{3}$.

(a) Estimate the maximum value of carrierdensity gradient displayed in the diagram without regard for algebraic sign.
(b) Calculate the maximum value of the current densities $\left|J_{n, \text { diff }}\right|=\left|J_{n \text {,drift }}\right|$ without regard for algebraic sign. Use $\mu_{\mathrm{n}}=700$ $\mathrm{cm}^{2} / \mathrm{Vs}$.
(c) Given that $X_{o}=0.16 \mu \mathrm{~m}$ (as can be confirmed on the sketch), calculate the maximum electric field in the junction, $E_{\text {OM }}$
(d) Calculate the value of the current densities $\left|J_{n \text {,diff(0) }}\right|=\left|J_{n \text {,drf(0) }}\right|$ without regard for algebraic sign.
(e) Inwhatapproximatefractionofthespace-charge-layer thickness does electric field exceed $50 \mathrm{kV} / \mathrm{cm}$, the value at which the drift velocity of electrons saturates at $107 \mathrm{~cm} / \mathrm{s}$ ?
(f) In view of your answer to part (e), what is the appropriate value of $\mu \mathrm{m}$ to use in solving part (d)? Explain.
11. A certain one-sided silicon step junction under bias exhibits the carrier profile.

(a) Find the magnitude and sign of the applied voltage $V_{N P}$. Use units in calculation.
(b) $V_{N p}$ is changed so that $n_{p}(0)=10^{8} / \mathrm{cm}^{3}$. Given that the total current density is $J=-4.19 \times 10^{-8} \mathrm{~A} / \mathrm{cm}^{2}$, find the minority-carrier diffusion length $L_{n}$ in $\mu \mathrm{m}$ for the $p$-type region. Use units in calculation.
(c) The sample of (a) is replaced by another ofidenticaldopingthatexhibitsminoritycarrier diffusion length of $L_{n}=2 \mathrm{~mm}$. Find the carrier lifetime $\tau$ in $\mu$ s for the $p$-type region of the new sample. Use units in calculation.
12. A silicon sample at equilibrium contains an asymmetric step junction. Shown here is a portion of its field profile that is based upon the depletion approximation.
(a) With the help of Poisson's equation, derive an expression for net doping on the left-hand side. Put your final expression in terms of only symbols given in the diagram and the right-hand side of Poisson's equation.
(b) Determine the potential drop on the $n$-type side of the junction. Calculate numerical value and units.


13. This $N+P$ junction is under a bias of $V_{N P}=-k T / q$. In the $p$-type region, it has the values $D_{n}=22 \mathrm{~cm}^{2} / \mathrm{s}$ and $T=2 \mu \mathrm{~s}$. The law of the junction is not very accurate at such a low bias, but for purposes of this problem, assumes that it is accurate. The value of $n_{o p}$ is $10^{6} / \mathrm{cm}^{3}$.
(a) Calculate at the origin the slope of $n_{p}$. Give the correct units and algebraic sign along with the numerical value.

(b) Using a solid line, sketch $n_{p}(x)$ for $x>$ 0.
(c) Calculate $Q^{\prime}$, the excess-electron charge stored in the $p$-type region. The cross section of the sample is square, $1 \mathrm{~mm} \times 1$ mm . Give units.
14. To analyse this one-sided step junction at equilibrium:

(i) Use the depletion approximation
(ii) Neglect potential drop on the $p+-$ side
(iii) Neglect depletion-layer penetration on the $p+-$ side
(iv) Include units in all necessary calculations
The properties of the sample are these: On the left-hand side, $\left(N_{D}-N_{A}\right)=N_{1}=10^{15} / \mathrm{cm}^{3}$; on the right-hand side, $\left(N_{A}-N_{D}\right)=N_{2}$; the deple-tion-layer dimension $X_{1}=X_{0}=0.5 \mu \mathrm{~m} ; E=$ $12 \mathrm{pF} / \mathrm{cm} ;(\mathrm{k} T / q)=0.06566 \mathrm{~V}$; and finally

$$
\psi(x)=\frac{q N_{1}}{\varepsilon}\left(\frac{x^{2}}{2}+X_{0} x\right)
$$

(a) Sketch $\psi(x)$ versus $x$ on the upper axis pair. Label the axis.
(b) Derive an expression for $E(x)$ versus $x$
(c) Use your expression to calculate $E\left(-X_{0}\right)$, and $E(0)$ in terms of $X_{0}$
(d) Plot $E(x)$ in the space provided
(e) Derive an expression for $\Delta \psi_{0}$
(f) Calculate $\Delta \psi_{0}$
(g) Derive an expression for $E_{O M}$ in terms of $\Delta \psi_{0}$
(h) Calculate $E_{O M}$ in $\mathrm{kV} / \mathrm{cm}$
(i) Given $\Delta \psi_{0}=(k T / \mathrm{q}) \ln \left(N_{1} N_{2} / n_{i}^{2}\right)$, find $\mathrm{N}_{2}$
15. Following is a one-sided junction sample having an extensive $p$-type region and a cross-sectional area of $10^{-3} \mathrm{~cm}^{2}$. It is subjected to a steady-state forward-bias. Calculate the number of excess minority-carriers stored in the $p$-type region.

16. Given this symmetric step junction at equilibrium with a net doping on each side of $10^{16} / \mathrm{cm}^{3}$, perform approximate calculations, estimating where necessary.
(a) Calculate $\Delta \psi_{0}$
(b) Calculate $X_{0}$
(c) Calculate $E_{O M}$
(d) Estimate the value of maximum hole gradient.
(e) Compute the approximate value of $J_{p, \text { diff }}$ there.

(f) What is the value of $J_{p, \mathrm{drft}}$ there?
(g) Is $J_{p, \text { drft }}$ higher or lower at $x=0$ ?
(h) Calculate $E=E_{O M}$ there; why doesn't $J_{p, \text { drft }}$ peak at $x=0$ ?
(i) Calculate $J_{p, \mathrm{drft}}$ at $x=0$
17. A single-crystal silicon sample has a thin ideally intrinsic region flanked by heavily doped $n$-type and $p$-type regions, forming a PIN (or NIP) junction. It is not a step junction.
(a) Considering that there is sufficient space charge in the given sample to launch and terminate four lines of force when the sample is at equilibrium, sketch these lines in the top diagram, using arrowheads to indicate direction.
(b) Sketch and dimension the approximate field profile in the space provided, given $\Delta \psi_{0}=2.0 \mathrm{~V}$.
(c) Sketch and dimension the equilibrium potential profile in the space provided, taking the potential of the $p+$ region as reference. Your sketch should show potential throughout the entire device, from $x=0$ to $x=30 \mu \mathrm{~m}$.

(d) Sketch the equilibrium band diagram for this sample, letting $\psi_{G}=1.1 \mathrm{~V}$. Show the Fermi level $\varnothing$.
(e) Assuming the two extrinsic regions have equal net-doping magnitudes, calculate net-doping density approximately.
(f) Calculate the magnitude and sign of applied voltage $V_{N P}$ required to produce a maximum field of $E_{M}=4 \mathrm{kV} / \mathrm{cm}$ in this junction.
18. Write a completely general expression for volumetric space-charge density $p_{v}(x)$ at equilibrium in a region with arbitrary doping profiles $N_{D}(x)$ and $N_{A}(x)$.
19. Given the depletion approximation for an equilibrium step junction of arbitrary doping, one can specify the junction completely by specifying two of its independent variables. With the well known six variables demonstrate the validity of this assertion.
(a) By writing four independent equations in the six variables.
(b) By writing three independent equations in the first five variables.
(c) By writing two independent equations in the first four variables.
(d) By writing one equation in the first three variables.
20. You are given an ideal silicon junction having a saturation current of $I_{0}=10^{-14} \mathrm{~A}$, and carrying a forward current of $1 \mu \mathrm{~A}$.
(a) Assuming a reverse resistance of $R=\infty$, compute values for a piece-wise-linear model of the junction.
(b) Sketch and dimension the resulting I-V characteristic.
(c) Repeat part a for $I=1.5 \mathrm{~A}$
(d) Repeat part b for $I=1.5 \mathrm{~A}$
21. A $p^{+} n$ junction diode with a junction area of $1 \mathrm{~mm}^{2}$ has a charge of $10^{-6} \mathrm{C}$ of excess holes stored in it when it carries a current of 49 mA . Compute the minority-carrier diffusion length in the $n$-type region.
22. An abrupt GaAs $p-n$ diode has $N_{a}=10^{16} \mathrm{~cm}^{-3}$ and $N_{d}=10^{15} \mathrm{~cm}^{-3}$. Calculate the Fermi level positions at 300 K in the $p$ - and $n$-regions.
23. Consider the sample discussed in Problem 22. The diode has a diameter of $25 \mu \mathrm{~m}$. Calculate the depletion widths in the $n$ and $p$-regions. Also calculate the charge in the depletion regions and plot the electric field profile in the diode.
24. An abrupt silicon $p-n$ diode at 300 K has a doping of $N_{a}=10^{18} \mathrm{~cm}^{-3}, N_{d}=10^{13} \mathrm{~cm}^{-3}$. Calculate the built-in potential and the depletion widths in the $n$ - and $p$-regions.
25. AGe $p-n$ diode has $N_{a}=5 \times 10^{17} \mathrm{~cm}^{-3}$ and $N_{d}=10^{17} \mathrm{~cm}^{-3}$. Calculate the built-in voltage at 300 K . At what temperature does the built in voltage decrease by 2 per cent?
26. The diode of Problem 25 is subjected to bias values of:
(i) $V_{f}=0.1 \mathrm{~V}$
(ii) $V_{f}=1.5 \mathrm{~V}$
(iii) $v_{f}=1.9 \mathrm{~V}$
(iv) $v_{f}=5.0 \mathrm{~V}$. Calculate the depletion widths and the maximum field $F_{m}$ under these biases.
27. Consider a $p+n$ Si diode with $N_{a}=10^{18} \mathrm{~cm}^{-3}$ and $N_{d}=10^{16} \mathrm{~cm}^{-3}$. The hole diffusion coefficient in the $n$-side is $10 \mathrm{~cm}^{2} / \mathrm{s}$ and $\tau_{p}=10^{-7}$ s . The device area is $10^{-4} \mathrm{~cm}^{2}$. Calculate the reverse saturation current and the forward current at a forward bias of 0.4 V at 300 K .
28. Considera $p+n$ silicondiodewitharea $10^{-4} \mathrm{~cm}^{2}$. The doping is given by $N_{a}=10^{18} \mathrm{~cm}^{-3}$ and $N_{d}=$ $10^{17} \mathrm{~cm}^{-3}$. Plot the 300 K values of the electron and hole currents $I_{n}$ and $I_{p}$ at a forward-bias of 0.4 V . Assume $\tau_{\mathrm{n}}=\tau_{\mathrm{p}}=1 \mu \mathrm{~s}$ and neglect recombination effects. $D_{n}=20 \mathrm{~cm}^{2} / \mathrm{s}$; and $D_{p}=20 \mathrm{~cm}^{2} / \mathrm{s}$.
29. A GaAs LED has a doping profile of $N_{a}=$ $10^{17} \mathrm{~cm}^{-3}, N_{d}=10^{18} \mathrm{~cm}^{-3}$ at 300 K . The minority carrier time is $\tau_{\mathrm{n}}=10^{-8} \mathrm{~s} ; \tau_{\mathrm{p}}=5 \times$ $10^{-9} \mathrm{~s}$. The electron diffusion coefficient is $150 \mathrm{~cm}^{2} \mathrm{~s}^{-1}$ while that of the holes is $20 \mathrm{~cm}^{2}$ $\mathrm{s}^{-1}$. Calculate the ratio of the electron injected current to the total current.
30. The diffusion capacitance of a wide base diode is greater than that of a narrow base diode. Show that the ratio of the diffusion capacitances of such diodes with heavily doped $p$-regions is $3 \tau_{p} / 4 \tau_{B}$.
31. Consider a GaAs $p-n$ diode with a doping profile of $N_{a}=10^{16} \mathrm{~cm}^{-3}, N_{d}=10^{16} \mathrm{~cm}^{-3}$ at 300 K . The minority carrier lifetimes are $\tau_{\mathrm{n}}=10^{-7} \mathrm{~s} ; \tau_{\mathrm{p}}=10^{-8} \mathrm{~s}$. The electron and hole diffusion coefficients are $150 \mathrm{~cm}^{2} / \mathrm{s}$ and 24 $\mathrm{cm}^{2} / \mathrm{s}$, respectively. Calculate and plot the minority carrier current density in the neutral $n$ - and $p$-regions at a forward-bias of 1.0 V .
32. Consider a $p-n$ diode made from InAs at 300 K . The doping is $N_{a}=10^{17} \mathrm{~cm}^{-3}=N_{d}$. Calculate the saturation current density if the electron and hole density of states masses are 0.02 $\mathrm{m}_{0}$ and $0.4 \mathrm{~m}_{0}$, respectively. Compare this value with that of a silicon $p-n$ diode doped at the same levels. The diffusion coefficients are $D_{n}=800 \mathrm{~cm}^{2} / \mathrm{s} ; D_{p}=30 \mathrm{~cm}^{2} / \mathrm{s}$. The carrier
lifetimes are $\tau_{\mathrm{n}}=\tau_{\mathrm{p}}=10^{-8} \mathrm{~s}$ for InAs. For the silicon diode use the values $D_{n}=30 \mathrm{~cm}^{2} / \mathrm{s}$; $D_{p}=20 \mathrm{~cm}^{2} / \mathrm{s} ; \tau_{\mathrm{n}}=\tau_{\mathrm{p}}=10^{-7} \mathrm{~s}$.
33. Consider a $p-n$ diode in which the doping is linearly graded. The doping is given by:

$$
N_{d}-N_{a}=G x
$$

so that the doping is $p$-type at $x<0$ and $n$-type at $x>0$. Show that the electric field profile is given by:

$$
F(x)=\frac{e}{2 \varepsilon} G\left[x^{2}-\left(\frac{w}{2}\right)^{2}\right]
$$

where, $w$ is the depletion width given by:

$$
W=\left[\frac{12 \varepsilon \mathrm{H}(V b i-V)}{e G}\right]^{1 / 3}
$$

34. A silicon diode is being used as a thermometer by operating it at a fixed forward bias current. The voltage is then a measure of the temperature. At 300 K , the diode voltage is found to be 0.7 V . How much will the voltage change if the temperature changes by 1 K ?
35. Consider a GaAs $p-n$ diode with $N_{a}=10^{17}$ $\mathrm{cm}^{-3}, N_{d}=10^{17} \mathrm{~cm}^{-3}$. The diode area is $10^{-3}$ $\mathrm{cm}^{2}$ and the minority carrier mobilities are (at 300 K ) $\mu_{n}=3000 \mathrm{~cm}^{2} / \mathrm{V}-\mathrm{s} ; \mu_{p}=200$ $\mathrm{cm}^{2} / \mathrm{V}-\mathrm{s}$. The electron-hole recombination times are $10^{-8} \mathrm{~s}$. Calculate the diode current at a reverse-bias of 5 V .
36. A long base GaAs abrupt $p-n$ junction diode has an area of $10^{-3} \mathrm{~cm}^{2}, N_{a}=10^{18} \mathrm{~cm}^{-3}$, $N_{d}=10^{17} \mathrm{~cm}^{-3}, \tau_{\mathrm{p}}=\tau_{\mathrm{n}}=10^{-8} \mathrm{~S}, D_{p}=6 \mathrm{~cm}^{2}$ $\mathrm{s}^{-1}$ and $D_{n}=100 \mathrm{~cm}^{2} \mathrm{~s}^{-1}$. Calculate the 300 K diode current at a forward bias of 0.3 V and a reverse bias of 5 V . The electron-hole recombination time in the depletion regions is $10^{-7} \mathrm{~s}$.
37. The critical field for breakdown of silicon is $4 \times 105 \mathrm{~V} / \mathrm{cm}$. Calculate the $n$-side doping of an abrupt $p+n$ diode that allows one to have a breakdown voltage of 29 V .
38. What is the width of the potential barrier seen by electrons during band to band tun-
neling in an applied field of $5 \times 10^{5} \mathrm{~V} / \mathrm{cm}$ in $\mathrm{GaAs}, \mathrm{Si}$ and $\mathrm{In}_{0.53} \mathrm{Ga}_{0.47} \mathrm{As}\left(E_{g}=0.8 \mathrm{~V}\right)$ ?
39. If the electron effective mass is $0.5 \mathrm{~m}_{0}$, and the semiconductor band gap is 1.0 eV , at what applied field does the tunneling probability become $10^{-11}$ ?
40. Consider a Si $p-n$ diode with $N_{a}=10^{18} \mathrm{~cm}^{-3}$ and $N_{d}=10^{18} \mathrm{~cm}^{-3}$. Assume that the diode will break down by Zener tunneling if the peak field reaches $10^{6} \mathrm{~V} / \mathrm{cm}$. Calculate the reverse bias at which the diode will break down.
41. A $p+-n$ silicon diode has an area of $10^{-2}$ $\mathrm{cm}^{2}$. The measured junction capacitance (at 300 K ) is given by:

$$
\frac{1}{C^{2}}=5 \times 10^{8}(2.5-4 \mathrm{~V})
$$

in which C is in units of $\mu \mathrm{F}$ and $V$ is in volts. Calculate the built-in voltage and the depletion width at zero bias. What are the dopant concentrations of the diode?
42. In a long base $n+p$ diode, the slope of the $C_{\text {diff }}$ versus $I_{F}$ plot is $1.6 \times 10^{-5} \mathrm{~F} / \mathrm{A}$. Calculate the electron lifetime, the stored charge, and the value of the diffusion capacitance at $I_{F}=2 \mathrm{~mA}$.
43. Consider a Si $p+n$ diode with a long base. The diode is forward-biased (at 300 K ) at a current of 2 mA . The hole lifetime in the $n$-region is $10^{-7} \mathrm{~s}$. Assume that the depletion capacitance is negligible and calculate the diode impedance at the frequency of $100 \mathrm{KHz}, 100 \mathrm{MHz}$ and 500 MHz .
44. Consider a diode with the junction capacitance of 16 pF at zero applied bias and 4 pF at full reverse bias. The minority carrier time is $2 \times 10^{-8} \mathrm{~s}$. if the diode is switched from a state of forward bias with current of 2.0 mA to a reverse bias voltage of 10 V applied through a 5 Kohm resistance, estimate the response time of the transient.
45. What is the differential resistance of a diode at zero bias?
46. Assume a $p-n$ diode with a heavily doped $p$-region. Show that the concentration of excess holes is proportional to the forward current either in a wide or a narrow $n$ region.
47. Derive the built-in potential of a junction for heavy doping, $N_{A}$ on the $p$-side and near intrinsic doping on the $n$-side.
48. When the junction capacitance is plotted against the applied reverse voltage on log-
$\log$ graph paper, a straight line results for $V_{a} \gg V_{b}$. What is the slope of this line?
49. For a $p+n$ diode $\mu_{p}=450 \mathrm{~cm}^{2} / \mathrm{Vs}$ and $\tau_{p}=1$ $\mu s$ in the $n$-region. Calculate the widths of the $n$-region for which: (a) $W_{n} \leq 0.1 L_{p}$ and (b) $W_{n}$ $\geq 4 L_{p}$.
50. How can you connect two Zener diodes, 6 V and 4 V to obtain a reference of 10 V , if the supply voltage is 15 V and the load resistance is variable? The minimum current for each Zener diode is 1 mA and the wattage of each diode is 0.5 Watts.

## SUGGESTED READINGS

1. Shockley, W. 1949. "The Theory of $p-n$ Junctions in Semiconductors and $p-n$ Junction Transistors". Bell System Technical Journal. Vol. 28: 435-89.
2. Shockley, W. and W. T. Read Jr. 1952. "Statistics of the Recombination of Holes and Electrons". Physical Review. Vol. 87: 835-42.
3. Mou, J. N. 1958. "The Evolution of the Theory of the Voltage Current Characteristic of $p-n$ Junctions". Proceedings of the IRE: 1076-82.

## 3

## Diode Circuits

## Outline

3-1 Introduction
3-2 Analysis of Diode Circuits
3-3 Load Line and Q-point
3-4 Zener Diode as Voltage Regulator
3-5 Rectifiers

## 3-6 Clipper and Clamper Circuits

## 3-7 Comparators

3-8 Additional Diode Circuits
3-9 Special Types of $p-n$ Junction
Semiconductor Diodes
3-10 Applications of Diode

## Objectives

This chapter analyses diode circuits and load line with the $Q$-point concept. The formulation of the diode as a voltage regulator, half-wave rectifier, and full-wave rectifier along with bridge rectification and performance analysis of rectifier circuits will be dealt with in detail. This is followed by a derivation of peak inverse voltage, dc voltage and current, ripple factor, and efficiency. Clipper and clamper circuits, comparators, and additional diode circuits will also be analysed. The degenerate semiconductors that were the first to enjoy device applications through tunnel diodes, the first element to produce negative resistance in microwaves, have also been discussed. The chapter ends with an examination of optoelectronic devices like light-emitting diode, photo detector diode, etc.

## 3-1 INTRODUCTION

In the field of electronics, the simplest and the most fundamental non-linear circuit element is the diode. The $p-n$ junction diode is considered to be a circuit element. For easy and lucid evaluation of the diode element, the concept of load line is extremely important. Among the many applications of diodes, their use in the design of rectifiers, which convert ac to dc, is the most common. The piecewise linear model is used in certain applications of diodes, namely clippers, rectifiers and comparators. Many more such circuits are possible with one or more diodes being implemented in them.

## 3-2 ANALYSIS OF DIODE CIRCUITS

The basic diode circuit consists of a voltage source in series with a resistor and a diode. The circuit might be analysed properly to obtain the instantaneous current and diode voltage. For such an analysis to be done, the concept of load line and its effective use in various circuits has to be thoroughly understood. The concept of load line is absolutely essential.

## 3-3 LOAD LINE AND Q-POINT

The applied load will normally have an impact on the region (or point) of operation of a device. If the analysis is performed in a graphical manner, a line can be drawn on the characteristics of the device to represent the applied load. The intersection of the load line with the characteristics will determine the point of operation of the system. Physically, this point of operation mainly determines the conditions under which the device is to be operated in a circuit. This case takes care of the various intriguing attributes of the circuit. This kind of an analysis is known as the load-line analysis. We will discuss the concept of load line from all practical points of view. An example has been shown in Figure 3-1(a) and Figure 3-1(b).

Let us consider the network and its characteristics as given in Figure 3-1(a). The voltage established by the battery $E$ is to generate a current through the series resistor $R$ of the circuit in the clockwise direction. The fact that this current and the defined direction of conduction of the diode are the same reveals that the diode is in the ON state, i.e., the diode is forward-biased and consequently, the forward resistance of the diode is very low. Under normal conditions, this resistance is approximately $10 \Omega$. Applying Kirchoff's voltage law (KVL) of circuit theory, to the series circuit of Figure 3-1(a), we obtain:

$$
\begin{gather*}
E-V_{D}-V_{R}=0  \tag{3-1}\\
E=V_{D}+I_{D} R \tag{3-2}
\end{gather*}
$$

The intersection of the load line with the curve of current-voltage characteristics under forward-biased


Figure 3-1(a) Analysis of a basic diode circuit


Figure 3-1(b) I-V characteristics of the diode conditions easily implicates the conditions of operation of the device in the circuit.

If $V_{D}=0 \mathrm{~V}$, we can calculate $I_{D}$ and plot the magnitude of $I_{D}$ on the vertical axis.
As $V_{D}=0 \mathrm{~V}$, Equation (3-2) is modified as:

$$
\begin{align*}
E & =V_{D}+I_{D} R \\
& =0 \mathrm{~V}+I_{D} R \\
& I_{D}=\left.\frac{E}{R}\right|_{V_{D}=0 \mathrm{~V}} \tag{3-3}
\end{align*}
$$

If $I_{D}=0 \mathrm{~A}$, we can calculate $V_{D}$ and plot the magnitude of $V_{D}$ on the horizontal axis.
As $I_{D}=0$ A, Equation (3-2) is modified as:

$$
\begin{aligned}
& E=V_{D}+I_{D} R \\
&=V_{D}+(0 \mathrm{~A}) R
\end{aligned}
$$

$V_{D}=\left.E\right|_{I_{D}=0 \mathrm{~A}}$
A straight line drawn between two points will define the load line, as shown in Figure 3-2(a).

If the value of $R$ is changed, the intersection on the vertical axis will change. This affects the slope of the load line, and gives a different point of intersection between the load line and the device characteristics. The point of intersection between the device characteristics and the load line $\left(V_{D_{0}}, I_{D_{0}}\right)$ is called the point of operation or the quiescent point ( $Q$-point) as defined by a dc network.

From the circuit diagram given in Figure 3-1(a) it can be seen that the voltage drop across the diode is given by:

$$
\begin{equation*}
V_{D}=E-V_{L} \tag{3-5}
\end{equation*}
$$

or, $\quad V_{D}=E-i_{D} R_{L}$
where, $V$ is the supply voltage, $V_{L}$ is the voltage across the load, and $I_{a}$ is the current flowing through the diode.

Equation (3-5) gives a relation between the voltage across the diode and the current flowing through it. It can be seen that this equation is an equation of a straight line. The load line and the static characteristic curve of the diode intersect at the quiescent point. The coordinates of the $Q$-point are $v_{Q}, i_{Q}$. The point is as shown in Figure 3-3(a). Again, if the value of the


Figure 3-3(a) Change of Q-point with changes in supply voltage and load

(b)

Figure 3-3(b) Reverse-biased diode circuit
voltage source is changed, another point on the static characteristic of the diode is obtained. The coordinates of the new point are $Q^{\prime}\left(v_{Q}{ }^{\prime}, i_{Q}{ }^{\prime}\right)$.

If the diode currents $i_{Q}$ and $i_{Q}{ }^{\prime}$ are plotted vertically above the corresponding supply voltages, two distinct points are obtained- $B$ and $B^{\prime}$. The curve passing through these two points is known as the dynamic load line. Dynamic load line can be obtained for different load resistances. This dynamic load line is important, because with the help of this, for any given input voltage, the diode current can be obtained directly from the graph. The load-line concept is important in reverse biasing.

Figure 3-3(b) depicts the diode circuit under the reversed condition. The forward-biased parameters over here are $I_{D}$ (diode current) and $V_{D}$ (voltage). It can be written with the application of Kirchoff's voltage law, $V_{P S}=I_{P S} R-V_{D}=-I_{D} R-V_{D}$ (where, $I_{D}=-I_{P S}$ ).

The equation, $V_{P S}=I_{P S} R-V_{D}=-I_{D} R-V_{D}$, characterizes the load line.

For the first end point, putting $I_{D}=0$ :

$$
V_{D}=-V_{P S}=-6 \mathrm{~V}
$$

For the second end point, putting $I_{D}=0$ :

$$
I_{D}=\frac{-V_{P S}}{R}=-\frac{6}{3}=-2 \mathrm{~mA}
$$


(c)

Figure 3-3(c) Load line

Figure 3-3(c) depicts the plot of diode characteristics and load line. The reverse-biased condition of the diode is demonstrated by the fact that the load intersects the diode characteristics curve in the third quadrant at $V_{D}=-6 \mathrm{~V}$ and $I_{D}=0$.

## 3-4 ZENER DIODE AS VOLTAGE REGULATOR

A Zener diode can be used as a voltage regulator because it maintains a constant output voltage even though the current passing through it changes. It is generally used at the output of an unregulated power supply to provide a constant output voltage free of ripple components.

The circuit diagram of a voltage regulator is shown in Figure 3-4. The circuit consists of a current limiting resistor $R_{S}$ and a Zener diode connected in parallel with the load resistance $R_{L}$. The diode is selected in such a way that its breakdown voltage is equal to the desired regulating output.

For proper voltage regulation, the voltage of an unregulated power supply must be greater than the Zener voltage of the diode selected. The diode does not conduct current when the input voltage is less than the Zener voltage. The value of $R_{S}$ is chosen to ensure that the diode initially operates in the breakdown region under the Zener voltage across it. The function of the regulator is to keep the output voltage nearly constant with changes in $V_{\text {in }}$ or $I_{L}$.

The operation is based on the fact that in the Zener breakdown region small changes in the diode voltage are accompanied by large changes in the diode current. The large currents flowing through $R_{S}$ produce voltages that compensate for the changes in $V_{\text {in }}$ or $I_{L}$. The relation gives the input current:

$$
\begin{equation*}
I=\frac{V_{\mathrm{in}}-V_{Z}}{R_{S}}=I_{Z}+I_{L} \tag{3-6}
\end{equation*}
$$



Figure 3-4 Zener regulation of a variable input voltage

There are two types of regulation:
(i) Regulation with varying input voltage, also known as line regulation
(ii) Regulation with varying load resistance, also known as load regulation

## 3-4-1 Line Regulation

When the input voltage is more than $V_{Z}$, the Zener diode conducts. With a further increase in $V_{\text {in }}$, the input current $I$ will also increase. This increases the current through the Zener diode without affecting the load current $I_{L}$. The limitations on the input-voltage variations are set by the minimum and maximum current values ( $I_{Z K}$ and $I_{Z M}$ ) within which the Zener diode can operate.

The increase in the input current $I$ will also increase the voltage drop across series resistance $R_{S}$, thereby keeping the output voltage constant. If the input voltage decreases, the input current through the Zener diode will also decrease. Consequently, the voltage drop across the series resistance will be reduced. Thus, the output voltage and the load current remain constant.

For fixed values of $R_{L}$ (see Figure 3-4), the voltage $V_{i}$ must be sufficiently large to turn the Zener diode on. The turn-on voltage is determined by $V_{L}$ and $V_{i_{\text {min }}}$ as:

$$
\begin{gather*}
V_{L}=V_{Z}=\frac{R_{L} V_{i}}{R_{L}+R_{S}}  \tag{3-7a}\\
V_{i_{\min }}=\frac{\left(R_{L}+R_{S}\right) V_{Z}}{R_{L}} \tag{3-7b}
\end{gather*}
$$

The maximum value of $V_{i}$ is limited by the maximum Zener current $I_{Z M}$.
We have:

$$
\begin{align*}
I_{Z M} & =I_{R}-I_{L}  \tag{3-8}\\
I_{R \max } & =I_{Z M}+I_{L} \tag{3-9}
\end{align*}
$$

As $I_{L}$ is fixed at $V_{Z} / R_{L}$, and $I_{Z M}$ is the maximum value of $I_{Z}$, the maximum $V_{i}$ is given by:

$$
\begin{equation*}
V_{i_{\max }}=V_{R_{s_{\max }}}+V_{Z} \tag{3-10}
\end{equation*}
$$



Figure 3-5(a) Output voltage vs. input voltage for line regulation


Figure 3-5(b) Load regulation showing the variation of load voltage $V_{L}$ and $R_{L}$ taking $V_{i}$ as constant

$$
\begin{equation*}
V_{i_{\max }}=I_{R_{\max }} R_{s}+V_{Z} \tag{3-11}
\end{equation*}
$$

Figure 3-5(a) shows a plot of $V_{o}$ versus $V_{i}$ for line regulation. It is observed from the graph that the output voltage $V_{o}$ remains constant when the diode is in the Zener region, i.e., when the stipulated current is flowing. This is called input or line regulation.

## 3-4-2 Load Regulation: Regulation with Varying Load Resistance

In this case, the input voltage, $V_{\text {in }}>V_{z}$, is kept fixed and the load resistance, $R_{L}$, is varied. The variation of $R_{L}$ changes the current $I_{L}$ through it, thereby changing the output voltage. When the load resistance decreases, the current through it increases. This ultimately causes a decrease in the Zener current. As a result, the input current and the voltage drop across $R_{S}$ remains constant. And the output voltage is also kept constant, as shown in Figure 3-5(b). On the other hand, if the load resistance increases, the load current decreases. As a result, the Zener current $I_{Z}$ increases. This again keeps the value of input current and voltage drop across the series resistance constant. Thus, the output voltage remains constant. This is called load regulation.

Due to the offset voltage $V_{Z}$, there is a specific range of resistor values, which will ensure that the Zener is in the ON state. Too small a load resistance, $R_{L}$, will result in a voltage, $V_{L}$, across the load resistor to be less than $V_{Z}$, and the Zener device will be in the OFF state, which is usually not required in this kind of operation.

To determine the minimum load resistance which will turn the Zener diode on, simply remove the Zener diode, as shown in Figure 3-6, and calculate the value of $R_{L}$ that will result in a load voltage $V_{L}=V_{Z}$.

That is:

$$
\begin{equation*}
V_{L}=V_{Z}=\frac{R_{L} V_{i}}{R_{L}+R_{S}} \tag{3-12}
\end{equation*}
$$



Figure 3-6 Diode as a voltage regulator


Figure 3-7 Analytical circuit of Zener diode being used as a regulator

$$
\begin{align*}
& R_{L} V_{Z}+V_{Z} R_{S}=R_{L} V_{i} \\
& R_{L}\left(V_{i}-V_{Z}\right)=R_{S} V_{Z} \\
& R_{L}=\frac{R_{S} V_{Z}}{V_{i}-V_{Z}} \tag{3-13}
\end{align*}
$$

From the voltage-divider rule and solving for $R_{L}$, we have:

$$
\begin{equation*}
R_{L_{\min }}=\frac{R_{S} V_{Z}}{V_{i}-V_{Z}} \tag{3-14}
\end{equation*}
$$

Any resistance with a value greater than the $R_{L}$ will ensure that the Zener diode is in the ON state and the diode can be replaced by its $V_{Z}$ source equivalent, as shown in Figure 3-7.

The condition defined by Equation (3-14) establishes the minimum $R_{L}$, but the maximum $I_{L}$ is:

$$
\begin{equation*}
I_{L_{\max }}=\frac{V_{L}}{R_{L}}=\frac{V_{Z}}{R_{L_{\min }}} \tag{3-15}
\end{equation*}
$$

Once the diode is in the ON state, the voltage across $R_{S}$ will remain fixed at:

$$
\begin{equation*}
V_{R_{S}}=V_{i}-V_{Z} \tag{3-16}
\end{equation*}
$$

And $I_{R}$ remains fixed at:

$$
\begin{align*}
I_{R_{S}} & =\frac{V_{R_{S}}}{R_{S}}  \tag{3-17}\\
I_{Z} & =I_{R}-I_{L} \tag{3-18}
\end{align*}
$$

This will result in a minimum $I_{Z}$ when $I_{L}$ is a maximum; and a maximum $I_{Z}$ when $I_{L}$ is a minimum value ( $I_{R}$ is constant). Since $I_{Z}$ is limited to $I_{Z M}$, it does affect the range of $R_{L}$, and therefore, $I_{L}$.

Substituting $I_{Z M}$ for $I_{Z}$ establishes the minimum $I_{L}$ as:

$$
\begin{equation*}
I_{L_{\min }}=I_{R_{S}}-I_{Z M} \tag{3-19}
\end{equation*}
$$

and the maximum load resistance as:

$$
\begin{equation*}
R_{L_{\max }}=\frac{V_{\mathrm{Z}}}{I_{L_{\min }}} \tag{3-20}
\end{equation*}
$$

Thus, load resistance can be calculated by using Equations (3-14) and (3-20).

## Solved Examples

Example 3-1 A p-n germanium junction at room temperature has a reverse saturation current of $10 \mu \mathrm{~A}$, negligible ohmic resistance, and a Zener breakdown voltage of 100 V . A 1.5 K resistor is in series with this diode, and a 45 V battery is impressed across this combination.
(a) Find the current if the diode is forward-biased.
(b) Find the current if the battery is inserted into the circuit with reverse polarity.
(c) Repeat part (a) and (b) if the Zener breakdown voltage is 10 V with 1 K resistor and 30 V battery.

Solution:
(a) The solution can be found graphically by plotting the diode characteristics and drawing the load line. Using the method of successive approximation, we have with us, diode drop equal to zero, in essence neglecting the diode threshold voltage.

3-8 | Basic Electronics

$$
I=\frac{45}{1.5 \mathrm{~K}}=30 \mathrm{~mA}
$$

For this current, $V$ is given by:
or,

$$
\begin{gathered}
30 \times 10^{-3}=10 \times 10^{-6}\left(e^{38.4 \mathrm{~V}}-1\right) \\
e^{38.4 \mathrm{~V}}=3000 \text { and } \quad V=0.208 \mathrm{~V} \\
I=\frac{45-0.208}{1.5 \mathrm{~K}} \approx 29.8 \mathrm{~mA}
\end{gathered}
$$

Hence,
For this current, $V=0.2 \mathrm{~V}$

$$
\therefore \quad I=29.8 \mathrm{~mA}
$$

(b) The diode drop is -45 V and $I=-I_{0}=-10 \mu \mathrm{~A}$. The voltage drop across the 1.5 K resistors is only 15 mV and may be neglected.
(c) In the forward direction, the answer is the same as in part (a), i.e., $I=29.8 \mathrm{~mA}$.

In the reverse direction, we draw a load line from $V=-30 \mathrm{~V}$ to $I=-30 \mathrm{~mA}$, as shown in the following figure. Then:

$$
I^{\prime}=-30 \times \frac{20}{30}=-20 \mathrm{~mA}
$$



Alternatively, there is a 10 V across the diode, leaving 20 V across the 1 K resistor.

$$
\therefore \quad \text { Current }=20 \mathrm{~mA} \text {, as there is a } 10 \mathrm{~V} \text { drop }
$$

Example 3-2 Each diode is described by a linearized volt-ampere characteristic with incremental resistance $r$ and offset voltage $V_{\gamma}$. Diode $D_{1}$ is germanium with $V_{\gamma}=0.2 \mathrm{~V}$ and $r=20 \Omega$, whereas $D_{2}$ is silicon with $V_{\gamma}=0.6 \mathrm{~V}$ and $r=15 \Omega$. Find the diode currents if: (a) $R=10 \mathrm{~K}$, (b) $R=1.5 \mathrm{~K}$.


## Solution:

(a) $R=10 \mathrm{~K}$. Assume both diodes are conducting. We have:

$$
\begin{aligned}
& 100=10.02 I_{1}+10 I_{2}+0.2 \\
& 100=10.015 I_{2}+10 I_{1}+0.6
\end{aligned}
$$



Solving for $I_{2}$ we find $I_{2}<0$. Thus our assumption that $D$ is ON is not valid. Assume $D_{1}$ is ON and $D_{2}$ is OFF. Then:

$$
I_{1}=\frac{100-0.2}{10.02}=9.97 \mathrm{~mA} \quad \text { and } \quad I_{2}=0
$$

(b) $\quad R=1 \mathrm{~K}$. Assume both $D_{1}$ and $D_{2}$ are ON . We have:

$$
\begin{aligned}
& 100=1.52 I_{1}+1.5 I_{2}+0.2 \\
& 100=1.515 I_{2}+1.5 I_{1}+0.6
\end{aligned}
$$

Solving, we find $I_{1}=39.717 \mathrm{~mA}$ and $I_{2}=26.287 \mathrm{~mA}$. Since both currents are positive, our assumption is valid.

Example 3-3 Calculate the break region over which the dynamic resistance of a diode is multiplied by a factor of 10,000 .

## Solution:

We have:

Hence,

$$
r=\eta \frac{V_{T}}{I_{0}} \varepsilon^{-V / \eta V_{T}}
$$

$$
\frac{r_{1}}{r_{2}}=\varepsilon^{V_{2}-V_{1} / \eta V_{T}}
$$

But,

$$
\frac{r_{1}}{r_{2}}=10^{4}
$$

Hence,

$$
\frac{\Delta V}{\eta V_{T}}=\frac{V_{2}-V}{\eta V_{T}}=\ln 10^{4}
$$

For silicon $\eta=2$, and at room temperature $\Delta \mathrm{V}=2 \times 26 \times 4 \times 2.3=478 \mathrm{mV}$.
For germanium, $\eta=1$ and at room temperature $\Delta V=1 \times 26 \times 4 \times 2.3=239 \mathrm{mV}$.

## 3-5 RECTIFIERS

The process of rectification involves converting the alternating waveforms to the corresponding direct waveforms. Thus, it is one type of converter in which the direct waveforms must be filtered so that the resultant output waveforms become time invariant. Rectifiers can, in general, be classified into two categories.

## 3-5-1 Half-Wave Rectifier

In a half-wave rectifier, the output waveform occurs after each alternate half-cycle of the input sinusoidal signal. Figure 3-8 shows a simple half-wave rectifier circuit.

The half-wave rectifier will generate an output waveform $v_{o}$. Between the time interval $t=0$ to $T / 2$, the polarity of the applied voltage $v_{i}$ is such that it makes the diode forward-biased. As a result the diode is turned on, i.e., the forward voltage is more than the cut-in voltage of the diode. Substituting the short-circuit equivalence of the ideal diode will result in the equivalent circuit of Figure 3-9 where it is obvious that the output signal is a replica of the applied signal.

For the period $T / 2$ to $T$, the polarity of the input voltage $\left(v_{i}\right)$ is reversed and the resulting polarity across the diode produces an OFF state with an open circuit equivalent, as shown in Figure 3-10.


Figure 3-8 Half-wave rectifier


Figure 3-9 Conduction region (0 to $T / 2$ )


Figure 3-10 Non-conducting region ( $T / 2$ to $T$ )

The result is the absence of a path for charge to flow and $v_{o}=i_{R}=0 \mathrm{~V}, R=0 \mathrm{~V}$ for the period $T / 2$ to $T$. The output signal $v_{o}$ has the average value determined by:

$$
V_{\mathrm{dc}}=0.318 V_{m}
$$

The input $v_{i}$ and the output $v_{o}$ are sketched together in Figure 3-11. It is to be noted and clearly understood that when the diode is in the forward-biased mode, it consumes 0.7 V in the case of a silicon-based diode, and 0.3 V in the case of a germanium-based diode. Thus, in such a case, there must be a drop in the voltage across the diode. Consequently, the voltage across the resistance $R$ in case of a half-wave rectifier is lowered to a value of $E-V_{d}$. If a sinusoidal source is kept in place of the battery, the sinusoidal voltage will represent the voltage across the resistance. The corresponding figure will then be as shown in Figure 3-12.

In such a case, the peak of the voltage $V_{m}$ gets lowered by an amount $V_{m}-V_{d}$. Thus, there is a finite time lag between turn-on and turn-off time of the diode in a complete time period.


Figure 3-11 Half-wave rectified signal


Figure 3-12 Output signal of the form $V_{\text {in }}-V_{\text {diode }}$


Figure 3-13 Full-wave rectifier

## 3-5-2 Full-Wave Rectifier

The circuit diagram for full-wave rectifier is shown in Figure 3-13. The full-wave rectifier can be classified into two distinct types.
(i) Centre-tapped transformer full-wave rectifier
(ii) Bridge type full-wave rectifier


Figure 3-14 Waveform for full-wave rectifier

## Centre-tapped transformer rectifier

It comprises of two half-wave circuits, connected in such a manner that conduction takes place through one diode during one half of the power cycle and through the other diode during the second half of the cycle.

When the positive half-cycle is applied to the input, i.e., transformer primary, then the top of the transformer secondary is positive with reference to the centre tap, while the bottom of the transformer secondary is negative with reference to the centre tap. As a result, diode $D_{1}$ is forward-biased and diode $D_{2}$ is reverse-biased. So the current will flow through $D_{1}$, but not through $D_{2}$ during the positive half-cycle. During the negative half-cycle, the condition is reversed. Diode $D_{2}$ is now forward-biased and diode $D_{1}$ is reverse-biased. Current will flow through diode $D_{2}$ and not through $D_{1}$ for the negative half-cycle. So the load current is shared alternatively by the two diodes and is unidirectional in each half-cycle. As a result, for the full-wave rectifier, we get the output for both the half-cycles. The waveforms for the full-wave rectifier are shown in Figure 3-14.

## Bridge rectifier

The most important disadvantage of the centre-tapped rectifier is that it brings in the use of a heavy transformer with three terminals at its output, i.e., a centre-tapped transformer. The centre tapping may not be perfect in most cases. This problem can be solved by designing another circuit with four diodes and a simple transformer. This is called a bridge rectifier. The circuit of the bridge rectifier is shown in Figure 3-15(a).

The circuit realizes a full-wave rectifier using four different diodes, connected in such a way that two of these diodes are forward-biased at a time and the other two are kept in OFF state. Consequently, the circuit is completed in both the half-cycles and a rectified output is obtained.

In the positive half-cycle of the input voltage, the current flows through the diode $D_{4}$, the resistor $R$ and diode $D_{3}$. Meanwhile the diodes $D_{1}$ and $D_{2}$ are reverse-biased. Thus, we observe that two diodes $D_{3}$ and $D_{4}$ are in the ON state and two diodes $D_{1}$ and $D_{2}$ are in the OFF state. The disadvantage of the bridge rectifier is that it uses four diodes instead of two as used in the full-wave rectifier. This does not matter much because diodes are quite cheap.

In the negative half-cycle, the other two diodes ( $D_{1}$ and $D_{2}$ ) are switched ON and the previous two ( $D_{3}$ and $D_{4}$ ) are in the OFF state. An important point to be noted is that since the current in both the half-cycle flow in the same direction, the output voltage is positive.

The biggest advantage of such a rectifier is that it does not require the use of a centre-tapped transformer. Again the PIV of the diodes has to be greater than the maximum negative voltage of the input signal.


Figure 3-15(a) Bridge rectifier

## Advantages of a bridge rectifier

(i) In the bridge circuit a transformer without a centre tap is used.
(ii) The bridge circuit requires a smaller transformer as compared to a full-wave rectifier giving the identical rectified dc output voltage.
(iii) For the same dc output voltage, the PIV rating of a diode in a bridge rectifier is half of that for a full-wave circuit.
(iv) The bridge circuit is more appropriate for high-voltage applications, thus, making the circuit compact.

## Disadvantages of a bridge rectifier

(i) Two or more diodes are required in case of a bridge rectifier, as a full-wave rectifier uses two diodes whereas a bridge rectifier uses four diodes.
(ii) The amount of power dissipated in a bridge circuit is higher as compared to a full-wave rectifier. Hence, the bridge rectifier is not efficient as far as low voltages are concerned.

## Comparison between half-wave and full-wave rectifier

(i) In a half-wave rectifier, a single diode exists and the load current flows through it for only the positive half-cycle. On the other hand, in a full-wave rectifier, the current flows throughout the cycles of the input signals.
(ii) Full-wave rectifiers require a centre-tapped transformer. For a half-wave rectifier, only a simple transformer is required.
(iii) The PIV in a half-wave rectifier is the maximum voltage across the transformer secondary. Whereas, in the case of a full-wave rectifier, the PIV for each diode is two times the maximum voltage between the centre tap and at the either end of the transformer secondary.
(iv) In a half-wave rectifier, the frequency of the load current is the same as that of the input signal and it is twice the frequency of the input supply for the full-wave rectifier.
(v) The dc load current and conversion efficiency for a full-wave rectifier is twice that of a halfwave rectifier. Also, the ripple factor of the full-wave rectifier is less than that of the half-wave circuit. This indicates that the performance of the full-wave rectifier is better than the half-wave rectifier.
(vi) In a full-wave rectifier, two diode currents flow through the two halves of the centre-tapped transformer secondary in opposite directions, so that there is no magnetization of the core. The transformer losses being smaller, a smaller transformer can be used for a full-wave rectifier.

## 3-5-3 Use of Filters in Rectification

A rectifier converts ac to dc Inadvertently, when the output voltage of the rectifier is passed through the load, fluctuating components of currents appear across the load; these are called ripples. Filters help in reducing these ripples considerably. The simplest filter in a rectifier can be understood by placing a capacitor across the load, as shown in Figure 3-15(b).

In the filtered-rectified circuit, diodes $D_{1}$ and $D_{2}$ conduct in alternate half cycles at the secondary of the transformer. So, in the absence of the filtering capacitor $C$, the output voltage consists of a series of half sinusoids. This is shown in Figure 3-16.


Figure 3-15(b) A full-wave capacitor-filtered rectifier

(b)

(c)

Figure 3-16 (a) Rectified output without filter
(b) Rectified output with filter
(c) Ideal dc filtered dc output with proper choice of capacitor in filter

During the positive half-cycle the capacitor starts charging and gets charged to the maximum amplitude of the input signal. Beyond this maximum voltage the voltage across the diode $D_{1}$ is reversed and the diode $D_{1}$ consequently stops conducting. During this period, the capacitor discharges through the load with a time constant $\tau=C R$. As the capacitor reactance at the ripple frequency is much smaller than $R$, the time constant $C R$ is much larger than the time period of the alternating voltage. The capacitor, thus, discharges very slowly and the output waveform during this interval is represented by the curve $B D$. In the following half-cycle also, the same thing is repeated with the diode $D_{2}$.Thus, due to the operation of the filter, it can be seen from Figure 3-16 that the output curve is smoothened and consequently, the ripple factor also decreases. Also, the regulation increases. The capacitor voltage at any given time is:

$$
\begin{aligned}
\frac{V_{N L}-V_{R L}}{V_{R L}} \times 100 & =\frac{V_{M}-I_{\mathrm{dc}} R_{L}}{I_{\mathrm{dc}} R_{L}} \times 100 \\
& =\frac{I_{\mathrm{dc}} R_{0}}{I_{\mathrm{dc}} R_{L}} \times 100=\frac{100}{4 f C R_{L}}
\end{aligned}
$$

$$
\begin{equation*}
\Delta V=\frac{I_{\mathrm{dc}} T}{2 C} \tag{3-21}
\end{equation*}
$$

where, $T$ is the time period of the input signal.
The average voltage across the capacitor is:

$$
\begin{equation*}
V_{\mathrm{dc}}=V_{m}-\frac{\Delta V}{2}=V_{m}-\frac{I_{\mathrm{dc}}}{4 f C} \tag{3-22}
\end{equation*}
$$

The percentage regulation (discussed in detail in the next section) is:

$$
\begin{align*}
\frac{V_{N L}-V_{R L}}{V_{R L}} \times 100 & =\frac{V_{M}-I_{\mathrm{dc}} R_{L}}{I_{\mathrm{dc}} R_{L}} \times 100 \\
& =\frac{I_{\mathrm{dc}} R_{0}}{I_{\mathrm{dc}} R_{L}} \times 100=\frac{100}{4 f C R_{L}} \text { percent } \tag{3-23}
\end{align*}
$$

The fluctuation $\Delta V$ is a measure of the ripple voltage, we have:

So that,

$$
V_{\mathrm{rms}}^{\prime 2}=\frac{2}{T} \int_{0}^{T / 2}\left(\frac{\Delta V}{2}-\frac{\Delta V}{T / 2} t\right)^{2} d t
$$

,

$$
\begin{equation*}
V_{\mathrm{rms}}^{\prime}=\Delta V / 2 \sqrt{3}=I_{\mathrm{dc}} /(4 \sqrt{3} f C) \tag{3-24}
\end{equation*}
$$

noting that $V_{\mathrm{dc}}=I_{\mathrm{dc}} R_{L}$, the ripple factor is written as:

$$
\begin{equation*}
\gamma=\frac{V_{\mathrm{rms}}^{\prime}}{V_{\mathrm{dc}}}=\frac{1}{4 \sqrt{3 f C R_{L}}} \tag{3-25}
\end{equation*}
$$

## 3-5-4 Regulation

The average load current can be written as:

$$
\begin{equation*}
I_{\mathrm{dc}}=K I_{m}=\frac{K V_{s}}{R_{f}+R_{L}} \tag{3-26}
\end{equation*}
$$

where, $R_{f}$ is the forward resistance of the diode and $R_{L}$ is the value of the load resistance.
Again, the value of $K$ is:

$$
\begin{equation*}
\frac{V_{N L}-V_{R L}}{V_{R L}} \times 100 \% \tag{3-27}
\end{equation*}
$$

The value of $K$ is $1 / \pi$ in case of a half-wave rectifier and $2 / \pi$ in case of a full-wave rectifier. The dc load voltage is given by:

$$
\begin{equation*}
V_{\mathrm{dc}}=I_{\mathrm{dc}} R_{L}=K V_{s}-I_{\mathrm{dc}} R_{L} \tag{3-28}
\end{equation*}
$$

A plot of $V_{\mathrm{dc}}$ against $I_{\mathrm{dc}}$ gives a linear variation of $V_{\mathrm{dc}}$ with $I_{\mathrm{dc}}$.
The variation of $V_{\mathrm{dc}}$ with $I_{\mathrm{dc}}$ is called regulation and the plot of $V_{\mathrm{dc}}$ vs. $I_{\mathrm{dc}}$ is referred to as the voltage regulation characteristics of the rectifier. In an ideal rectifier, $V_{\mathrm{dc}}$ is independent of $I_{\mathrm{dc}}$. In practice, the departure of the behaviour of an actual rectifier from that ideal rectifier is expressed by percentage voltage regulation. It is defined as:

Percentage voltage regulation:

$$
\begin{equation*}
\frac{V_{N L}-V_{R L}}{V_{R L}} \times 100 \% \tag{3-29}
\end{equation*}
$$

In an ideal case, $V_{N L}=V_{R L}$. So we get the percentage regulation of a rectifier as zero.

## Solved Examples

Example 3-4 Adiode, whose internal resistance is $30 \Omega$, is to supply power to a $990 \Omega$ load from a 110 V (rms) source of supply. Calculate (a) the peak load current, (b) the dc load current, (c) the ac load current, (d) the dc diode voltage, (e) the total input power to the circuit, and (f) the percentage regulation from no load to the given load.

## Solution:

(a)

$$
I_{m}=\frac{V_{m}}{R_{f}+R_{L}}=\frac{110 / 2}{1020}=152.5 \mathrm{~mA}
$$

(b)

$$
I_{\mathrm{dc}}=\frac{I_{m}}{\pi}=152.5 / \pi=48.5 \mathrm{~mA}
$$

(c)

$$
I_{\mathrm{rms}}=\frac{1}{2}(152.5)=76.2 \mathrm{~mA}
$$

(d)

$$
V_{\mathrm{dc}}=\frac{I_{m} R_{L}}{\pi}=-48.5 \times .990=-48 \mathrm{~mA}
$$

(e)

$$
\begin{gathered}
P_{i}=I_{\mathrm{rms}}^{2}\left(R_{f}+R_{L}\right)=\left(76.2 \times 10^{-3}\right)^{2}(1020) \\
=5800 \times 10^{-6} \times 1020=5.92 \mathrm{~W}
\end{gathered}
$$

(f)

$$
\begin{gathered}
\text { Percentage regulation }=\frac{V_{N L}-V_{F L}}{V_{F L}}(100 \%)=\frac{V_{m} / \pi-I_{\mathrm{dc}} R_{L}}{I_{\mathrm{dc}} R_{L}}(100 \%) \\
=\frac{49.5-48}{48}=3.125 \%
\end{gathered}
$$

## 3-5-5 Performance Analysis of Various Rectifier Circuits

## Half-wave rectifier

Peak inverse voltage (PIV). It is the voltage that the diode must withstand, and it is equal to the peak input voltage, $V_{m}$.
DC voltage. The average output voltage

$$
\begin{equation*}
V_{o(\mathrm{dc})}=0.318 V_{m} \tag{3-30}
\end{equation*}
$$

And the rms voltage:

$$
\begin{equation*}
V_{\mathrm{rms}}=1.21 V_{o(\mathrm{dc})} \tag{3-31}
\end{equation*}
$$

DC value of load current. The load current of a rectifier is unidirectional but fluctuating. The current at the output of the diode is:

$$
\begin{aligned}
& i_{L}=I_{m} \sin \omega t \text { for } 0 \leq \omega \mathrm{t} \leq \pi \\
& i_{\mathrm{L}}=0 \text { for } \pi \leq \omega \mathrm{t} \leq 2 \pi
\end{aligned}
$$

where, $I_{m}$ is the amplitude of the input signal. If $V_{S}$ is the amplitude of the transformer secondary voltage, the value of $I_{m}$ is given by:

$$
I_{m}=\frac{V_{S}}{R_{f}+R_{L}}
$$

From the definition of the average value of the load current:

$$
\begin{equation*}
I_{\mathrm{dc}}=\frac{1}{2 \pi} \int_{0}^{\pi} I_{m} \sin \omega t d(\omega t)=\frac{I_{m}}{\pi} \tag{3-32}
\end{equation*}
$$

The value of rms current can be obtained from the definition, that is:

$$
\begin{align*}
I_{\mathrm{rms}}^{2} & =\frac{1}{2 \pi} \int_{0}^{\pi} I_{m}^{2} \sin ^{2} \omega t d(\omega t)=\frac{I_{m}^{2}}{4} \\
I_{\mathrm{rms}} & =\frac{I_{m}}{2} \tag{3-33}
\end{align*}
$$

Ripple factor. Periodically, fluctuating components-the ripples-are superimposed on $I_{\mathrm{dc}}$ to give the actual load current. Due to these fluctuating components, the conversion from ac to dc by a rectifier is not perfect. The ripple factor gives a measure of this imperfection or the fluctuating components. The ripple factor, $r$, is defined by:

$$
r=\frac{\mathrm{rms} \text { value of the alternating components of the load current }}{\text { average value of the load current }}
$$

The ripple factor $r$ is given by:

$$
\begin{equation*}
r=\sqrt{\left(\frac{I_{\mathrm{rms}}}{I_{\mathrm{dc}}}\right)^{2}-1} \tag{3-34}
\end{equation*}
$$

From the expressions of dc and rms current, we can derive the ripple factor. Thus, we obtain:

$$
r=\sqrt{\left(\frac{I_{m} / 2}{I_{m} / \pi}\right)^{2}-1}
$$

which, after calculation stands at 1.21 .
Therefore, ripple factor $=1.21$ or $121 \%$.
Efficiency. The effectiveness of a rectifier in delivering the dc output power is generally measured by the rectification efficiency:

$$
\begin{equation*}
\eta_{R}=\frac{P_{o(\mathrm{dc})}}{P_{o(\mathrm{ac})}}=\frac{\left(V_{m} / \pi\right)^{2} / R}{\left(V_{m} / 2\right)^{2} / R}=\frac{4}{\pi^{2}}=40.5 \% \tag{3-35}
\end{equation*}
$$

Efficiency can also be defined as:

$$
\begin{equation*}
\left(\frac{I_{\mathrm{rms}}}{I_{\mathrm{dc}}}\right)=\frac{I_{m} / 2}{I_{m} / \pi}=\frac{\pi}{2}=1.571 \% \tag{3.36}
\end{equation*}
$$

From the above, we see that $\left(I_{\mathrm{dc}} / I_{\mathrm{rms}}\right)=2 / \pi$ and putting the value in Equation (3-35), we get

$$
\begin{equation*}
\eta_{R}=\frac{40.6}{1+R_{f} / R_{L}} \text { percent } \tag{3-37}
\end{equation*}
$$

## Full-wave rectifier

Peak inverse voltage. This is the peak voltage that the diode must be able to withstand without any breakdown. In other words, it is the largest reverse voltage that is expected to appear across the diodes.

In this case:

$$
\mathrm{PIV}=-2 \mathrm{~V}
$$

where, $V$ is the voltage peak of the input waveform.
DC voltage. The average output voltage:

The rms voltage:

$$
\begin{gather*}
V_{o(\mathrm{dc})}=0.636 V_{m}  \tag{3-38}\\
V_{\mathrm{rms}}=0.483 V_{o(\mathrm{dc})} \tag{3-39}
\end{gather*}
$$

Average load current. From the definition of the load current, we obtain:

$$
\begin{equation*}
I_{\mathrm{dc}}=\frac{2}{2 \pi} \int_{0}^{\pi} I_{m} \sin \omega t d(\omega t)=\frac{2 I_{m}}{\pi} \tag{3-40}
\end{equation*}
$$

And the rms value of the current is given by:

$$
\begin{equation*}
I_{\mathrm{rms}}=\left[\frac{2}{2 \pi} \int_{0}^{\pi} I_{m}{ }^{2} \sin ^{2} \omega t d(\omega t)\right]^{1 / 2}=\frac{I_{m}}{\sqrt{2}} \tag{3-41}
\end{equation*}
$$

Thus, we obtain:

$$
\begin{equation*}
\left(\frac{I_{\mathrm{rms}}}{I_{\mathrm{dc}}}\right)=\frac{I_{m} / \sqrt{2}}{2 I_{m} / \pi}=\frac{\pi}{2 \sqrt{2}}=1.11 \tag{3-42}
\end{equation*}
$$

Current ripple factor. Periodically, the fluctuating component-ripples-are superimposed on $I_{\mathrm{dc}}$ to give the actual load current. Due to these fluctuating components, the conversion of ac to dc by a rectifier is not perfect. The ripple factor gives a measure of this imperfection or the fluctuating components. The ripple factor is defined by:

$$
r=\frac{\text { rms value of the alternating components of the load current }}{\text { average value of the load current }}
$$

The ripple factor $r$ is given by:

$$
\begin{equation*}
r=\sqrt{\left(\frac{I_{\mathrm{rms}}}{I_{\mathrm{dc}}}\right)^{2}-1} \tag{3-43}
\end{equation*}
$$

From Equations (3-40) and (3-41) we get:

$$
\begin{align*}
I_{\mathrm{rms}} & =I_{m} / \sqrt{2} \\
r & =\sqrt{\left(\frac{\left(\frac{I_{m}}{2}\right)^{2}}{\left(\frac{2 I_{m}}{\pi}\right)^{2}}-1\right.}  \tag{3-44}\\
r & =\sqrt{\left(\frac{\pi}{2 \sqrt{2}}\right)^{2}-1} \\
& =0.482
\end{align*}
$$

Efficiency. The rectification efficiency is given by:

$$
\begin{equation*}
\eta=\frac{P_{\mathrm{dc}}}{P_{\mathrm{ac}}} \times 100 \% \tag{3-45}
\end{equation*}
$$

For a full-wave rectifier circuit:

$$
\begin{gather*}
P_{\mathrm{dc}}=\left(I_{\mathrm{dc}}\right)^{2} R_{L}=\left(\frac{2 I_{m}}{\pi}\right)^{2} \frac{1}{\left(R_{f}+R_{L}\right)^{2}}=\frac{4 V_{m}^{2} R_{L}}{\pi^{2}\left(R_{f}+R_{L}\right)^{2}}  \tag{3-46}\\
P_{\mathrm{ac}}=\left(I_{\mathrm{rms}}\right)^{2}\left(R_{f}+R_{L}\right)=\frac{V_{m}^{2}}{2\left(R_{f}+R_{L}\right)}  \tag{3-47}\\
\eta=\frac{P_{\mathrm{dc}}}{P_{\mathrm{ac}}} \times 100 \%=\frac{0.812}{\left(1+\frac{R_{f}}{R_{L}}\right)} \times 100 \% \tag{3-48}
\end{gather*}
$$

## Solved Examples

Example 3-5 Show that the maximum dc output power $P_{\mathrm{dc}}=V_{\mathrm{dc}} I_{\mathrm{dc}}$ in a half-wave single-phase circuit occurs when the load resistance equals the diode resistance $R_{f}$.

## Solution:

We have:

$$
P_{\mathrm{dc}}=I_{\mathrm{dc}}^{2} R_{L}=\frac{V_{m}^{2} R_{L}}{\pi^{2}\left(R_{f}+R_{L}\right)^{2}}
$$

For max,

$$
P_{\mathrm{dc}} \text { set } \frac{d P_{\mathrm{dc}}}{d R_{L}}=0
$$

or,

$$
\frac{V_{m}^{2}}{\pi}\left[\frac{\left(R_{f}+R_{L}\right)^{2}-2\left(R_{f}+R_{L}\right) R_{L}}{\left(R_{f}+R_{L}\right)^{4}}\right]=0
$$

Then, $R_{f}+R_{L}=2 R_{L}$

$$
\therefore R_{L}=R_{f}
$$

Example 3-6 The efficiency of the rectification $\eta_{T}$ is defined as the ratio of the dc output power $P_{\mathrm{dc}}=V_{\mathrm{dc}} I_{\mathrm{dc}}$ to the input power $P_{i}=(1 / 2 \pi) \int_{0}^{2 \pi} v_{i} i d \alpha$.
(a) Show that, for the half-wave rectifier circuit:

$$
\eta_{r}=\frac{40.6}{1+R_{f} / R_{L}} \%
$$

(b) Show that, for the full-wave rectifier, $\eta_{r}$ has twice the value of the value given in Part (a).

## Solution:

(a)
(b)

$$
\begin{aligned}
& \eta_{r}=\frac{P_{\mathrm{dc}}}{P_{i}} \times 100 \%=\frac{I_{\mathrm{dc}}^{2} R_{L} \times 100 \%}{I_{\mathrm{rms}}^{2}\left(R_{f}+R_{L}\right)}=\left(\frac{I_{\mathrm{dc}}}{I_{\mathrm{rms}}}\right)^{2} \frac{100 \%}{1+\frac{R_{f}}{R_{L}}} \\
& =\left(\frac{I_{m}}{\pi / I_{m} / 2}\right)^{2} \frac{100 \%}{1+\frac{R_{f}}{R_{R}}}=\frac{40.6}{1+\frac{R_{f}}{R_{R}}} \%
\end{aligned}
$$

Example 3-7 Prove that the regulation of both the half-wave and the full-wave rectifier is given by: Percentage regulation $=R_{f} / R_{L} \times 100 \%$.
Solution:
Consider a half-wave rectifier: $V_{N L}=\frac{V_{m}}{\pi} \quad$ and $\quad V_{F L}=\frac{V_{m}}{\pi} \frac{R_{L}}{R_{L}+R_{f}}$
$\therefore$ Percentage regulation $=\frac{V_{N L}-V_{F L}}{V_{F L}} \times 100 \%=\frac{\frac{V_{m}}{\pi}\left(1-\frac{R_{L}}{R_{L}+R_{f}}\right)}{\frac{V_{m}}{\pi} \frac{R_{L}}{R_{L}+R_{f}}}=\frac{R_{f}}{R_{L}} \times 100 \%$
For a full-wave rectifier, $V_{N L}$ and $V_{F L}$ are doubled, and hence, the regulation remains the same as above.

Example 3-8 A full-wave single phase rectifier consists of a double diode, the internal resistance of each element of which may be considered to be constant and equal to $500 \Omega$. These feed into a pure resistance load of $2,000 \Omega$. The secondary transformer voltage to centre tap is 280 V . Calculate (a) the dc load current, (b) the direct current in each tube, (c) the ac voltage across each diode, (d) the dc output power, and (e) the percentage regulation.

## Solution:

(a) $I_{\mathrm{dc}}=\frac{2 I_{m}}{\pi}=\frac{2 V_{m}}{\pi\left(R_{L}+R_{f}\right)}=\frac{2 \times 280}{\mathrm{R} 2 / \pi(2500)}=101 \mathrm{~mA}$.
(b) $\left(I_{\mathrm{dc}}\right)_{\mathrm{tube}}=\frac{1}{2} I_{\mathrm{dc}}=50.5 \mathrm{~mA}$.
(c) The voltage to centre tap is impressed across $R_{f}$ in series with the $R_{L}$.

Hence, the voltage across the conducting is sinusoidal with a peak value:

$$
V_{m} \frac{500}{2500}=0.2 V_{m}
$$

During non-conduction of $V_{1}$, we see by transversing the outside path of the circuit sketched that $v_{1}=-2 v-v_{2}$.

Since, $V_{2}$ is now conducting, its peak value is $0.2 V_{m}$ and that of $v_{1}$ is $-2 V_{m}+0.2 V_{m}=-1.8 V_{m}$. Thus, the voltage $v_{1}$ across $V_{1}$ is as shown, and its ac value is:


$$
V_{\mathrm{rms}}^{2}=\frac{1}{2 \pi}=\int_{0}^{\pi}\left(0.2 V_{m}\right)^{2} \sin ^{2} \alpha d \alpha+\frac{1}{2 \pi} \int_{\pi}^{2 \pi}\left(-1.8 V_{m}\right)^{2} \sin ^{2} \alpha d \alpha=\frac{V_{m}^{2}}{4}\left[(0.2)^{2}+(1.8)^{2}\right]
$$

Hence, $V_{\text {rms }}=0.905 V_{m}=0.905 \times 280 \sqrt{2}=358 \mathrm{~V}$.
(d)

$$
P_{\mathrm{dc}}=I_{\mathrm{dc}}^{2} R_{\mathrm{L}}=(0.101)^{2}(2000)=20.4 \mathrm{~W}
$$

(e)

$$
\text { Percentage regulation }=\frac{R_{f}}{R_{L}} \times 100 \%=\frac{500}{2000} \times 100 \%=25 \%
$$

Example 3-9 In the full-wave single phase bridge, can the transformer and the load be interchanged? Explain carefully.

## Solution:

The load and the transformer cannot be interchanged. If they were, the circuit shown would be the result. Note that if $A$ is positive with respect to $B$, all diodes will be reverse-biased. If $B$ is positive with respect to $A$, then all four diodes conduct, thus, short circuiting the transformer.


Example 3-10 A 1 mA dc metre whose resistance is $20 \Omega$ is calibrated to read rms volts when used in a bridge circuit with semiconductor diodes. The effective resistance of each element may be considered to be zero in the forward direction and infinite in the reverse direction. The sinusoidal input voltage is applied in series with a 5 K resistance. What is the full-scale reading of this metre?

## Solution:

Hence,

$$
\begin{aligned}
& I_{\mathrm{dc}}=\frac{2 I_{m}}{\pi}=\frac{2 V_{m}}{\pi R_{L}}=\frac{2 \mathrm{R} 2 V_{\mathrm{rms}}}{\pi(5020)}=1 \times 10^{-3} \\
& v_{0(\max )}=14 \mathrm{~V}
\end{aligned}
$$

Example 3-11 An ac supply of 220 V is applied to a half-wave rectifier circuit through transformer with a turns ratio 10:1. Find (a) dc output voltage and (b) PIV. Assume the diode to be an ideal one.

## Solution:

Given $V_{i}=220 \mathrm{~V}, N_{2} / N_{1}=10$.
(a) The secondary voltage:

$$
\begin{aligned}
& V_{2}=V_{1} \times \frac{N_{2}}{N_{1}}=220 \times \frac{1}{10}=22 \mathrm{~V} \\
& \quad V_{m}=\sqrt{2} V_{2}=\sqrt{2} \times 22=31.11 \mathrm{~V} \\
& \quad V_{\mathrm{dc}}=0.318 V_{m}=0.318 \times 31.11=9.89 \mathrm{~V}
\end{aligned}
$$

(b) PIV of a diode is given by PIV $=V_{m}=31.11 \mathrm{~V}$

Example 3-12 In a half-wave rectifier circuit the input voltage is 230 V and transformer ratio is 3:1. Determine the maximum and the average values of power delivered to the load. Take $R_{L}$ equal to $200 \Omega$.

## Solution:

Given, $V_{1}=230 \mathrm{~V}, \quad \frac{N_{2}}{N_{1}}=\frac{1}{3}, \quad R_{L}=200 \Omega$.
The rms value of secondary voltage is given by:

$$
V_{2}=V_{1} \times \frac{N_{2}}{N_{1}}=230 \times \frac{1}{3}=76.67 \mathrm{~V}
$$

Maximum value of the secondary voltage is:

$$
V_{m}=\sqrt{2} V_{2}=1.414 \times 76.67=108.41 \mathrm{~V}
$$

Maximum value of the load current is then given by:

$$
I_{m}=\frac{V_{m}}{R_{L}}=\frac{108.41}{200}=0.542 \mathrm{~A}
$$

Maximum load power:

$$
\begin{aligned}
P_{\max } & =I_{m}^{2} \times R_{L} \\
& =(0.542)^{2} \times 200=58.75 \mathrm{~W}
\end{aligned}
$$

Average value of output voltage, $V_{d c}=0.318 V_{m}=0.318 \times 108.41=34.47 \mathrm{~V}$
Average value of load current:

$$
I_{d c}=\frac{V_{d c}}{R_{L}}=\frac{34.47}{200}=0.172 \mathrm{~A}
$$

Average value of load power, $P_{d c}=I_{d c}^{2} \times R_{L}=(0.172)^{2} \times 200=5.92 \mathrm{~W}$
Example 3-13 A half-wave rectifier is used to supply 30 V dc to a resistive load of 500 ohms. The diode has a forward resistance of $25 \Omega$. Find the maximum value of the ac voltage required at the input.

## Solution:

Given, $V_{\mathrm{dc}}=30 \mathrm{~V}, r_{f}=25 \Omega, R_{L}=500 \Omega$.
Average value of the load current:

$$
I_{d c}=\frac{V_{d c}}{R_{L}}=\frac{30}{500}=0.06 \mathrm{~A}
$$

Maximum value of the load current, $I_{m}=\pi \times I_{d c}=3.142 \times 0.06=0.188 \mathrm{~A}$
Voltage required at the input is given by:

$$
\begin{aligned}
V_{i(\max )} & =I_{m}^{2}\left(r_{f}+R_{L}\right) \\
& =(0.188)^{2}(25+500)=18.55 \mathrm{~V}
\end{aligned}
$$

Example 3-14 A half-wave rectifier is used to supply $100 V_{\text {dc }}$ to a load of $500 \Omega$. The diode has a resistance of $20 \Omega$. Calculate (a) the ac voltage required and (b) the efficiency of rectification.
Solution:
Given, $V_{d c}=100 \mathrm{~V}, R_{L}=500 \Omega, r_{f}=20 \Omega$.
(a) DC voltage:

$$
\begin{aligned}
& V_{\mathrm{dc}}=\frac{V_{m}}{\pi}=\frac{I_{m}\left(R_{L}+r_{f}\right)}{\pi} \\
& I_{\mathrm{dc}}=\frac{V_{\mathrm{dc}}}{R_{L}}=\frac{100}{500}=0.2 \mathrm{~A} \\
& I_{m}=I_{\mathrm{dc}} \times \pi=3.142 \times 0.2 \mathrm{~A}=0.6284 \mathrm{~A} \\
& V_{m}=I_{m}\left(R_{L}+r_{f}\right)=0.6284(500+20)=326.77 \mathrm{~V}
\end{aligned}
$$

(b) Rectification efficiency is given by:

$$
\eta=\frac{0.406}{1+\frac{r_{f}}{R_{L}}}=\frac{0.406}{1+20 / 500}=0.39=39 \%
$$

Example 3-15 A half-wave rectifier circuit has a load of $5000 \Omega$. Find the values of (a) current in the circuit, (b) dc output voltage across $R_{L}$ and (c) voltage across the load. Given $v=50 \sin 100 \pi t$, $r_{f}=20 \Omega$.

## Solution:

Given, $v=50 \sin 100 \pi t$.
Comparing the given equation with the standard equation $v=V_{m} \sin 2 \pi f t$, we have:

$$
V_{m}=50 \mathrm{~V}, f=50 \mathrm{~Hz}
$$

Since the diode conducts only during the positive half of the input voltage, we have:

$$
I_{m}=\frac{V_{m}}{R_{L}+r_{f}}=\frac{50}{5000+20} \approx 10 \mathrm{~mA}
$$

(a) Hence current $i=10 \sin 100 \pi t$ for $\pi<100 \pi t<2 \pi$

$$
=0 \text { for } 0<100 \pi t<\pi
$$

(b) DC output voltage, $V_{\mathrm{dc}}=I_{\mathrm{dc}} \times R_{L}$

$$
=\frac{I_{m}}{\pi} \times R_{L}=\frac{10 \times 10^{-3}}{3.142} \times 5000=15.9 \mathrm{~V}
$$

Output voltage, $V_{o}=15.9 \sin 100 \pi t$ for $\pi<100 \pi t<2 \pi=0$
(c) Assuming the diode is an ideal diode, the voltage across it is zero during the forward-biased. When the diode is reverse-biased, the voltage across diode is:

$$
v=15.9 \sin 100 \pi t \text { for } 0<100 \pi t<\pi=0 \text { for } \pi<100 \pi t<2 \pi
$$

Example 3-16 In a half-wave rectifier circuit fed from $230 \mathrm{~V}, 50 \mathrm{~Hz}$ mains, it is desired to have a ripple factor $\gamma \ll 0.004$. Estimate the value of the capacitance needed. Given, $I_{L}=0.5 \mathrm{~A}$.

## Solution:

Given $V_{\mathrm{rms}}=230 \mathrm{~V}, f=50 \mathrm{~Hz}, \gamma \leq 0.005, I_{L}=0.5 \mathrm{~A}$. Take $\gamma=0.003$.
Load current is given by:

$$
\begin{gathered}
I_{L}=\frac{I_{m}}{\pi}=I_{\mathrm{dc}} \\
V_{m}=\sqrt{2} \times V_{\mathrm{rms}}=1.4 \times 230=322 \mathrm{~V} \\
V_{\mathrm{dc}}=\frac{V_{m}}{\pi} \frac{322}{3.14}=102.5 \mathrm{~V}
\end{gathered}
$$

Load resistance:

$$
\begin{aligned}
R_{L} & =\frac{V_{\mathrm{dc}}}{I_{\mathrm{dc}}}=\frac{102.5}{0.5}=205 \Omega=200 \Omega \\
\gamma & =\frac{1}{2 \sqrt{3} f C R_{L}} \\
& =\frac{1}{2 \sqrt{3} f \gamma R_{L}}=\frac{1}{2 \sqrt{3} \times 50 \times 200 \times 0.003}=9.62 \mathrm{mF}
\end{aligned}
$$

Ripple factor:

Example 3-17 The voltage across half the secondary winding in a centre-tapped transformer used in a full-wave rectifier is $230 \sin 314 t$. The forward-bias resistance of each diode is $20 \Omega$ and the load resistance is $3.15 \mathrm{k} \Omega$. Calculate the ripple factor.

## Solution:

Given, $R_{L}=3.15 \mathrm{k} \Omega, r_{f}=20 \Omega$.
Instantaneous voltage, $v=V_{m} \sin 2 \pi f t$

$$
=230 \sin 314 t
$$

Comparing, we have, $V_{m}=230 \mathrm{~V}, f=50 \mathrm{~Hz}$

The rms value of current:

$$
\begin{aligned}
I_{\mathrm{rms}} & =0.707\left(\frac{V_{m}}{R_{L}+r_{f}}\right)=0.707\left(\frac{230}{3150+20}\right) \\
& =0.707 \times 0.0726=0.0513 \mathrm{~A}
\end{aligned}
$$

DC value of current, $I_{\mathrm{dc}}=0.637 I_{m}=0.637 \times 0.0726=0.0331 \mathrm{~A}$
Therefore, ripple factor:

$$
\gamma=\sqrt{\left(\frac{I_{\mathrm{rms}}}{I_{\mathrm{dc}}}\right)^{2}-1}=\sqrt{\left(\frac{0.0513}{0.0331}\right)^{2}-1}=0.48
$$

Example 3-18 Ideal diodes are used in a bridge rectifier with a source of $230 \mathrm{~V}, 50 \mathrm{~Hz}$. If the load resistance is $150 \Omega$ and turns ratio of transformer is $1: 4$, find the dc output voltage and pulse frequency of the output.

## Solution:

Given, $V_{p}=230 \mathrm{~V}, f=50 \mathrm{~Hz}, R_{L}=200 \Omega, N_{S}: N_{P}=1: 4$.
We know that:

$$
\frac{V_{S}}{V_{P}}=\frac{N_{S}}{N_{P}}
$$

The rms secondary voltage:

$$
\begin{gathered}
V_{S}=V_{P} \times \frac{N_{S}}{N_{P}}=230 \times \frac{1}{4}=57.5 \mathrm{~V} \\
V_{S}=V_{\mathrm{rms}}=57.5 \mathrm{~V}
\end{gathered}
$$

Maximum voltage across secondary, $V_{m}=V_{\text {rms }} \times \sqrt{2}=57.5 \times \sqrt{2}=81.3 \mathrm{~V}$

Average current:

$$
I_{\mathrm{dc}}=\frac{2 V_{m}}{\pi R_{L}}=\frac{2 \times 81.3}{3.14 \times 200}=0.26 \mathrm{~A}
$$

DC output voltage, $V_{\mathrm{dc}}=I_{\mathrm{dc}} \times R_{L}=0.26 \times 150=39 \mathrm{~V}$
As there are two output pulses for each complete cycle of the input ac voltage in full-wave rectification, the output frequency is twice that of the ac supply frequency.

$$
\therefore \quad f_{\text {out }}=2 f_{\text {in }}=2 \times 50=100 \mathrm{~Hz}
$$

Example 3-19 Find the maximum dc voltage that can be obtained from the full-wave rectifier circuit.

## Solution:

Given, $V_{p}=220 \mathrm{~V}, f_{i}=50 \mathrm{~Hz}, R_{L}=1.5 \mathrm{k} \Omega, N_{p}=1000, N_{S}=100$.
We know that:

$$
\frac{V_{S}}{V_{P}}=\frac{N_{S}}{N_{P}}
$$

The rms secondry voltage:

$$
V_{S}=V_{p} \times \frac{N_{S}}{N_{P}}=220 \times \frac{100}{1000}=22 \mathrm{~V}
$$

Maximum secondary voltage, $V_{\text {rms }}=22 \times \sqrt{2}=30.8 \mathrm{~V}$
Maximum voltage across half-secondary winding, $V_{m}=\frac{30.8}{2}=15.4 \mathrm{~V}$
Average current: $\quad I_{\mathrm{dc}}=\frac{2 V_{m}}{\pi R_{L}}=\frac{2 \times 15.4}{3.14 \times 1500}=6.53 \times 10^{-3} \mathrm{~A}$
Dc output voltage, $V_{\mathrm{dc}}=I_{\mathrm{dc}} \times R_{L}=6.53 \times 10^{-3} \times 1500=9.79 \mathrm{~V}$

Example 3-20 A full-wave rectifier using a capacitor filter is to supply 30 V de to a $1 \mathrm{k} \Omega$ load. Assuming the diode and transformer winding resistance to be negligible, calculate the input voltage required and the value of the filter capacitor for a ripple of 0.015 .

## Solution:

Given, $V_{\mathrm{dc}}=30 \mathrm{~V}, R_{L}=1 \mathrm{k} \Omega$ and $\gamma=0.015$.
DC output current:

$$
I_{\mathrm{dc}}=\frac{V_{\mathrm{dc}}}{R_{L}}=\frac{30 \mathrm{~V}}{1 \mathrm{k} \boldsymbol{\Omega}}=30 \mathrm{~mA}
$$

DC output voltage:

$$
V_{\mathrm{dc}}=V_{m}-\frac{5000 I_{\mathrm{dc}}}{C}
$$

In order to determine $V_{m}$, we must calculate the value of $C$.
We know that ripple factor:

$$
\gamma=\frac{2900}{C R_{L}}=0.01
$$

Hence:

$$
C=\frac{2900}{0.015 \times 1000} \mu \mathrm{~F}=193 \mu \mathrm{~F}
$$

$$
V_{m}=V_{\mathrm{dc}}+\frac{5000 I_{\mathrm{dc}}}{C}=30+\frac{5000 \times 0.03}{193}=30.78 \mathrm{~V}
$$

Line-to-line secondary voltage: $\quad \frac{2 V_{m}}{\sqrt{2}}=\frac{2 \times 30.78}{\sqrt{2}}=43.52 \mathrm{~V}$
Example 3-21 The output of a full-wave rectifier is fed from a $40-0-40 \mathrm{~V}$ transformer. The load current is 0.1 A . The two $40 \mu \mathrm{~F}$ capacitors are available. The circuit resistance exclusive of the load is $40 \Omega$. (a) Calculate the value of inductance for a two-stage L -section filter. The inductances are to be equal. The ripple factor is to be 0.0001 . (b) Calculate the output voltage.

## Solution:

(a)

$$
\begin{aligned}
L C & =1.76\left(\frac{0.472}{r}\right)^{\frac{1}{n}} \\
L & =\frac{1.76}{40 \times 10^{-6}}\left(\frac{0.472}{0.0001}\right)^{\frac{1}{2}} \\
& =3.02 \mathrm{H} \\
V_{d c} & =\frac{2 V_{m}}{\pi}-I_{d c} R \\
& =\frac{(2 \sqrt{2}) 40}{\pi}-0.1 \times 40 \\
& =36-4=32 \mathrm{~V}
\end{aligned}
$$

Example 3-22 A full-wave single-phase rectifier employs a $\pi$-section filter consisting of two $4 \mu \mathrm{~F}$ capacitances and a 20 H choke. The load current is $50 \mu \mathrm{~A}$. Calculate the dc output voltage and ripple voltage. The resistance of the choke is $200 \Omega$.

## Solution:

$$
\begin{aligned}
V_{\mathrm{dc}} & =V_{m}-\frac{4170}{C} I_{\mathrm{dc}}-I_{\mathrm{dc}} R \\
& =300 \sqrt{2}-\frac{4170}{C}(0.05) 0-(0.05) \times 200 \\
& =362.13 \mathrm{~V} \\
r & =\frac{3300}{C C_{1} L R_{L}} \\
& =\frac{3300 \times 0.05}{4 \times 4 \times 20 \times 353} \\
& =1.46 \times 10^{-3} \\
V_{\mathrm{rms}} & =r V_{\mathrm{dc}}=0.015 \mathrm{~V}
\end{aligned}
$$

## 3-6 CLIPPER AND CLAMPER CIRCUITS

## 3-6-1 Clipper

A clipper is a type of diode network that has the ability to "clip off" a portion of the input signal without distorting the remaining part of the alternating waveform. The half-wave rectifier is an example of the simplest form of diode clipper-one resistor and a diode. Depending on the orientation of the diode, the positive or negative region of the input signal is "clipped" off.

There are two general categories of clippers: series and parallel. The series configuration is defined as one where the diode is in series with the load, while the parallel clipper has the diode in a branch parallel to the load.

## Series clipper

A series clipper and its response for two types of alternating waveforms are provided in Figures 3-17(a) and 3-17(b).

From the Figure 3-17(b) of the half-wave rectifier, we see that there are no clear cut restrictions on the type of signals that can be applied at the input. The addition of a dc supply, as shown in Figure 3-18, can have a pronounced effect on the output of a clipper.


Figure 3-17(a) Series clipper circuit

## Key points

(i) The first step is to find out in which interval of the input signal the diode is in forward-bias.
(ii) For Figure 3-18, the direction of the diode suggests that the signal $v_{i}$ must be positive to turn it on. The dc supply further requires the voltage $v_{i}$ to be greater than $v$ volts to turn the diode on. The negative region of the input signal turns the diode into the OFF state. Therefore, in the negative region the diode is an open circuit.


Figure 3-17(b) Response of clipper circuit



Figure 3-18 Series clipper with a dc supply
(iii) Determine the applied voltage (transition voltage) that will cause a change in state for the diode. For the ideal diode the transition between states will occur at that point on the characteristics where $v_{d}=0 \mathrm{~V}$ and $i_{d}=0 \mathrm{~A}$. Applying this condition to Figure 3-18 will result in the configuration of Figure 3-19 and it is recognized that the level of $v_{i}$ that will cause a transition in state is:

$$
v_{i}=\mathrm{V}
$$



Figure 3-19 Determining the transition level of the input signal

Figure 3-20 Determining $v_{o}$ in the clipper circuit



Figure 3-22 Determining $v_{o}$ when $v_{i}=V_{m}$

Figure 3-21 Determining levels of $v_{0}$

For an input voltage greater than $V$ volts, the diode is in the short-circuit state, while for input voltage less than $V$ volts it is in the open-circuit or OFF state (as it is reverse-biased).
(iv) Be continually aware of the defined terminals and polarity of $v_{o}$. When the diode is in the shortcircuit state, as shown in Figure 3-20, the output voltage $v_{o}$ can be determined by applying KVL in the clock-wise direction:
or,

$$
\begin{aligned}
& v_{i}-V-v_{o}=0 \\
& v_{o}=v_{i}-V
\end{aligned}
$$

(v) It can be helpful to sketch the input signal above the output and determine the output at instantaneous values of the input. It is then possible to sketch the output voltage from the resulting data points of $v_{o}$, as shown in Figure 3-21.

At $v_{i}=V_{m}$, the network to be analysed is shown in Figure 3-22.
For $V_{m}>V$, the diode is in the short-circuitstate and $v_{o}=V_{m}-V$. At $v_{i}=V$, the diodechanges state and $v_{i}=-V_{m}, v_{o}=0 \mathrm{~V}$. The complete curve for $v_{o}$ can be sketched, as shown in Figure 3-23.

## Parallel clipper

A simple parallel clipper and its response are shown in Figure 3-24 and Figure 3-25 respectively. Input $v_{i}$ is applied for the output $v_{o}$. The analysis of parallel configuration is very similar to the series configuration.


Figure 3-23 Sketch for $v_{\text {o }}$


## Break region

There is a discontinuity at the voltage $V_{\gamma^{\prime}}$. Actually the transition of a diode state is not exactly abrupt but gradual. Thus, a waveform, which is transmitted through the clipper circuit, will not show an abrupt clipping. Instead, it will show a gradual broken region, exhibiting the regions of un-attenuated and attenuated transmission. Now, we will estimate the range of this break region. The output current of a diode is given by:

$$
\begin{equation*}
I=I_{o}\left(e^{V / \eta V_{T}}-1\right) \tag{3-49}
\end{equation*}
$$

Beyond the diode break point, the expression of the current that is large, compared to $I_{o}$, may be given by:

$$
I=I_{o} e^{V / \eta V_{T}}
$$

The incremental diode resistance $r=d v / d I$ and as obtained from the Equation (3-49) is given by:

$$
\begin{equation*}
r=\frac{\eta V_{T}}{I_{o}} e^{-V / \eta V_{T}}=\frac{\eta V_{T}}{I} \tag{3-50}
\end{equation*}
$$



Figure 3-25 Response of parallel clipper

From Equation (3-50), we note that $r$ varies inversely with the quiescent current, and directly with the absolute temperature. We also note that the break region is independent of the quiescent current.

Again for meaningful clipping to be done, the applied signal must vary from one side of the break point to a point well on the other side. If the signal is only of the order of magnitude of the extent of the break region, the output will not display sharp limiting.

## Solved Examples

Example 3-23 A symmetrical 5 kHz square wave whose output varies between +10 V and -10 V is impressed upon the clipping circuit shown. Assume, $R_{f}=0, R_{r}=2 \mathrm{M}$, and $V_{\gamma}=0$. Sketch the steady-state output waveform, indicating numerical values of the maximum, minimum, and constant portions.


## Solution:

The diode conducts when, $v_{i}<2.5 \mathrm{~V}$. The diode is open when:

$$
v_{i}>2.5 \mathrm{~V} \text { and } v_{o}=2.5 \mathrm{~V}+\frac{v_{i}-2.5 \mathrm{~V}}{3}
$$

When diode conducts, $v_{\mathrm{i}}=v_{0}<2.5 \mathrm{~V}$.
Example 3-24 (a) The input voltage $v_{i}$ to the two level clippers shown in Figure (a) of the figure varies linearly from 0 to 150 V . Sketch the output voltage $v_{o}$ to the same time scale as the input voltage. Assume ideal diodes.

(b) Repeat Part (a) for the circuit shown in Figure (b).

## Solution:

(a) When $v_{i}<50 \mathrm{~V}$, the first diode is open and second diode conducts, and:

$$
v_{o}=100-\frac{2}{3} \times 27=50 \mathrm{~V}
$$

When $50<v_{i}<100$, both diodes conduct, and $v_{o}=v_{i}$. When $v_{i}>100$, the first diode is conducting but the second diode is open, so $v_{o}=100 \mathrm{~V}$.

(b) When $v_{i}<25 \mathrm{~V}$, neither diode conducts and $v_{o}=25 \mathrm{~V}$. When $v_{\mathrm{i}}>25 \mathrm{~V}$, the upper diode conducts and:

$$
v_{o}=\left(v_{i}-25\right) \frac{2}{3}+25
$$

When $v_{0}$ reaches $100 \mathrm{~V}, v_{i}$ rises to 137.5 V . For larger $v_{i}$, both diodes conduct and $v_{o}=100 \mathrm{~V}$ (if $v_{i}=40 \sin \omega t$, then $v_{0}=20 \sin \omega t$ ).


Example 3-25 The triangular waveform shown is to be converted into a sine wave by using clipping diodes. Consider the dashed waveform sketched as a first approximation to the sinusoid. The dashed waveform is coincident with the sinusoid at $0^{\circ}, 30^{\circ}, 60^{\circ}$, etc. Devise a circuit whose output is this broken-line waveform when the input is the triangular waveform. Assume ideal diodes and calculate the values of all supply voltages and resistances used. The peak value of the sinusoid is 50 V .

## Solution:

Desired output:




## 3-6-2 Clamper

A clamping network is one that will "clamp" a signal to a different dc level. The network must have a capacitor, a diode, and a resistive element, but it can also employ an independent dc supply to introduce an additional shift. Before further probing into the clamper circuit one must have a basic understanding of a transient $R C$ circuit.

From the basic understanding of a series $R C$ transient circuit applied across a dc voltage $E_{O}$, the instantaneous charge across the capacitor at any time is given by

$$
Q(t)=Q_{o}\left(1-e^{-t / R C}\right)
$$

$Q_{o}=E_{o} C$ where, $C$ is the capacitance of the capacitor.
We know that the time constant of the $R C$ circuit is given by $\tau=R C$. This was the case when the capacitor was being charged from zero voltage level. From Figure 3-26 it is at once interpreted that the rise time becomes smaller if we decrease the time constant.

Hence, to reach the maximum charging level quickly, we need to reduce the time constant. In case of discharge through a $R C$ circuit, it can again be shown that, $Q(t)=Q_{o} e^{-t / R C}$ where, $Q_{o}$ is the initial charge on the capacitor.


Figure 3-26 Charging of a $R C$ circuit


Figure 3-27 Discharging of an $R C$ circuit

Here also the time constant has the same value, and from Figure 3-27 we can instantly say that the discharge will occur quickly if the time constant of the circuit is decreased. In other words, we can state, that to hold the charge in a capacitor for a sufficiently longer time, we need to increase the time constant of the circuit.

In electronic circuits, clamping usually refers to holding voltage at its maximum value for a desired period of time. In order to do that, the magnitude of $R$ and $C$ must be so chosen that the time constant, $\tau=R C$, is large enough to ensure that the voltage across the capacitor does not discharge significantly during the interval the diode is non-conducting. Figure 3-28 shows the clamping circuit that will clamp the input signal to the zero level.

During the interval $0-T / 2$ the network will appear, as shown in Figure 3-29, with the diode in the ON state effectively "shorting out" the effect of the resistor $R$.

The resulting $R C$ time constant is so small that the capacitor will charge to $V$ volts very quickly. During this interval the output voltage is directly across the short circuit and $v_{o}=0 \mathrm{~V}$.

When the input switches to $-V$ state, the network will appear as shown in Figure 3-30.
The diode will now be in the open-state condition. Applying KVL around the input loop of Figure 3-30 will result in:

$$
-V-V-v_{o}=0
$$




Figure 3-28 Simple clamper circuit
or,

$$
v_{o}=-2 \mathrm{~V}
$$

The negative sign results from the fact that the polarity of 2 V is opposite to the polarity defined for $v_{o}$. The resulting output waveform appears with the input signal. The output signal is clamped to 0 V for the interval $0-T / 2$ but maintains the same total swing $(2 \mathrm{~V})$ as the input. For a clamping network the total swing of the output is equal to the total swing of the input.

## Analysis of clamping networks

In general, the following steps must be kept in mind when analysing the clamping networks.


Figure 3-29 State of the circuit when $v_{i}$ is more than $v_{\text {diode }}$
(i) The first step is to calculate the interval of the input signal in which the diode is in forward bias.


Figure 3-30 State of the circuit in the negative half-cycle
(ii) The second step is to determine the voltage across the capacitor. This is assumed to rise instantaneously.
(iii) Due to the longer time constant of the circuit, the capacitor will hold on to its established voltage level.
(iv) During the whole process, the analysis maintains a continual awareness of the location and reference polarity for $v_{o}$ to ensure that the proper levels for $v_{o}$ are obtained.
(v) The general rule that the total swing of the output must match the swing of the input signal, should be kept in mind.

## 3-7 COMPARATORS

The diode circuit which has been used in the design of the clipping circuit can also be used for the purpose of comparison, hence the name comparator. The basic principle on which the comparator works is the switching of the diodes. This action corresponds to the phase when the diode conducts; and when it does, the comparator circuit is used to compare the input arbitrary voltage with the reference voltage. This reference voltage is predefined, and


Figure 3-31 A diode comparator the output attains a sharp slope when the input waveform crosses the predefined level. The basic and foremost difference between a clipper and a comparator is that, in case of a comparator, we are not interested in reproducing the input waveform or any of its parts. In general the comparator output consists of a sharp departure from its quiescent point as the input signal attains the reference level, but otherwise the circuit remains unaffected by the input signal. The basic operation is given in Figure 3-31. It also gives a comparative study of the input and the output, as can be understood from Figure 3-32.
Figure 3-31 shows that as long as the input signal is below the total threshold voltage, i.e., cutin voltage of the diode and that of the voltage source, the output is not affected at all. The output


Figure 3-32 Input signal with the threshold voltage


Figure 3-33 Corresponding output waveform
is just the reference voltage of the voltage source. But, as soon as the input voltage exceeds the predefined threshold voltage, the output gives a sharp response and executes the ultimate purpose of the comparator. Thus, the output of the circuit in Figure 3-33 shows that the output is very different when the input is below the threshold level than when it is above the threshold value. Consequently, we obtain a device that can make a sharp demarcation in the cases as described earlier.

## 3-8 ADDITIONAL DIODE CIRCUITS

## 3-8-1 Voltage Multiplier

The voltage multiplier is a passive circuit, similar to the rectifier circuit and gives an output which is approximately equal to a certain multiple of the peak value of the peak input voltage. Here it is possible to obtain a dc voltage equal to the peak value of the applied ac voltage.

The circuit of a half-wave doubler is as shown in Figure 3-34. With terminal $A$ of the ac source assumed positive, diode $D_{2}$ is forward-biased and diode $D_{1}$ is reverse-biased, i.e., open. The diode $D_{2}$ charges the capacitor to the peak supply voltage. In the next half-cycle, the same case is repeated with the second diode, i.e., $D_{1}$, and consequently, as seen from the circuit, the diode $D_{2}$ is reverse-biased. Again, in this case, the capacitor $C_{1}$ charges to its fullest.

Now, the capacitors $C_{1}$ and $C_{2}$ are in series for the dc output circuit; and at no load, the dc voltage is equal to the sum of the positive and negative peaks of the applied voltage. In other words, the output voltage is equal to twice the peaks of the applied voltage. It should be noted, that for the proper operation of the circuit, the input has to be symmetrical.

Another important requirement is that the values of the capacitors $C_{1}$ and $C_{2}$ have to be sufficiently large so that they maintain the voltage level over the intervals in which each diode is conducting.

Similarly, with such designs, various types of multipliers-triplers and quadruplers-can be designed with a proper choice of such components and by suitably connecting them.

## 3-8-2 Peak Detector

The half-wave rectifier circuit can be suitably manipulated to obtain the peak detector circuit. The working principle depends on the charging and discharging of the capacitor, and also on the conducting and non-conducting regions of the diode. Its simple circuit consists of a diode kept in series with a resistor and a load at the end. The circuit of a peak detector is as shown in Figure 3-35.

When the input signal forward-biases the diode, the diode conducts and the voltage is obtained at the load. In this process, the output voltage is available across the capacitor, which in this process charges itself to the full.


Figure 3-35 Peak detector

Again, when the diode is reversebiased, the diode does not conduct, and the input voltage is not obtainable at the output. During this time, because the capacitor is charged to the maximum, it begins to discharge and an almost steady voltage is obtained at the output. This process continues till the input voltage again forward-biases the diode.
In this sequence of steps, the output becomes the envelope of the input voltage. But proper care has to be taken regarding the value of the capacitor. Its time constant has to be properly set so that proper replication of the envelope is obtained. These circuits are used extensively for communication purposes in various detection devices.

## 3-8-3 Digital Circuits

In various kinds of analog to digital converters, and in many digital circuits, diodes are extensively brought to use. Their primary domain of operation is switching, i.e., to keep a portion of a large circuit in the ON state, selectively for a given interval of time. They, in coherent action with resistors, form many important logic families, which are used in digital electronic circuits.

## 3-8-4 Switching Regulators

Power supplies with switching regulators offer great versatility, as the design of power supplies employing this type of regulator can be lighter and more compact. Another advantage of these power supplies is that the circuit can be designed to give an output voltage that is higher than the unregulated voltage or, has a different polarity.

But there is also a disadvantage. The circuit becomes more complex because of the control circuitry, which is the filtering required to remove the switching noise from the output and the electromagnetic interference that can degrade the performance of the device.

Specifically, a switching regulator has two parts: a converter circuit to perform the switching action and a feedback system to control the switching rate. The structure of the converter can be of three types: buck, boost and buck-boost. Let us first study the buck-type converter.

## Buck converter

The basic circuit of the buck converter is as shown in Figure 3-36.
The total output voltage of the supply is $v_{R}=V_{R}+v_{r}$ where, $V_{R}$ is the regulated dc output voltage and $v_{r}$ is a small ac ripple. From Figure 3-36, we find that we have the switches with two voltage controlled devices that can be switched ON and OFF by critically controlling the control voltage $V_{C}$. In Figure 3-36(b), it is seen that the voltage across $L$ is:

$$
\begin{equation*}
v_{L} \approx V_{U}-V_{R} \tag{3-51}
\end{equation*}
$$



Figure 3-36 Various stages in the operation of a buck-type switching converter

While forming Equation (3-51), it is assumed that the capacitor is previously charged to $V_{R}$, the regulated voltage. At this stage we consider $\delta$ to be the duty cycle of the control voltage. This duty cycle has to be chosen very accurately as it figures out the operational performance of the device. Here, in the period $0-\delta T_{S}$, the switch $S_{1}$ is closed and the switch $S_{2}$ is open. After $\delta T_{S}$, both $S_{1}$ and $S_{2}$ are open. Consequently, from Lenz's law-as the inductor must resist the cause of such a change- $v_{L}$ becomes negative, and the inductor tries to maintain the constant current. At this stage, the voltage $v_{L}$ is given by:

$$
\begin{equation*}
\mathrm{v}_{L} \approx-V_{R} \tag{3-52}
\end{equation*}
$$

As the cycle expires, the previous state is restored, resulting in the closing of both $S_{1}$ and $S_{2}$. Figure 3-37 gives the inductor voltage waveform.

Just as the current through the capacitor is zero, so also must be the average voltage across the inductor. Consequently, it can be written as:

$$
\frac{\left(V_{U}-V_{R}\right) \delta T_{S}+\left(-V_{R}\right)(1-\delta) T_{S}}{T_{S}}=0
$$

This gives us:

$$
\begin{equation*}
V_{R}=\delta V_{U} \tag{3-53}
\end{equation*}
$$

To obtain a regulated voltage $V_{R}$ from an unregulated voltage $V_{U}, v_{C}$ must provide the required duty cycle. In order to make $V_{R}$ impervious to the changes in $V_{U}$, we need a feedback circuit to keep track of the output continuously and adjust the duty cycle as and when required.

Let us now turn to the ripple, $V_{r}$. The inductor current is given by $i_{L}=1 / \mathrm{L} \int v_{L}(t) d t$, which is represented in Figure 3-37(b). Also, we note that as the capacitor cannot carry the dc current and consequently the time varying part of $i_{l}$ must flow through the capacitor, therefore:

(a)

(b)

(c)

Figure 3-37 Key waveforms for buck-type converters

$$
v_{L, \mathrm{avg}}=\frac{V_{U}\left(\delta T_{\mathrm{S}}\right)+V_{R}(1-\delta) T_{S}}{T_{S}}=0
$$

Subsequently, on solving this:

$$
\begin{equation*}
V_{R}=\frac{-\delta}{1-\delta} V_{U} \tag{3-54}
\end{equation*}
$$

## Boost converter

The following circuits will also have the previously defined assumptions. The output ripple components can be ignored initially.
$S_{1}$ closes in the $\delta T_{S}$ and is open for the subsequent part of the cycle.
$S_{2}$ closes as soon as $S_{1}$ opens.
The circuit for the basic boost converter is shown in Figure 3-38.

Moving ahead, the average voltage across the inductor leads to:


Figure 3-38 Boost converter

$$
\begin{equation*}
v_{L_{\mathrm{avg}}}=\frac{V_{U}\left(\delta T_{S}\right)+\left(V_{U}-V_{R}\right)(1-\delta) T_{S}}{T_{S}}=0 \tag{3-55}
\end{equation*}
$$

And upon solving Equation (3-55), we obtain the constraint $V_{R}=(1 / 1-\delta) V_{U}$. We also find that as $\delta$ is less than 1 ; and we obtain a boosted output, a higher value at the regulated output.

## Buck-boost converter

The circuit of the buck-boost converter is shown in Figure 3-39.

Applying the principles discussed earlier, we note that in this circuit also the average voltage across the inductor is zero. Therefore:

$$
v_{L, \mathrm{avg}}=\frac{V_{\mathrm{U}}\left(\delta T_{S}\right)+V_{R}(1-\delta) T_{S}}{T_{S}}=0
$$



Figure 3-39 Buck-boost converter

Subsequently, on solving this:

$$
\begin{equation*}
V_{R}=\frac{-\delta}{1-\delta} V_{U} \tag{3-56}
\end{equation*}
$$

As we concentrate, we find that in Equation (3-56), the polarities of $V_{R}$ and $V_{U}$ are always opposite.

## Solved Examples

Example 3-26 By direct integration find the average value of the diode voltage and the load voltage for a diode whose specifications are as given: $V_{m}=2.4 \mathrm{~V}, V_{\gamma}=0.6 \mathrm{~V}, R_{f}=10 \Omega$ and $R_{L}=100 \Omega$. Note that these two answers are numerically equal and explain why?

## Solution:

$$
\varphi=\arcsin \frac{V_{\gamma}}{V_{m}}=\arcsin \frac{1}{4}=14.5^{\circ}
$$

For $a=\frac{\pi}{2}$ :

$$
I_{\max }=\frac{1.8}{110}=16.35 \mathrm{~mA}
$$

Hence, $v_{D \max }=0.6+16.35 \times 10^{-3} \times 10=0.763 \mathrm{~V}$

$$
\begin{aligned}
\overline{v_{L}} & =\frac{1}{T} \int_{0}^{T} i R_{L} d \alpha=\frac{1}{2 \pi} \int_{0}^{2 \pi} i R_{L} d \alpha=\frac{1}{2 \pi}\left(\int_{0}^{\phi} i R_{L} d \alpha+\int_{\phi}^{\pi-\phi} i R_{L} d \alpha+\int_{\pi-\phi}^{2 \pi} i R_{L} d \alpha\right) \\
& =\frac{1}{2 \pi}\left[0+\int_{\phi}^{\pi-\phi} \frac{R_{L}}{R_{L}+R_{f}}\left(V_{m} \sin \alpha-V_{\gamma}\right) d \alpha+0\right] \\
& =\frac{1}{2 \pi} \times \frac{R_{L}}{\left(R_{L}+R_{f}\right)}\left[V_{m} \cos \phi-V_{m} \cos (\pi-\phi)\right]-\frac{1}{2 \pi} \frac{R_{L}}{R_{L}+R_{f}} V_{\gamma}(\pi-\phi-\phi) \\
& =\frac{1}{2 \pi} \times \frac{R_{L}}{R_{L}+R_{f}}\left[2 V_{m} \cos \phi-V_{\gamma}(\pi-2 \phi)\right]
\end{aligned}
$$

When the diode is ON:

$$
v_{D}=V_{\gamma}+i R_{f}=\frac{R_{L}}{R_{L}+R_{f}}\left(V_{m} \sin \alpha+V_{\gamma}\right)
$$

When the diode OFF:

$$
v_{D}=V_{m} \sin \alpha-V_{\gamma}
$$

Hence,

$$
\begin{gathered}
\bar{v}_{D}=\frac{1}{2 \pi}\left[\int_{0}^{\phi}\left(V_{m} \sin \alpha-V_{\gamma}\right) d \alpha+\int_{\phi}^{\pi-\phi} \frac{R_{L}}{R_{L}+R_{f}}\left(V_{m} \sin \alpha-V_{\gamma}\right) d \alpha+\int_{\pi-\phi}^{2 \pi}\left(V_{m} \sin \alpha-V_{\gamma}\right) d \alpha\right] \\
\quad=-\frac{1}{2 \pi} \times \frac{R_{L}}{R_{L}+R_{f}}\left[2 V_{m} \cos \phi-V_{\gamma}(\pi-2 \phi)\right]
\end{gathered}
$$

Since, $v_{i}=v_{D}+v_{L}$ when the diode is ON and $v_{i}=v_{D}+v_{L}=0 \quad$ when the diode is OFF:
or,

$$
\begin{aligned}
& 0= \frac{1}{T} \int_{0}^{\mathrm{T}} v_{i} d t=\frac{1}{T} \int_{0}^{\mathrm{T}} v_{D} d t+\frac{1}{T} \int_{0}^{\mathrm{T}} v_{L} d t \\
& \quad \frac{1}{T} \int_{0}^{\mathrm{T}} v_{D} d t=\overline{v_{D}}=-\frac{1}{T} \int_{0}^{\mathrm{T}} v_{L} d t=-\overline{v_{L}}
\end{aligned}
$$

Example 3-27 For the circuit shown find $I_{1}, V_{1}, I_{2}$, and $V_{2}$. Assume ideal diode.

## Solution:



As $D_{1}$ is also short-circuited, therefore:

$$
\begin{aligned}
I_{1}=\frac{20-V_{i}}{20 \mathrm{~K}}=\frac{20}{20} \times 10^{3} & \\
& I_{1}=1 \mathrm{~mA}
\end{aligned}
$$

As $D_{2}$ is short-circuited, therefore:

$$
\begin{aligned}
& V_{2}=0 \\
& \qquad I_{2}=\frac{V_{2}-(-10)}{20 \mathrm{~K}}=\frac{10}{20}-10^{3} \\
& \quad I_{2}=0.5 \mathrm{~mA}
\end{aligned}
$$

Therefore,

$$
V_{1}=0 \mathrm{~V}
$$

$$
\begin{aligned}
V_{2} & =0 \mathrm{~V} \\
I_{1} & =1 \mathrm{~mA} \\
I_{2} & =0.5 \mathrm{~mA}
\end{aligned}
$$

Example 3-28 Consider the circuit and its $V-1$ characteristics, find voltage across diode $V_{D}$.

## Solution:

From the given figure:


Voltage across diode $V_{D}$.

$$
\begin{aligned}
& V_{D}=I R_{D} \\
&=0.1075 \times 1
\end{aligned}
$$

Therefore,

$$
V_{D}=0.1075 \mathrm{~V}
$$

Example 3-29 A silicon diode is in forward-biased state with constant voltage $V$. Prove that the temperature coefficient of the forward current is given by:

$$
\frac{\left(V_{G o}-V\right)}{\eta_{T} V_{T}}
$$

## Solution:

Forward voltage is given by:

$$
V f=I R f
$$

Forward resistance:

$$
R f=\frac{\eta V_{T}}{I}
$$

The voltage temperature coefficient is given by:

$$
\begin{aligned}
\frac{d V}{d T} & =\frac{V-\left(V_{G o}-\eta V_{T}\right)}{T} \\
R f_{d T}^{d I} & =\frac{V-\left(V_{G o}+\eta V_{T}\right)}{T}+R f
\end{aligned}
$$

Therefore:

$$
\frac{d I}{d T}=\frac{V-\left(V_{G o}+\eta V_{\mathrm{T}}\right)}{T . R f}
$$

Putting up the value of $R f$ :

$$
\frac{d I}{d T}=\frac{V-V_{G o}+\eta V_{T}}{T} \times \frac{I}{\eta V_{T}}
$$

Therefore:

$$
\frac{d I}{d T}=\frac{V_{G o}-V}{\eta V_{T} T}
$$

Example 3-30 The avalanche diode regulates at 50 V . The range of diode current from 5-40 mA. The supply voltage $V_{i}=200 \mathrm{~V}$. Calculate $R$ to allow voltage regulation from a load current of $I_{L}=0$ up to $I_{L \max }$. Hence find $I_{L \max }$.


## Solution:

Given data:

$$
\begin{gathered}
V_{0}=V_{L}=50 \mathrm{~V}(\text { Zener Voltage }) \\
I_{L}=0
\end{gathered}
$$

Diode current ranges from 10 to 40 mA .
Therefore,

$$
I_{D}<40 \mathrm{~mA}=I
$$

Therefore,

$$
R=\frac{V_{A}-V_{B}}{I_{D}}=\frac{200-50}{40 \times 10^{-3}}
$$

$$
\begin{array}{lc} 
& R=3.75 \mathrm{k} \Omega \\
\therefore & I_{L}=I_{\max } \text { when, } I_{D}=I_{D \min }= \\
\therefore \quad \text { Maximum load current is, } I_{L \max } & =40-10 \\
& =30 \mathrm{~mA}
\end{array}
$$

## 3-9 SPECIAL TYPES OF p-n JUNCTION SEMICONDUCTOR DIODES

In this section, we shall discuss the tunnel, light-emitting, photo detector and photovoltaic diodes. These types of diodes find extensive applications in different areas of electronics in general.

## 3-9-1 Tunnel Diode

The tunnel diode is a negative-resistance semiconductor $p-n$ junction diode. The negative resistance is created by the tunnel effect of the electrons in the $p-n$ junction as already discussed in the section of Zener diode. The doping of both the $p$ - and $n$-type regions of the tunnel diode is very high-impurity concentration of $10^{19}$ to $10^{20}$ atoms $/ \mathrm{cm}^{3}$ are used (which means both $n$-type and $p$-type semiconductors having parabolic energy bands are highly degenerate) - and the depletion layer barrier at the junction is very thin, in the order of $10^{-6} \mathrm{~cm}$. Quantum mechanically, if the barrier is less than $3 \hat{\AA}$ there is an appreciable probability that particles will tunnel through the potential barrier even though they do not have enough kinetic energy to pass over the same barrier. In addition to the barrier thinness, there must be filled energy states on one side from which the particles will tunnel and allowed energy states on the other side into which the particles will penetrate through at the same energy level. This phenomenon is called the tunnel effect and the diode that operates on the tunneling phenomena is called a tunnel diode. This is also known as Esaki diode, named so after Leona Esaki who invented this diode in 1956 and later became a Noble laureate in 1973 for this invention. It may be noted that the Figures 3-40(a) to 3-40(e) exhibit the energy band diagram of the tunnel diode under five different conditions which are described as follows.

Step I: This is the equilibrium condition and the Fermi level is constant throughout the junction. The Fermi energy for $p$-type semiconductors $\left(E_{F P}\right)$ lies below the valence band edge on the $p$-side and lies above the


Figure 3-40(a) Tunnel diode under zero bias equilibrium


Figure 3-40(b) Small reverse bias


Figure 3-40(e) Increased forward bias condition where the current begins to increase again.
conduction band edge on the $n$-side (both under the conditions of carrier degeneracy). Thus, the bands must overlap on the energy scale in order for $E_{F}$ to be constant. This overlapping of bands means that with a small reverse-bias or forward-bias, filled states and empty states appear opposite to each other only separated by the width of the depletion region. Under this condition, the upper levels of electron energy of both $p$ - and $n$-type are lined up at the same Fermi level. Since there are no filled states on one side of the junction that are at the same energy level as empty allowed states on the other side, there is no net flow of charge in either direction across the junction, and the current is zero as there is equal tunneling from $n$ to $p$ and from $p$ to $n$ giving a zero net current.
Step II: Since the bands overlap under equilibrium condition, only a small reverse-bias allows electrons to tunnel or move from the filled valence band to the empty conduction band.

This condition is similar to the Zener effect except that no bias is needed to create the condition of overlapping bands. As the reverse-bias is increased, $E_{F P}$ continues to move down on the $n$-region with respect to the $p$-region, placing more filled states on the $p$-side opposite to the empty states on
the $n$-side. The tunneling of electrons from $p$ to $n$ thus, increases with an increase in the reverse-bias. The resulting conventional current is opposite to that of electron flow from $p$ to $n$.
Step III: When a small forward bias is applied $E_{F P}$ moves up in energy on the $n$-side with respect to that on the $p$-side. Thus, electrons below $E_{F P}$ on the $n$-side are placed opposite empty states above $\mathrm{E}_{F P}$ on the $p$ side. Electron tunneling occurs from $n$ to $p$ as shown with the resulting conventional current flowing from $n$ to $p$ as shown.

This type of tunneling continues to increase with increased bias as more filled states are placed opposite empty states.
Step IV: As the voltage is increased, EFP on the $n$-side continues to move up with respect to that on the $p$-type and gradually a condition is reached at which the bands begin to pass by each other. When this occurs, the number of filled states from empty states decreases. The resulting decrease in the current is shown in the I-V characteristics curve.

This region of the I-V characteristics curve is important as it shows the decrease of the tunneling current with increase in the applied forward voltage and hence depicts the negative resistance region; i.e., the dynamic resistance of $d V / d I$ is negative.

Step V: When the applied bias is increased beyond the negative resistance region, the current begins to increase again. Once the bands have passed each other the characteristics resemble that of a conventional diode. The forward current is now dominated by the diffusion current. The diffusion current is present in the forward tunneling region, but it is negligible compared to the tunneling current.

The total tunnel diode characteristics have the general shape of a tilted N ; therefore it is a common practice to refer to the curve as type N negative resistance. It is also called a voltage-controlled negative resistance, which means that the current decreases rapidly at some critical voltage, known as the peak voltage. As the tunneling process is very fast, tunnel diodes can be operated at microwave frequencies. The I-V curve, the symbol and the linear equivalent circuit of the tunnel diode are shown in Figures 3-41(a), (b) and (c) respectively.


Figure 3-41(a) I-V characteristics of a tunnel diode


Figure 3-41(b) Symbol of tunnel diode


Figure 3-41(c) Small-signal model of the tunnel diode. (Typical values for these parameters for a tunnel diode of peak current $I_{P}=10 \mathrm{~mA}$ are $-R_{n}=-30 \Omega, R_{s}=1 \Omega, L_{s}=5 \mathrm{nH}$ and capacitance $C=20 \mathrm{pF}$ respectively).

## 3-9-2 Light-Emitting Diode

Charge carriers recombination takes place at the $p-n$ junction as electron crosses from the $n$-side and recombines with holes on the $p$-side. When the junction is forward-biased the free electron is in the conduction band and is at a higher energy level than the hole located at valence band. The recombination process involves radiation of energy in the form of photons. If the semiconductor material is translucent, the light will be emitted and the junction becomes a light source, i.e., a light-emitting diode (LED). LEDs are $p-n$ junctions that can emit spontaneous radiation in ultraviolet, visible, or infrared regions.

In other words LED is a diode, which generates visible light from the region of the depletion layer when it is forward-biased. $\mathrm{GaAs}_{1-y} \mathrm{P}_{y}$ is the most preferred material for a visible LED. The phosphorus mole fraction in this ternary compound is denoted by $y$, i.e., as $y$ is increased, more and more phosphorus atoms replace arsenic in the crystal lattice. For $0<y<0.45$, the band gap of the material is direct and increases from $1.424 \mathrm{eV}($ at $y=0)$ to 1.977 eV (at $y=0.45$ ). In Si and Ge , greater percentage of released energy is given up in the form of heat and the emitting light is insignificant. The efficiency of light generation increases with an increase in the injected current and with a decrease in temperature. Since LED is a $p-n$ junction device, it has forward current vs forward voltage characteristics similar to that of a diode. LEDs are available in different colours. LEDs have fast response and offer good contrast ratios of visibility. The lifetime of LEDs is high, exceeding 106 hours.

## Advantages of LEDs

1. Low operating voltage, current and power consumption make LEDs compatible with electronic drive circuits.
2. LEDs exhibit high resistance to mechanical shock and vibration and allow them to be used in severe environment conditions.
3. LEDs ensure a longer operating life line, thereby improving the overall reliability and lowering the maintenance costs of equipment.
4. LEDs have low inherent noise levels and also high immunity to externally generated noise.
5. LEDs exhibit linearity of radiant power output with forward current over a wide range.

## Limitations of LEDs

1. Temperature dependence of radiant output power and wavelength.
2. Sensitivity to damages by over voltage or over current.
3. Theoretical overall efficiency is not achieved except in special cooled or pulsed conditions.

## Operation of LEDs

The dominant operating process for LEDs is spontaneous emission. A photon of appropriate energy can be absorbed by a semiconductor, creating an EHP in the process. This is called optical absorption. Let us consider Figure 3-42(a) which depicts two energy levels in a semiconductor $E_{1}$ and $E_{2}$ where $E_{1}$ corresponds to the ground state and $E_{2}$ to the excited state. At room temperature, most of the electrons are in ground state.

When a photon of frequency greater than, or equal to, $v_{12}=\left(E_{2}-E_{1}\right) / h$ is incident on the system, an electron in the ground state absorbs it and goes to the excited state. However, the excited state is unstable. So, after a short time, without any external stimulus, the electron comes back to the ground state emitting a photon of energy $h v_{12}$. The emitted wavelength $\lambda$ is given by:


Figure 3-42 Schematic diagram showing the basic process of (a) absorption and (b) emission

$$
\lambda=\frac{h c}{E_{g}}
$$

where, $E_{g}$ is the band gap of the semiconductor.
This process is referred to as spontaneous emission and is schematically represented in Figure 3-42(b).

Infrared LEDs are used in fibre-optic communication systems where silica fibres are used to guide the optical signal over long distances. An important application of infrared LED is in optoisolators where an input electrical signal is applied to the LED. Light is generated and subsequently detected by a photodiode and converted back to an electrical signal as a current flowing through a load resistor. Opto-isolators allow signal transmission at the speed of light and are electrically isolated. In this context, it may be noted that the emitted wavelength $\lambda$ is given by:

$$
\lambda=\frac{h c}{E_{g}}
$$

where, $E_{g}$ is the band gap of the semiconductor. The probability of direct (radiative) transition is high in direct band gap semiconductors. Hence, $\operatorname{GaAs}_{1-y} \mathrm{P}_{y}(y<0.45)$ is used for light emission in the wavelength range of 627-870 nm. For $y>0.45$, the material has an indirect band gap. So, special recombination centres have to be introduced to facilitate radiative recombination. Incorporation of nitrogen results in the formation of such a recombination centre. It introduces an electron trap level very close to the bottom of the conduction band and greatly enhances the probability of radiative recombination. In general, red LEDs are fabricated on GaAs substrates while orange, green, and yellow LEDs are fabricated on GaP substrates on which a graded $\mathrm{GaAs}_{1-y} \mathrm{P}_{y}$ layer is grown by epitaxy. In optical communications, to take advantage of the $1.3-\mu \mathrm{m}$ and $1.55-\mu \mathrm{m}$ low-loss windows in optical fibers, InGaAsP substrates are used.

At a low forward voltage, the LED current is dominated by the non-radiative recombination current, mostly due to surface recombination. At higher forward voltages, the radiative diffusion current dominates and light is emitted as the injected minority-carriers recombine with the majoritycarriers through a radiative-recombination process. Finally, at very high forward voltages, the series resistance limits the


Figure 3-43 The symbol of an LED current. Figure 3-43 shows the symbol of an LED.

## 3-9-3 Photo Detector Diode

The detector is an essential component of an optical fibre communication system and is one of the crucial elements that dictate the overall system performance. Its function is to convert the received


Figure 3-44 The operation of a p-n photodiode
optical signal into an electrical signal, which is then amplified before further processing. The following criteria define important performance and compatibility for the detectors, which are generally similar to the requirements for the sources:
(i) High sensitivity at the operating wavelengths
(ii) High fidelity
(iii) Large electrical response to the received optical signal
(iv) Short response time to obtain a suitable bandwidth
(v) A minimum noise introduced by the detector
(vi) Stability of performance characteristics
(vii) Small size
(viii) Low bias voltages
(ix) High reliability
(x) Low cost

## Detection principles

The basic detection process in an intrinsic absorber is illustrated in Figure 3-44. The $p-n$ photodiode is reverse-biased and the electric field developed across the $p-n$ junction sweeps mobile carriers (holes and electrons) to their respective majority sides ( $p$ - and $n$-type material). A depletion region or layer is therefore created on either side of the junction. This barrier has the effect of stopping the majority carriers crossing the junction in the opposite direction to the field. However, the field accelerates minority-carriers from both the sides to the opposite side of the junction, forming the reverse leakage current of the diode. Thus, intrinsic conditions are created in the depletion region.

A photon incident in or near the depletion region of this device which has an energy greater than or equal to the band gap energy $E g$, of the fabricating material will excite an electron from the valence band into the conduction band. This process leaves an empty hole in the valence band and is known as the photo-generation of an electron-hole (carrier) pair. Carrier pairs so generated near the junction are separated and swept (drift) under the influence of the electric field to produce a displacement by current in the external circuit in excess of any reverse leakage current. Figures 3-44(a), (b) and (c) illustrate the operation of a $p-n$ photodiode which can be stated briefly as follows:
(i) Photo-generation of an electron hole pair
(ii) Structure of the reversed biased $p-n$ junction illustrating carrier drift in depletion region.
(iii) Energy band diagram of the reversed biased $p-n$ junction

## 3-9-4 Photovoltaic Diode

The photovoltaic diode or solar cell is an important technological device for overcoming energy problems. It is also known as solar energy converter; it is basically a $p-n$ junction diode which converts solar energy into electrical energy. The energy reaching the earth's surface from the sun is primarily electromagnetic radiation, which covers a spectral range of 0.2 to 0.3 micrometre. The conversion of this energy into electrical energy is called photoelectric effect.

## Construction and working principle

A photovoltaic diode essentially consists of a silicon $p-n$ junction diode usually packaged with a glass window on the top. Surface layer of the $p$-material is made extremely thin so that the incident light (photons) can penetrate and reach the $p-n$ junction easily, as shown in Figure 3-45.

When these photons collide with the valence electrons, they impart in them sufficient energy so that they gain enough energy to leave the parent atoms. In this way, free electrons and holes are generated on both sides of the junction. Consequently, their flow constitutes a current (minority current). This current is directly pro-


Figure 3-45 Structure of a solar cell portional to the illumination (lumen $/ \mathrm{m}^{2}$ or $\mathrm{mW} / \mathrm{m}^{2}$ ). This, in general depends on the size of the surface being illuminated. The open circuit voltage $V_{o c}$ is a function of illumination. Consequently, power output of a solar cell depends on the level of sunlight illumination. Power cells are also available in the form of a flat strip so as to cover sufficiently large surface areas.

## Current-voltage characteristics

The current voltage characteristic is shown in Figure 3-46. It is seen that the curve passes through the fourth quadrant and hence the device can deliver power from the curve. We also see that $V_{o c}$ is the maximum voltage obtainable at the load under open-circuit conditions of the diode, and $I_{s c}$ is the maximum current through the load under short-circuit conditions. The power delivered by the device can be maximized by maximizing the area under the curve (see Figure 3-46) or by maximizing the product $\left(I_{s c} \times V_{o c}\right)$. By properly choosing the load resistor, output power can be achieved. In the absence of light, thermally generated minority carriers across the junction constitute the reverse saturation current.

To maximize power, we need to maximize both $I_{s c}$ and $V_{o c}$. This can be done by making both the $p$ - and $n$-side of the junction heavily doped. The fill factor $(F F)$ is defined as $F F=P_{m} / V_{o c} I_{L}$ where $P_{m}$ is the maximum power output of the solar cell. For a well-designed solar cell the $F F$ usually lies between 0.7 and 0.8 . The efficiency of a solar cell can be written as $\eta=V_{m} I_{m} / P_{\text {in }}=F F=V_{o c} I_{L} / P_{\text {in }}$ where $V_{m}$ and $I_{m}$ are the voltage and the current at the point of maximum power, and $P_{\text {in }}$ is the incident optical power.

Thus, to realize a solar cell with high efficiency, it is not only necessary to have high $V_{o c}$ and $I_{s c}$ but also a high $F F$. Solar cells with 15 per cent efficiency are commercially available.


Figure 3-46 I-V characteristics of an illuminated solar cell showing the point of maximum power


Figure 3-47 Top finger contact with anti-reflecting coating

The surface of the solar cell is coated with anti-reflecting coating materials such as $\mathrm{SiO}_{2}, \mathrm{TiO}_{2}$ and $\mathrm{Ta}_{2} \mathrm{O}_{5}$ to obtain better conversion efficiency, as shown in Figure 3-47. Today the solar cell, a nonconventional source of energy of the twenty-first century, has become popular in remote villages and in rural areas. Solar cells are used on board the satellites to recharge their batteries. Since their sizes are small, a large number of cells are required for charging; therefore, series parallel cell combinations are employed for this purpose. Si and Ge are the most widely used semiconductor materials for solar cell but nowadays GaAs is used for better efficiency and better thermal stability.

## Solved Examples

Example 3-31 For the photovoltaic cell whose characteristics are given in Figure 3-45, find out the power output for different values of the load resistance $R_{L}$. What is the optimum value of $R_{L}$ ?

Solution:
The table indicates the Power versus $R_{L}$ chart.

| $R_{L}$ | $I(\mathrm{~mA})$ | $V(\mathrm{~V})$ | $P(\mu \mathrm{~W})$ |
| :--- | :--- | :--- | :--- |
| 0 | 0.145 | 0 | 0 |
| $800 \Omega$ | 0.14 | 0.12 | 15.4 |
| 3.4 K | 0.10 | 0.35 | 34 |
| 10 K | 0.04 | 0.42 | 16.4 |

The optimum value of $R_{L}=3.4 \mathrm{~K} . P=V I=0.35 \mathrm{~V} \times 0.10 \mathrm{~mA}=35 \mu \mathrm{~W}$. The hyperbola intersects the characteristics at one point. And maximum power is generated at one point only.

## 3-10 APPLICATIONS OF DIODE

Inthe following sections, we shallexamine the various applications of the diode. The diode is used in radio demodulation, power conversion, over-voltage protection, logic gates, ionizing radio detectors, chargecoupled devices and measuring temperature,

## 3-10-1 Radio Demodulation

In demodulation of amplitude modulated (AM) radio broadcasts diodes are used. The crystal diodes rectify the AM signal, leaving a signal whose average amplitude is the desired audio signal. The average value is obtained by using a simple filter and the signal is fed into an audio transducer, which generates sound.

## 3-10-2 Power Conversion

In the Cockcroft-Walton voltage multiplier, which converts ac into very high dc voltages, diodes are used. Full-wave rectifiers are made using diodes, to convert alternating current electricity into direct current.

## 3-10-3 Over-Voltage Protection

Diodes are used to conduct damaging high voltages away from sensitive electronic devices by putting them in reverse-biased condition under normal circumstances. When the voltage rises from normal range, the diodes become forward-biased (conducting). In stepper motor, H -bridge motor controller and relay circuit's diodes are used to de-energize coils rapidly without damaging voltage spikes that would otherwise occur. These are called a fly-back diodes. Integrated circuits also use diodes on the pins to protect their sensitive transistors from damaging external voltages. At higher power, specialized diodes are utilized to protect sensitive electronic devices from over-voltages.

## 3-10-4 Logic Gates

AND and OR logic gates are constructed using diodes in combination with other components. This is called diode logic.

## 3-10-5 lonizing Radiation Detectors

In addition to light, energetic radiation also excites semiconductor diodes. A single particle of radiation, having very high electron volts of energy, generates many charge carrier pairs, as its energy is transmitted in the semiconductor material. If the depletion layer is large enough to catch the whole energy or to stop a heavy particle, an accurate measurement of the particle's energy is possible, simply by measuring the charge conducted and excluding the complexity of using a magnetic spectrometer. These semiconductor radiation detectors require efficient charge collection and low leakage current. They are cooled by liquid nitrogen. For longer range (of the order of a centimetre) particles
the requirements are very large depletion depth and large area. Short range particles require any contact or un-depleted semiconductor on at least one surface to be very thin. The back-bias voltages are near breakdown (of the order of a thousand volts per centimetre). Common materials are Ge and Si . Some of these detectors sense both position as well as energy. Due to radiation damage, they have a finite life, especially when detecting heavy particles. Semiconductor detectors for high energy particles are used in large numbers.

## 3-10-6 Temperature Measuring

The forward voltage drop across the diode depends on temperature. A diode can be used as a temperature measuring device. This temperature dependence follows from the Shockley ideal diode equation and is typically around -2.2 mV per degree Celsius.

## 3-10-7 Charge-Coupled Devices

Arrays of photodiode, integrated with readout circuitry are used in digital cameras and similar units.

## POINTS TO REMEMBER

1. A basic diode circuit consists of a diode in series with a voltage source. It mainly corresponds to the inclusion of a diode in the concerned circuit or a diode as a circuit element.
2. The circuit analysis of a diode in a circuit is made simpler by analysing it using the concept of load line.
3. A load line corresponds to the basic equation of the circuit concerned. It mainly deals with the relation of the voltage across the diode and the current flowing through it.
4. A load line actually has an impact on the region of operation of the device. It is an analysis performed in a graphical mannera line drawn on the characteristics of the device that represents the applied load.
5. The intersection of the load line with the characteristic curve of the device determines the point of operation.
6. Dynamic load line can be obtained from different load resistances. This dynamic load
line is important because with the help of this, we can directly obtain the diode current for any given input voltage, as the corresponding current can be obtained from the graph.
7. The principle behind the use of the Zener diode as a voltage regulator is the fact that it maintains a constant output voltage even though the current through it changes. For proper operation, the voltage of an unregulated power supply must be greater than the Zener voltage of the diode selected. If the input voltage is less, the diode does not conduct.
8. A rectifier mainly works on the principle of conduction through the diode, i.e., it conducts when forward-biased, and not when reversebiased. Depending on the design of the circuit, two types of rectifiers result-halfwave rectifiers and full-wave rectifiers.
9. In case of half-wave rectifiers, diode conducts for only one half-cycle of the input signal till the diode is forward-biased. Also,
the rectified voltage appearing at the load is 0.7 V less than the input signal, the loss owing to the cut in the voltage of the diode concerned.
10. Depending upon the design implemented, two different types of rectifiers result:
(a) Centre-tapped transformer rectifiers that use a bulky centre tapped transformer with three terminals and two diodes.
(b) Bridge-rectifiers use a lightweight, simple transformer with four diodes in the circuit.
11. Advantages of a bridge rectifier:
(a) A transformer without a centre tap can be used in a bridge circuit.
(b) Since both the primary and the secondary currents in the transformer are sinusoidal, the bridge circuit requires a smaller transformer than that needed by a full-wave rectifier giving the same dc output voltage.
(c) The peak inverse voltage rating of a diode in a bridge rectifier is half of that of a full-wave circuit yielding the same dc output voltage. The bridge circuit is therefore suitable for high voltage applications.
(d) Crystal diodes are usually used to construct the bridge rectifier and the assembly of four such diodes is available in the market in a block form. The bridge circuit is therefore more compact and cheaper.
12. Disadvantages of the bridge rectifier:
(a) A full-wave rectifier uses two diodes whereas a bridge rectifier uses four diodes.
(b) Since the current flows through two diodes in a series in a bridge circuit, a large power is dissipated in the diodes. Hence, the bridge is not efficient for the low voltages.
(c) Vacuum diodes with directly heated cathodes are not convenient for a bridge circuits because the cathodes for the diodes do not have the same potential.

Hence, they cannot be connected in parallel across a transformer secondary meant for a filament supply. Bridge circuits generally employ Se and copper oxide rectifiers.
13. Comparison between half- and full-wave rectifiers:
(a) In a half-wave rectifier, a single diode exists and the load current flows through it for only the positive half-cycle. On the other hand, in a full-wave rectifier, the current flows throughout the cycles of the input signals.
(b) In a full-wave rectifier, we usually require a centre-tapped transformer. For a halfwave rectifier, only a simple transformer is required.
(c) The peak inverse voltage in a half-wave rectifier is the maximum voltage across the transformer secondary. Whereas in the case of full-wave rectifier, the PIV for each diode is two times the maximum voltage between the centre tap and at the either end of the transformer secondary.
(d) In the case of a half-wave rectifier, the frequency of the load current is the same as that of the input signal and it is twice the frequency of the input supply for a full-wave rectifier.
(e) The dc load current and conversion efficiency for a full-wave rectifier is twice that of a half-wave rectifier. Also, we see the ripple factor of the full-wave rectifier is less than that of the half-wave circuit. This indicates that the performance of the full-wave rectifier is better than the half-wave rectifier.
(f) In a full-wave rectifier two diode currents flow through the two halves of
the centre-tapped transformer secondary in opposite directions, so that there is no direct current magnetization of the core. The transformer losses being smaller, a smaller transformer can be used for a full-wave rectifier. This is an important advantage of the half-wave rectifier over a full-wave rectifier.
14. Filters form an integral part of a rectifier for obtaining a regulated, steady dc output at the end of a rectifier.
15. Clipper is a type of diode circuit where the diode network is able to clip off a portion of the input signal without disturbing the remaining portion of the input signal.
16. A clamper circuit clamps a signal to a different dc level. The network must have a capacitor, a diode, a resistive network and should also employ an independent voltage source which introduces an additional voltage shift.
17. Comparators are circuits that employ diode for comparisons between two different input voltages. The basic principle on which the comparator works is the switching of the diodes i.e., the action corresponding to the portion when the diode conducts and when it does not.
18. The recombination process involves radiation of energy in the form of photons or leaf. If the semiconductor material is translucent, the light will be emitted and the junction becomes a light source i.e., a light emitting diode (LED).
19. Photo detector diodes accept light (optical signal) as input and produces corresponding current as output, which varies proportionally with the intensity of the incident light. The resultant current is amplified before it is passed as output.

## IMPORTANT FORMULAE

1. For a simple diode circuit with a diode connected in series with a resistor and a voltage source, the equation governing the behaviour of the circuit is given by:

$$
V_{a}=V-i R_{L}
$$

2. Average value of load current is given by:

$$
I_{d c}=\frac{1}{2 \pi} \int_{0}^{2 \pi} i_{L} d(\omega t)
$$

3. Ripple factor is given by:

$$
\gamma=\frac{\left(I_{r m s}{ }^{2}-I_{d c}{ }^{2}\right)^{1 / 2}}{I}=\frac{\left(V_{r m s}{ }^{2}-V_{d c}{ }^{2}\right)^{1 / 2}}{V_{d c}}
$$

4. Rectification efficiency is given by:

$$
\eta=\frac{P_{d c}}{P_{i}} \times 100 \%=\left(\frac{I_{d c}{ }^{2}}{I_{r m s}{ }^{2}}\right) \frac{1}{1+\frac{R_{f}}{R_{L}}} \times 100 \%
$$

5. For a half-wave rectifier:

$$
\begin{aligned}
I_{d c} & =\frac{I_{m}}{\pi} \\
I_{r m s} & =\frac{I_{m}}{\sqrt{2}} \\
\gamma & =\left[\left(\frac{I_{r m s}}{I_{d c}}\right)^{2}-1\right]^{1 / 2}=1.21 \\
\eta & =\frac{40.6}{1+R_{f} / R_{L}} \%
\end{aligned}
$$

6. For a full-wave rectifier:

$$
\begin{aligned}
I_{d c} & =\frac{2 I_{m}}{\pi} \\
I_{r m s} & =\frac{I_{m}}{\sqrt{2}} \\
\gamma & =0.482 \\
\eta & =\frac{81.2}{1+R_{f} / R_{L}} \%
\end{aligned}
$$

7. Percentage voltage regulation:
$\frac{V_{N L}-V_{R L}}{V_{R L}} \times 100 \%$

## OBJECTIVE QUESTIONS

1. A More Zener diode is based on the principle of:
(a) Thermionic emission
(b) Tunneling of charge carriers across the junction
(c) Diffusion of charge carriers across the junction
(d) None of the above
2. Silicon diode is less suited for low voltage rectifier operation because:
(a) Its breakdown voltage is high
(b) Its reverse saturation current is low
(c) Its cut-in voltage is high
(d) None of the above
3. Silicon is not suitable for fabrication of lightemitting diodes because it is:
(a) An indirect band gap semiconductor
(b) A direct band gap semiconductor
(c) A wide band gap semiconductor
(d) None of the above
4. For an abrupt junction Varactor diode, the dependence of the device capacitance $(C)$, an applied reverse-bias $(V)$ is given by:
(a) $C \propto V l / 3$
(b) $C \propto V I / 2$
(c) $C \propto V-I / 3$
(d) None of the above
5. A Zener diode:
(a) Has a high forward voltage rating
(b) Has a sharp breakdown at low reverse voltage
(c) Is useful as an amplifier
(d) None of the above
6. Which of these is a best description of a Zener diode?
(a) It operates in the reverse region
(b) It is a constant voltage device
(c) It is a constant current device
(d) None of the above
7. When two Zener diodes each of 10 V and 15 V are connected in series, then the overall voltage between them when they are in conduction is
(a) 10 V
(b) 25 V
(c) 15 V
(d) Zero
8. In a standard regulator circuit that uses Zener diode 10 V , the input voltage varies from 25 to 40 V , load current varies from 10 to 20 mA , and the minimum Zener current is 5 mA , the value of the series resistance in ohms will be:
(a) 1500
(b) 1200
(c) 600
(d) None of the above
9. The LED is usually made of materials like:
(a) GaAs
(b) C and Si
(c) GeAs
(d) None of the above
10. Varactor diodes are used in FM receivers to obtain:
(a) Automatic frequency control
(b) Automatic gain control
(c) Automatic volume control
(d) None of the above
11. No-load voltage of power supply is 100 V and full-load voltage is 80 V , the percentage of regulation is:
(a) 0
(b) 25
(c) 15.75
(d) None of the above
12. Zener diodes are used as:
(a) Reference voltage elements
(b) Reference current elements
(c) Reference resistance
13. Zener diodes are:
(a) Specially doped $p-n$ junction
(b) Normally doped $p-n$ junction
(c) Lightly doped $p-n$ junction
(d) None of the above
14. Silicon diode is less suited for low voltage rectifier operation because:
(a) It can withstand high temperatures
(b) Its reverse saturation current is low
(c) Its breakdown voltage is high
(d) None of the above
15. Silicon is not suitable for fabrication of light emitting diodes because it is:
(a) An indirect band gap semiconductor
(b) A direct band gap semiconductor
(c) A wide band gap semiconductor
(d) None of the above
16. In an abrupt junction Varactor diode, the dependence of the device capacitance $(C)$ and applied reverse-bias $(V)$ is given by:
(a) $C \propto V l / 3$
(b) $C \propto V I / 2$
(c) $C \propto V-I / 3$
(d) None of the above
17. A general propose diode is more likely to suffer an avalanche breakdown rather than a Zener breakdown because:
(a) It is lightly doped
(b) It is heavily doped
(c) It has weak covalent bonds
(d) None of the above
18. A Zener diode:
(a) Has a high forward voltage rating
(b) Is useful as an amplifier
(c) Has a sharp breakdown at low reverse voltage
(d) None of the above.
19. If the junction temperature of LED is increased the radiant output power:
(a) Decreases
(b) Increases
(c) Remains the same
(d) None of the above
20. The Zener effect is valid approximately:
(a) Below 5 V
(b) Above 5 V
(c) Equal to 5 V
(d) None of these
21. Each diode of full-wave centre-tapped rectifier conducts for:
(a) $360^{\circ}$
(b) $270^{\circ}$
(c) $90^{\circ}$
(d) $180^{\circ}$
22. When a capacitor filter is used, the PIV for a half-wave rectifier:
(a) Increases
(b) Decreases
(c) Remains unaltered
(d) None of the above
23. The transfer characteristics of a diode relates to:
(a) The diode current and the input voltage
(b) The diode current and the output voltage
(c) The output voltage and the input voltage
(d) None of the above
24. The clipping action of a diode requires that its forward resistance:
(a) Be zero
(b) Have a finite value
(c) Be infinite
(d) None of the above
25. For a low voltage rectification:
(a) Two diode full-wave rectifier is suitable
(b) Both bridge and full-wave rectifier are suitable
(c) Bridge rectifier is suitable
(d) None of the above
26. If $V_{m}$ is the peak value of an applied voltage in a half-wave rectifier with a large capacitor across the load, then PIV is:
(a) $V_{m}$
(b) $V_{m} / 2$
(c) $2 V_{m}$
(d) None of the above
27. The induction filter is mostly used for rectifiers with:
(a) Half-wave rectifiers
(b) Light loads
(c) High loads
(d) None of the above
28. The most significant component of ripple voltage in a half-wave rectifier is contained in:
(a) Fundamental frequency
(b) Second harmonic
(c) DC component
(d) None of the above
29. The disadvantages of capacitor input $L C$ filter are:
(a) High cost, more weight and external field produced by a series inductor
(b) High cost, less weight
(c) Low cost, more weight
(d) None of the above
30. Larger the value of the capacitor filter:
(a) Smaller the dc voltage across the load
(b) Longer the time that current pulse flows through the diode
(c) Larger the peak current in the rectifying diode
(d) None of the above

31 . Which rectifier requires four diodes?
(a) Half-wave voltage doublers
(b) Full-wave voltage doublers
(c) Full-wave bridge circuit
(d) None of the above

## REVIEW QUESTIONS

1. What is the dynamic characteristic of a diode? How can you obtain it from the dynamic characteristics?
2. What is a load line in connection with a diode connected to a supply voltage through a series load resistance? How does the load line change with the change of the supply voltage, the load resistance, and the type of diode?
3. What do you mean by rectification? How can you study the performance of the diode rectifier with the help of its dynamic characteristic?
4. Draw the circuit diagram of a half-wave rectifier and explain the operation of the circuit.
5. Draw the circuit of a full-wave rectifier and explain the operation of the circuit.
6. Distinguish between the following:
(a) Full-wave rectifier and half-wave rectifier
(b) Full-wave rectifier and bridge rectifier.
7. Draw the waveforms of the diode current and the load voltage for a sinusoidal input voltage applied to
(a) Half-wave rectifier
(b) Full-wave rectifier

Is it necessary for the two diodes of the rectifier to be identical?
8. Draw the circuit diagram of a full-wave rectifier using junction diodes and explain clearly its action.
9. Discuss how a semiconductor diode can be used as a rectifier. Do you prefer a valve diode or a junction diode for rectification?
10. Explain the phenomena of a bridge rectifier with the help of a circuit diagram. Mention its advantages and disadvantages when compared with a full-wave rectifier with a centre-tapped transformer.
11. Explain the term peak inverse voltage in connection with a diode rectifier. Is it different for half and full-wave rectifiers with a centre tap? Does it change if we use a capacitor filter?
12. Define the following terms:
(a) dc load current
(b) Ripple factor
(c) Conversion efficiency
13. For a half-wave rectifier, calculate
(a) The dc load current
(b) The peak load current
(c) The rms load current
(d) The rms value of ripple current
(e) The ripple factor
(f) The dc power output
(g) The efficiency of the rectifier
14. What do you mean by the regulation characteristics of a rectifier? Figure out the main quantity determining the regulation characteristics. Define percentage voltage regulation.
15. Explain the significance of percentage voltage regulation. Find the percentage voltage regulation for both the half and full-wave rectifiers.
16. Why is a filter used in a rectifier? Enumerate the different types of filters used at the output of the rectifiers.
17. Explain how the dc voltage of a full-wave rectifier is improved when a capacitor filter is used. Draw waveforms of the load voltage and the diode current.
18. Derive expressions of the percentage regulation for a half-wave, full-wave and a bridge rectifier circuit each employing the same capacitor and the same load resistance.
19. What is a voltage multiplier? Draw the circuit diagram of a half-wave voltage doubler and explain its operation. What is the advantage of the circuit?
20. What is the function of the clipping circuit? Draw the circuit diagram of a diode clipper
that limits the positive peak of the input voltage. Explain how the circuit works.
21. Draw the neat diagram of a full-wave voltage doubler and explain its operation. How can you construct a voltage tripler?
22. What is the transfer characteristic of a diode? What is the utility of this characteristic?
23. Explain the working of a diode clipper that limits the lower portion of the input voltage.
24. What is a double diode clipper? Draw the circuit diagram of a double diode clipper and explain.
25. What do you understand by a clamping circuit? Draw the circuit diagram of a dc restorer. How does the circuit function?
26. Explain the working principle of tunnel diode.
27. Explain the basic working of a light emitting diode.
28. Explain the advantages and disadvantages of a light emitting diode.
29. Explain the working principle of a photo detector.
30. What are the advantages and disadvantages of a photo detector?
31. What are the basic criterions to be fulfilled by a photo detector?
32. Explain with diagrams the V-I curve of the following:
(a) Tunnel diode
(b) Light-emitting diode
(c) Photo detector diode
(d) Solar cell

## PRACTICE PROBLEMS

1. A 1 mA diode (i.e., one that has $v_{D}=0.7 \mathrm{~V}$ at $I_{D}=1 \mathrm{~mA}$ ) is connected in series with a $200 \Omega$ resistor to a 1 V supply. Provide a rough estimate of the diode current.

If the diode is characterized by $n=2$, estimate the diode current closely using iterative analysis.
2. Assuming the availability of the diodes for which $v_{D}=0.7 \mathrm{~V}$ and $I_{D}=1-\mathrm{mA}$ and $n=1$, design a circuit that utilizes four diodes in series with a resistor $R$ connected to ac 15 V power supply. The voltage across the string of diodes is to be 3.0 V .
3. Find the parameters of a piecewise-linear model of a diode, for which $v_{D}=0.7 \mathrm{~V}$ at $I_{D}=1-\mathrm{mA}$ and $n=2$. The model is to fit exactly at $1-\mathrm{mA}$ and 10 mA . Calculate the error-in millivolts-in predicting $v_{D}$, using the linear piecewise-linear model at $I_{D}$ at 0.5 , 5 and 14 mA .
4. A junction diode is operated in a circuit in which it is supplied with a constant current $I$. What is the effect on the forward voltage of the diode if an identical diode is connected in parallel? Assume $n=1$.
5. A diode measured at two operating currents, 0.2 mA and 10 mA , is found to have corresponding voltages 0.650 and 0.750 . Find the values of $n$ and $I_{s}$.
6. A diode for which the forward voltage drop is 0.7 V at 1.0 mA , and for which $n=1$, is operated at 0.5 V . What is the value of the current?
7. When a $10-\mathrm{A}$ current is applied to a particular diode it is found that the junction voltage immediately becomes 700 mV . However, as the power being dissipated in the diode raises its temperature, it is found that the voltage decreases and eventually reaches 600 mV . What is the apparent rise in junction temperature? What is the power dissipated in the diode in its final state? What is the temperature rise per watt of power dissipation?
8. The small-signal model is said to be valid for voltage variations of about 10 mV . To what percent current change does this correspond for:
(i) $n=1$
(ii) $n=2$
9. What is the incremental resistance of ten 1 mA diodes connected in parallel and fed with a dc current 10 mA . Let $n=2$.
10. In the circuit given, $I$ is the dc current and $v_{S}$ is the sinusoidal signal. Capacitor $C$ is very large; its function is to couple the signal to the diode but block the dc current from the
source. Use the diode small signal model to show that the signal component of the output voltage is:

$$
v_{o}=v_{S} \frac{n V_{T}}{n V_{T}+I R_{S}}
$$

If $v_{S}=10 \mathrm{mV}$, find $v_{o}$ for $I=1 \mathrm{~mA}, 0.1 \mathrm{~mA}$ and $1 \mu \mathrm{~A}$. Let $R_{S}=1 \mathrm{k} \Omega$ and $n=2$. At what value of $I$ does $v_{o}$ become one half of $v_{s}$ ?

11. Construct circuits which exhibit terminal characteristics as shown in parts (a) and (b) of the given figure.

(a)

(b)
12. At what forward voltage does a diode for which $n=2$ conduct a current equal to $1000 I_{S}$ ? In terms of $I_{S}$, what current flows in the same diode when its forward voltage is 0.7 V ?
13. A diode modeled by the $0.1 \mathrm{~V} /$ decade approximately operates in a series circuit with $R$ and $V$. A designer, considering using a constant voltage model, is uncertain whether to use 0.7 V or 0.5 V for $V_{D}$. For what value of $V$ is the difference only $1 \%$ ? For $V=2 \mathrm{~V}$ and $R=1 \mathrm{~K}$, what two currents would result from the use of the two values of $V_{D}$ ?
14. The circuit in the given figure utilizes three identical diodes having $n=1$ and $I_{S}=10^{-14} \mathrm{~A}$. Find the value of the current $I$ required to obtain an output voltage $V_{o}=2 \mathrm{~V}$. If a current of 1 mA is drawn away from the output terminal by a load, what is the change in output voltage?

15. Assuming that the diodes in the circuits of the given figure are ideal, utilize Thevenin's theorem to simplify the circuits, and thus,
find the values of the labeled currents and voltages.

(a)

(b)
16. For the rectifier circuit as given, let the input sine wave have 120 V rms value, and assume the diode to be ideal. Select a suitable value for $R$ so that the peak diode current does not exceed 0.1 A . What is the greatest reverse voltage that will appear across the diode?

17. For the logic gate as shown in the following figure, assume ideal diodes and input voltage levels of 0 and +5 V . Find a suitable value for $R$ so that the current required from each of the input signal sources does not exceed 0.2 mA .

18. Consider the voltage regulator circuit as shown in the following figure, under the condition that a load current $I_{L}$ is drawn from the output terminal. Denote the output voltage across the diode by $V_{o}$. If the value of $I_{L}$ is sufficiency small so that the corresponding change in the regulator output voltage $\Delta V_{o}$ is small enough to justify using the diode small signal model, show that:

$$
\pm \frac{\Delta V_{0}}{I_{L}}=-\left(r_{d} / / R\right)
$$

(Note: This quantity is known as the load regulation and is usually expressed in $\mathrm{mV} / \mathrm{mA}$.)
19. In the above problem, if the value of $R$ is selected such that at no load the voltage across the diode is 0.7 V and the diode current is $I_{D}$, show that the expression derived becomes:

$$
\frac{\Delta V_{0}}{I_{L}}=\frac{n V_{T}}{I_{D}} \frac{V^{+}-0.7}{V^{+}-0.7+n V_{T}}
$$

Select the lowest possible value for $I_{D}$ that results in a load regulation $<=5 \mathrm{mV} / \mathrm{mA}$. Assume $n=2$. If $\mathrm{V}^{+}$is nominally 10 V , what value of $R$ is required?
20. With reference to the Problem 18 and 19, generalize the expression derived in Problem 19 for the case of M diodes connected in series and $R$ adjusted to obtain $V_{o}=0.7 \mathrm{mV}$, at no load.
21. A voltage regulator consisting of a 6.8 V Zener diode, a 100 ohm resistor, and intended for operation with a 9 V supply is accidentally connected to 15 V supply instead. Assuming the $r_{Z}$ is very small; calculate the expected values of Zener current and the power dissipated in both the Zener diode and the resistor, for both the normal as well as aberrant situations. Also compare the ratios.
22. A shunt regulator utilizing a Zener with an incremental resistance of 6 ohms is fed through an 82 ohms resistor. If the raw supply changes by 1.4 V , what is the corresponding change in the regulated output voltage?
23. A 9.1 V Zener diode exhibits its nominal voltage at a current of 28 mA . At this current the incremental resistance is specified as 5 ohms. Find $V_{z o}$ of the Zener model. Find the Zener voltage at a current of 10 mA and at 100 mA .
24. Consider a half-wave peak rectifier fed with a voltage $v_{S}$ having a triangular waveform with 20 V peak to peak amplitude, zero average and 1 Khz frequency. Assume that the diode has a 0.7 V drop when conducting. Let the load resistance $R=100 \Omega$ and the filter capacitor $C=100 \mu \mathrm{~F}$. Find the average dc output voltage, the time interval during which the diode conducts-the average diode current during conduction, and the maximum diode current.
25. Sketch the transfer characteristics $V_{o}, V_{s}$, $V_{I}$ for the limiter circuits as shown in the following figures. All diodes start conducting at a forward voltage drop of 0.5 V and display voltage drops of 0.7 V when fully conducting.

26. In the figure provided, (a) and (b) are connected as follows: The two input terminals are tied together, and the output terminals are tied together. Sketch the transfer characteristic of the resulting circuit, assuming that the cut in voltage of the diodes is 0.5 V and their voltage drop when fully conducting is 0.7 V .

(a)

(b)
27. Plot the transfer characteristics of the circuit as shown in the following figure by evaluating $V_{I}$ corresponding to $V_{o}=0.5 \mathrm{~V}, 0.6 \mathrm{~V}$,
$0.7 \mathrm{~V}, 0.8 \mathrm{~V}, 0 \mathrm{~V},-0.5 \mathrm{~V},-0.6 \mathrm{~V},-0.8 \mathrm{~V}$. Assume that the diodes are 1 mA units having a $0.1 \mathrm{~V} /$ decade logarithmic characteristi(c) Characterize the circuit as a hard or a soft limiter. What is the vale of $K$ ? Estimate $L_{+}$and $L$.
28. A clamped capacitor using an ideal diode is supplied with a sine wave of $10-\mathrm{V}$ rms. What is the average dc value of the resulting output?
29. Design limiter circuits using only diodes and $10 \mathrm{k} \Omega$ resistors to provide an output signal limited to the range:
(a) -0.7 V and above
(b) -2.1 V and above
(c) $\pm 4.1 \mathrm{~V}$

Assume that each diode has a 0.7 V drop when conducting.

## SUGGESTED READINGS

1. Millman, J. and H. Tau(b) 1965. Pulse, Digital, and Switching Waveforms. New York: McGraw-Hill Book Company.
2. Boylsted, R. and L. Nashelsky. 2007. Electronic Devices and Circuit Theory. New Delhi: Pearson Education.

## 4

## BJT Fundamentals

## Outline

4-1 Introduction
4-2 Formation of $p-n-p$ and $n-p-n$ Junctions
4-3 Transistor Mechanism
4-4 Energy Band Diagrams
4-5 Transistor Current Components
4-6 CE, CB, CC Configurations
4-7 Expression for Current Gain
4-8 Transistor Characteristics

4-9 Operating Point and the Concept of Load Line<br>4-10 Early Effect<br>4-11 Transistor as Amplifier<br>4-12 Expressions of Current Gain, Input Resistance, Voltage Gain and Output Resistance<br>4-13 Frequency Response for CE Amplifier with and without Source Impedance<br>4-14 Emitter Follower

## Objectives

This chapter introduces one of the most important semiconductor devices, the bipolar junction transistor. This is followed by a discussion on the formation of the $p-n-p$ and $n-p-n$ junctions. Transistor mechanism and energy band diagrams are examined in detail. Transistor current components for $p-n-p$ and $n-p-n$ transistors are provided, and subsequently the CE, CB, CC configurations of transistors are explained. The chapter ends with a discussion on the Ebers-Moll model of a transistor, the transistor characteristics, the concept of load line, and Early effect.

## 4-1 INTRODUCTION

With the advent of junction transistors, leading to the first Nobel Prize in electronics to William Shockley, Walter Brattin and John Bardeen in 1956, the modern electronic era begins in the real sense of the term. The junction transistors are listed at the top among all the amplifying semiconductor devices. They form the key elements in computers, space vehicles and satellites, and in all modern communications and power systems.

A bipolar junction transistor (BJT) is a three-layer active device that consists of two $p-n$ junctions connected back-to-back. Although two $p-n$ junctions in a series is not a transistor since a transistor is an active device whereas a $p-n$ junction is a passive device. Besides, their designs are also different. A BJT is actually a current-amplifying device. In a BJT, the operation depends on the active participation of both the majority carrier, and the minority carrier; hence, the name "bipolar" is rightly justified.


Figure 4-1(a) $p-n-p$ transistor


Figure 4-1 (b) $n-p-n$ transistor

## 4-2 FORMATION OF $p-n-p$ AND $n-p-n$ JUNCTIONS

When an $n$-type thin semiconductor layer is placed between two $p$-type semiconductors, the resulting structure is known as the $p-n-p$ transistor. The fabrication steps are complicated, and demand stringent conditions and measurements. When a $p$-type semiconductor is placed between two $n$-type semiconductors, the device is known as the $n-p-n$ transistor. Both these types of transistors are shown in Figure 4-1(a) and Figure 4-1(b) respectively.

## 4-3 TRANSISTOR MECHANISM

The basic operation of the transistor is described using the $p-n-p$ transistor. The $p-n$ junction of the transistor is forward-biased whereas the base-to-collector is without a bias, as shown in the Figure 4-2.

The middle portion is termed as the base ( $B$ ) while the two end portions are known as the emitter $(E)$ and the collector $(C)$. The junction between the emitter and the base is called the emitter-base junction, or the emitter junction $\left(J_{E}\right)$. The junction between the collector and the base is called the collector-base junction, or briefly the collector junction $\left(J_{C}\right)$.

The depletion region gets reduced in width due to the applied bias, resulting in a heavy flow of majority carriers from the $p$-type to the $n$-type material gushing down the depletion region and reaching the base. The forward-bias on the emitter-base junction will cause current to flow. This flow of current consists of two components: (i) holes injected from emitter to base and (ii) electrons injected from base to emitter. The design of the transistor ensures that the base region is fabricated very lightly compared to the emitter or the


Figure 4-2 Forward-biased junction of a $p-n-p$ transistor


Figure 4-3 Reverse-biased junction of a $p-n-p$ transistor
collector regions. Consequently, we have the holes injected from the emitter into the base in large numbers, and we neglect the injection of electrons from the base region.

For easy analysis, let us now remove the base-to-emitter bias of the $p-n-p$ transistor, as shown in the Figure 4-3.

The flow of majority carriers is zero, resulting in a minority-carrier flow. Thus, one $p-n$ junction of a transistor is reverse-biased, while the other is kept open. The operation of this device becomes much easier when they are considered as separate blocks. In this discussion, the drift currents due to thermally generated minority carriers have been neglected, since they are very small.

## 4-4 ENERGY BAND DIAGRAMS

Since a transistor can be seen as two $p-n$ diodes connected back-to-back, the bending of the energy levels will take place-as is evident from the concepts of diodes-under both forward- and reversebiased conditions. Under equilibrium conditions, the bending will be such that the Fermi level will


Figure 4-4 State of energy bands under (a) no bias (b) forward-biased state (c) reverse-biased state
remain at par for both the emitter and the base regions. Similarly, for the collector and the base regions, the energy levels will bend sufficiently for the alignment of the Fermi level. If further bias is applied, respective changes will take place at both the junctions.

If the emitter-base junction is forwardbiased, the barrier potential is decreased and can be expressed as $V_{b i}-V_{f}$ where, $V_{b i}$ is the barrier potential difference and $V_{f}$ is the applied voltage across the junction, due to reverse-bias of the collector-base junction there is an increase in the barrier potential in the collector-base junction. The changes in the barrier potential and energy levels for both unbiased and biased transistors have been shown in Figure 4-4.

The energy band diagram of an $n-p-n$ bipolar transistor under zero bias and forward-mode bias is shown in the Figure 4-5.


Figure 4-5 Bending of the energy states under no bias and forward-bias

Thus, the basic transistor operation can be described as the state when the transistor is biased in the forward-active mode of operation. The current at one terminal of the transistor (collector-current) is controlled by the voltage applied across the other two terminals of the transistor (base-emitter voltage).

## 4-5 TRANSISTOR CURRENT COMPONENTS

The transistor current components in a non-degenerate $p-n-p$ transistor can be formulated from Figure 4-6.

Since the emitter junction is connected to the positive pole of the battery $V_{E E}$, which makes the emitter base region forward-biased, the majority carriers (holes) from the $p$-side diffuse into the base region ( $n$-type). From Figure 4-6 we can state that for a forwardbiased $p-n$ junction, with collector-base open circuited, a forward current flows in the hole direction, i.e., from $p$-side (emitter) to $n$-side (base), and hence is termed as the emitter current $I_{E}$. In the base region, the holes coming from the $p$-side act as minority carriers, which


Figure 4-6 Transistor with forward-biased emitter junction and open-collector junction have a large probability of meeting an electron in the base. In such a case, both the electron and hole disappear, forming a covalent bond. This act is highly dependent on the doping levels as well as on the temperature in the base region. This whole process of the hole meeting an electron is known as recombination. The electrons and holes that have been lost in the base region are supplied externally by the $V_{E E}$ through the base lead.

With the collector-base region connected through the $V_{C C}$ voltage source in reverse-bias mode, the whole situation takes a different twist. When this is done, the holes that have entered the base region and act as minority carriers "see" a reverse-biased system and thus, get swept by the negative polarity of the voltage $V_{C C}$. This is also valid for the electrons present in the $p$-side collector region. These electrons migrate from $p$-side (collector) to $n$-side (base), and consequently are also swept out by the positive pole of the voltage source $V_{C C}$. These currents that take part in the reverse-biased collector-base region are the reverse saturation currents. The effect of recombination can be dealt with by using the following example. Let us suppose that the emitter region ( $p$-side) transmits 8 holes to the base region ( $n$-side). Now, the doping level of the base region is such that for every 8 holes 2 electrons supplied by the base recombine 2 holes. In such a case $8-2=6$ holes reach the collector region. These two holes contribute to the reverse collector saturation current. Evidently, to increase the amount of current in the collector region, a lower amount of recombination requires to be done in the base. This is achieved by lowering the doping level of the base region, and narrowing the base width. In such a case most of the holes get transmitted to the collector region, thus, increasing the reverse collector saturation current.

Now consider two cases:
(i) When the collector side is open-circuited: In such a case only the emitter current $I_{E}$ flows from emitter to base and to the voltage source $V_{E E}$.
(ii) When the collector side is closed: In such a case recombination occurs in the base creating the recombination current $I_{E \text { minority }}$ plus $I_{E \text { majority }}$. Thus:

$$
\begin{equation*}
I_{E}=I_{E \text { majority }}+I_{E \text { minority }} \tag{4-1}
\end{equation*}
$$

Now, $I_{E \text { majority }}$ when transferred to $p$-region from the base gets converted to $I_{C \text { majority }}$ and the minority carriers due to the open-circuited emitter-base region flow from $n$-side (base) to $p$-side (collector). This minority carrier is of a very low magnitude - in the order of microamperes for silicon and nanoamperes for germanium - and is designated as $I_{C O}$ where "O" implies open-circuited emitter-base terminal. Thus, we can write:

$$
I_{E \text { majority }}=I_{C \text { majority }}
$$

Hence the current coming out of the collector region:

$$
\begin{equation*}
I_{C}=I_{C \text { majority }}+I_{C \text { minority }} \tag{4-2}
\end{equation*}
$$

Meanwhile the recombination current in the close-circuited emitter-base region, which was termed as $I_{E \text { minority }}$, is nothing but the base current $I_{B}$.

Thus, applying Kirchoff's current rule in the collector terminal:

$$
\begin{equation*}
I_{E}=I_{B}+I_{C} \tag{4-3}
\end{equation*}
$$

## 4-5-1 Current Components in $\mathbf{p - n - p}$ Transistor

Now, as we can see in the Figure 4-7(a), both biasing potentials have been applied to a $p-n-p$ transistor, with the resulting majority and minority carrier flow indicated. The width of the depletion region clearly indicates which junction is forward-biased and which is reverse-biased. A large number of majority carriers will diffuse across the forward-biased $p-n$ junction into the $n$-type material. Since the sandwiched $n$-type material is very thin and has a low conductivity, a very small number of these


Figure 4-7(a) Direction of flow of current in $p-n-p$ transistor with the base-emitter junction for-ward-biased and the collector-base junction reverse-biased
carriers will take this path of high resistance to the base terminal. The magnitude of the base current is typically in the order of microamperes as compared to milliamperes for the emitter and collector currents. The large number of these majority carriers will diffuse across the reverse-biased junction into the $p$-type material connected to the collector terminal, as indicated in the Figure 4-7(a).

The majority carriers can easily cross the reverse-biased junction, because for the reverse-biased diode the injected majority carriers will appear as minority carriers in the $n$-type material. These minority carriers assist in the reverse collector saturation current, and hence cross the reverse-biased junction.

Now, applying Kirchoff's current law to the transistor of the Figure 4-7(a) as if it was a single node, we get:

$$
\begin{equation*}
I_{E}=I_{C}+I_{B} \tag{4-4}
\end{equation*}
$$

and we find that the emitter current is the sum of the collector and base currents. The collector current, however, is comprised of two components: the majority and the minority carriers. The minority carrier components are termed as leakage current, and given the symbol $I_{C O}$. The collector current, therefore, is determined in total as:

$$
\begin{equation*}
I_{C}=I_{C \text { majority }}+I_{C O \text { minority }} \tag{4-5}
\end{equation*}
$$

For a general-purpose transistor, $I_{C}$ is measured in milliamperes, while $I_{C O}$ is measured in microamperes or nanoamperes. The basic operation of a $p-n-p$ transistor with its emitter-base junction $\left(J_{E}\right)$ forward-biased and collector-base junction $\left(J_{C}\right)$ reverse-biased, as shown in Figure 4-7(a), can be visualized as follows: when there is no external bias, the current through the transistor should be zero because of the development of an intrinsic potential barrier across the $p-n$ junction. Now the forward-biasing voltage ( $V_{E E}$ ) decreases the emitter-base potential barrier whereas the reverse-biasing voltage ( $V_{C C}$ ) increases the potential barrier across the collector junction $\left(J_{C}\right)$. The lowering of emitter-junction barrier allows injection of holes from emitter to base and injection of electrons from base to emitter. These two flows produce the emitter current:

$$
\begin{equation*}
I_{E}=I_{E}(p)+I_{E}(n) \tag{4-6}
\end{equation*}
$$

where, $I_{E}(p)$ is due to the holes moving from emitter to base, and $I_{E}(n)$ is due to the electrons going from base to emitter. In commercial transistors doping of emitter region is made much higher than the base. This makes $I_{E}(p) \gg I_{E}(n)$, and the emitter current is almost due to the holes only. With only $2-3 \%$ of the total carriers entering the base region, it is bound to be so. This is desirable, because the current component $I_{E}(n)$ does not contribute to the collector current. The injected holes diffuse through the base region towards the collector region. While diffusing through the base, a few of the injected holes are lost due to recombination with majority electrons. The holes that reach the collector junction cross the potential barrier and are immediately collected by the collector region. This gives one of the two current components- $I_{C}(p)$ of the collector current $I_{C}$. $I_{C}(p)$ is slightly smaller than $I_{E}(p)$.

The base current constitutes of electrons flowing from the battery to the base in order to maintain the charge neutrality of the base region. Despite the collector junction being reversebiased, a small amount of current flows from the collector due to the minority carriers. This current has two components. $I_{C O}(n)$, due to the minority electrons flowing from collector ( $p$-side) to base ( $n$-side), and $I_{C O}(p)$, due to the minority holes flowing from base to collector region across the collector-base junction $\left(J_{C}\right)$.The resultant $I_{C O}(n)+I_{C O}(p)$ is denoted by $I_{C B O}$. This is called the leakage current or reverse collector saturation current. This component is very much temperature sensitive; for every $10^{\circ}$ rise in temperature the reverse saturation current nearly doubles. Hence, the current component relations of a $p-n-p$ transistor are as follows:

$$
\begin{align*}
I_{C} & =I_{C}(p)+I_{C B O}  \tag{4-7}\\
I_{E} & =I_{B}+I_{C} \tag{4-8}
\end{align*}
$$

## 4-5-2 Current Components in $n-p-n$ Transistor

The operation of an $n-p-n$ transistor is the same as that of a $p-n-p$ transistor, but with the roles played by the electrons and holes interchanged. The polarities of the batteries and also the directions of various currents are to be reversed, as shown in Figure 4-7(b). Here the majority electrons from the emitter are injected into the base and the majority holes from the base are injected into the emitter region. These two constitute the emitter current.

$$
\begin{equation*}
I_{E}=I_{E}(n)+I_{E}(p) \tag{4-9}
\end{equation*}
$$

Since the doping of the emitter region is much higher than that of the base, i.e., $I_{E}(n) \gg I_{E}(p)$, we have $I_{E} \approx I_{E}(n)$. Thus, the emitter current is almost entirely due to the electrons moving from emitter to base. Since electrons are negatively charged, the direction of conventional current is opposite to the movement of the electrons. The injected electrons diffuse through the base towards the collector junction. A few of the injected electrons are lost due to recombination with the majority carrier holes in the base region.

The electrons moving from the base to the collector junction are collected by the collector region and result in the current $I_{C}(n)$. The difference, $I_{E}(n)-I_{C}(n)$, constitutes a part of the base current $I_{B}$. Since the collector junction is reverse-biased, there is a reverse saturation current $\left(I_{C B O}\right)$ through the junction. $I_{C B O}$ consists of two parts, $I_{C O}(n)$ and $I_{C O}(p) . I_{C O}(n)$ is due to the minority electrons from the base to the collector and $I_{C O}(p)$ is due to the minority holes from collector to base. The relations for the current components can be written as:

$$
\begin{align*}
& I_{C}=I_{C}(n)+I_{C B O}  \tag{4-10}\\
& I_{E}=I_{C}+I_{B} \tag{4-11}
\end{align*}
$$



Figure 4-7(b) The majority and the minority carrier current flow in a forward-biased $n-p-n$ transistor

## 4-6 CB, CE AND CC CONFIGURATIONS

Depending on the common terminal between the input and the output circuits of a transistor, it may be operated in the common-base mode, or the common-emitter mode, or the common-collector mode keeping any one of the three terminals common to both halves of the circuit.

## 4-6-1 Common-Base (CB) Mode

In this mode, the base terminal is common to both the input and the output circuits. This mode is also referred to as the ground-base configuration. Figure $4-8$ shows a $p-n-p$ transistor connected in the common-base (CB) mode and Figure 4-9 shows an $n-p-n$ transistor connected in the common-base mode.

## 4-6-2 Common-Emitter (CE) Mode

When the emitter terminal is common to both the input and the output circuits, the mode of operation is called the common-emitter (CE) mode or the ground-emitter configuration of the transistor. Figure 4-10 shows this type of configuration.


Figure 4-8 Notation and symbols used for the common-base configuration of a $p-n-p$ transistor


Figure 4-9 Common-base configuration of an $n-p-n$ transistor

## 4-6-3 Common-Collector (CC) Mode

When the collector terminal of the transistor is common to both the input and the output terminals, the mode of operation is known as the common-collector ( CC ) mode or the ground-collector configuration. Figure 4-11 shows the common-collector configuration.


Figure 4-10 Notation and symbols for common-emitter configuration
(a) $n-p-n$ transistor (b) $p-n-p$ transistor


Figure 4-11 Common-collector configuration

## 4-7 EXPRESSION FOR CURRENT GAIN

The collector current, when the emitter junction is forward-biased is given by:

$$
\begin{equation*}
I_{C}=I_{C O}-\alpha I_{E} \tag{4-12}
\end{equation*}
$$

where, $I_{C O}$ is the reverse saturation current, and $I_{E}$ is the emitter current.
Thus, $\alpha$ is given by:

$$
\begin{equation*}
\alpha=-\frac{I_{C}-I_{C O}}{I_{E}} \tag{4-13}
\end{equation*}
$$

$\alpha$, represents the total fraction of the emitter current contributed by the carriers injected into the base and reaching the collector. $\alpha$ is thus, called the dc current gain of the common-base transistor. $I_{E}$ and $I_{C}$ are opposites as far as their signs are concerned, therefore, $\alpha$ is always positive. Generally $\alpha$ lies within the $0.95-0.995$ range. It is not a constant but varies with respect to the emitter current $I_{E}$, the collector to base voltage $V_{C B}$, and temperature.

As we know, the value of the reverse saturation current is in the order of nanoamperes. This can be neglected as compared to the collector current. Thus, the expression for $\alpha$ reduces to $-I_{C} / I_{E}$.

The small-signal short-circuit current transfer ratio or the current gain for a common-base configuration is denoted by $\alpha^{\prime}$. It is defined as the ratio of the change in the collector current to the change in the base current at a constant collector to base voltage. Consequently, it is given by:

$$
\begin{equation*}
\left.\alpha^{\prime}=-\frac{\Delta I_{C}}{\Delta I_{B}} \right\rvert\, V_{C B}=0 \tag{4-14}
\end{equation*}
$$

Here $\Delta I_{C}$ and $\Delta I_{B}$ represent the change of collector and base current.

The maximum current gain of a transistor operated in the common-emitter mode is denoted by the parameter $\beta$ (a detailed discussion on this has been included in Chapter 5). It is defined as the ratio of the collector current to the base current.

$$
\begin{equation*}
\beta=\frac{I_{C}}{I_{B}} \tag{4-15}
\end{equation*}
$$

Its value lies in the range of $10-500$.

## 4-7-1 Relationship Between $\alpha$ and $\beta$

In the general model of a transistor the application of Kirchoff's current law (KCL) yields:

$$
\begin{equation*}
I_{E}=-\left(I_{C}+I_{B}\right) \tag{4-16}
\end{equation*}
$$

Replacing the value of $I_{E}\left(I_{C}=I_{C O}-\alpha I_{E}\right)$, we obtain:

$$
\begin{equation*}
I_{C}=\frac{\alpha}{1-\alpha} I_{B}+\frac{I_{C O}}{1-\alpha} \tag{4-17}
\end{equation*}
$$

Again we know that as the value of $I_{C O}$ is very small, therefore, we can neglect its value in comparison with $I_{B}$.

Upon neglecting its value we obtain:
or,

$$
\begin{align*}
& I_{C}=\frac{\alpha}{1-\alpha} I_{B}  \tag{4-18}\\
& \frac{I_{C}}{I_{B}}=\frac{\alpha}{1-\alpha}=\beta \\
& \beta=\frac{\alpha}{1-\alpha} \tag{4-19}
\end{align*}
$$

The relation between $\alpha$ and $\beta$ is expressed in terms of Equation (4-19).

## FOR ADVANCED READERS

## Ebers-Moll Model of Transistor

Investigators Ebers and Moll introduced a general model for transistors, now known as the EbersMoll model. This generalization enables us to understand the limits of forward-active operation; it operates the transistor in the reverse-active mode and shows how to operate the transistor as a switch. The Ebers-Moll model for a $p-n-p$ transistor is shown in the Figure 4-12.

The model involves a pair of ideal diodes connected back-to-back with two independent current sources.

Now, by applying KCL at the collector we get:

$$
\begin{equation*}
i_{C}=\alpha_{F} i_{D E}-i_{D C} \tag{4-20}
\end{equation*}
$$

where, $i_{c}$ is the ordinary diode current in the collector-base junction and represents the special transistor action. Now, upon substituting the values of $i_{D E}$ and $i_{D C}$ in the Equation (4-20) we obtain:

$$
\begin{equation*}
i_{C}=\alpha_{F} I_{E S}\left(e^{V_{B E} / V_{T}}-1\right)-I_{C S}\left(e^{V_{B C} / V_{T}}-1\right) \tag{4-21}
\end{equation*}
$$

where, $I_{E S}$ and $I_{C S}$ are the reverse saturation currents of the respective junctions.


Figure 4-12 Ebers-Moll model of a $p-n-p$ transistor
The Ebers-Moll model also describes the operation of the transistor in the reverse mode, i.e., forward-biasing the collector-base junction and reverse-biasing the emitter-base junction. In the reverse-active mode of operation, the electrons injected from the collector diffuse across the base and are collected at the emitter. Simply put, the collector now acts as the emitter and the emitter as the collector. $\alpha_{R}$ is the reverse current gain of the transistor.

Now, applying KCL at the emitter, we obtain:

$$
\begin{equation*}
i_{E}=l_{E S}\left(e^{V_{B E} / V_{T}}-1\right)-\alpha_{R} l_{C S}\left(e^{V_{B C} / V_{T}}-1\right) \tag{4-22}
\end{equation*}
$$

Solid-state electronics also describes a reciprocity law:

$$
\begin{equation*}
\alpha_{F} I_{E S}=\alpha_{R} I_{C S}=I_{S} \tag{4-23}
\end{equation*}
$$

This relates the two reverse saturation currents and defines the quantity $I_{s}$. Using reciprocity and on simplifying the equations for reverse saturation currents we get the final form of Ebers-Moll equations:

$$
\begin{align*}
& i_{C}=I_{S}\left(e^{V_{B E} / V_{T}}-1\right)-\frac{l_{S}}{\alpha_{R}}\left(e^{V_{B C} / V_{T}}-1\right)  \tag{4-24}\\
& i_{E}=\frac{I_{S}}{\alpha_{F}}\left(e^{V_{B E} / V_{T}}-1\right)-I_{S}\left(e^{V_{B C} / V_{T}}-1\right) \tag{4-25}
\end{align*}
$$

## 4-8 TRANSISTOR CHARACTERISTICS

The graphical forms of the relations between the various current and voltage variables (components) of a transistor are called transistor static characteristics. By considering any two of the variables as independent variables it is possible to draw different families of characteristic curves. However, two sets of characteristic curves known as the input and the output characteristics for common-base and common-emitter modes are of practical use and importance.

## 4-8-1 Input Characteristics

The plot of the input current against the input voltage of the transistor in a particular configuration with the output voltage as a parameter for a particular mode of operation gives the input characteristics for that mode.


Figure 4-13 Input characteristics in the CE mode


Figure 4-14 Input characteristics in the CB mode

## Common-emitter mode

The CE input characteristics constitute the plot of the input current $I_{B}$ against the input voltage $V_{B E}$, with the output voltage $V_{C E}$ as the parameter since the emitter is common to both the input and output sections of the device. The characteristics, as shown in Figure 4-13, are similar to that of the forwardbiased $p-n$ diode, as is expected from the basic device study. For a constant $V_{B E}$, the effective base width decreases with an increasing $\left|V_{C E}\right|$.

## Common-base mode

In this mode the base is common to both the input and output sections of the transistor. The input characteristic for the CB mode, as shown in Figure 4-14, constitutes the plot of the input current $I_{E}$ against the input voltage $V_{E B}$ with the output voltage $V_{C B}$ as the parameter.

Since, the emitter-base junction is forward-biased in normal operation, the input characteristics are similar to that of a forward-biased $p-n$ diode. For a fixed $V_{E B}, I_{E}$ increases with an increase in $\left|V_{C B}\right|$. When $\left|V_{C B}\right|$ increases, the width of the depletion region at the collector-base junction increases, and as a result the effective base width decreases. The change of the effective base width by the collector voltage is known as Early effect. $I_{E}$ increases with an increasing reverse collector voltage.

## 4-8-2 Output Characteristics

Similarly a plot for the output current against the output voltage with the input current as a parameter gives the output characteristics.

The output characteristics can be divided into four distinct regions:
(i) The active region
(ii) The saturation region
(iii) The inverse active region
(iv) The cut-off region

Table 4-1 provides the definitions for the four transistor states. These four BJT states or operating modes correspond to the four possible ways in which we can bias the transistor junctions. Figure 4-15 shows these four transistor states and Figure 4-16 shows the various regions of operation as defined by junction biasing.

Table 4-1 Definitions of transistor states

| Transistor State | Base-Emitter Junction | Base-Collector Junction |
| :--- | :--- | :---: |
| Forward active | Forward $\left(V_{B E} \geq V_{\gamma}\right)$ | Reverse $\left(V_{B C} \leq V_{\gamma}\right)$ |
| Reverse active | Reverse $\left(V_{B E} \leq V_{\gamma}\right)$ | Forward $\left(V_{B C} \geq V_{\gamma}\right)$ |
| Cut-off | Reverse $\left(V_{B E} \leq V_{\gamma}\right)$ | Reverse $\left(V_{B C} \leq V_{\gamma}\right)$ |
| Saturation | Forward $\left(V_{B E} \geq V_{\gamma}\right)$ | Forward $\left(V_{B C} \geq V_{\gamma}\right)$ |

The active region is the region normally employed for linear (undistorted) amplifiers. In the active region particularly, the collector-base junction is reverse-biased, while the base-emitter junction is forward-biased. In the active region, as the emitter current increases above zero and the collector current increases to a magnitude essentially equal to that of the emitter current. Therefore:

$$
I_{E} \approx I_{C}
$$

In the reverse-active region the base-emitter junction is reverse-biased and the base-collector region is forward-biased. In other words, in reverse-active mode, the roles of the emitter and the collector are reversed compared to forward-active mode. However, this mode of operation is hardly used. Figure 4-17 shows the model for the BJT in reverse-active mode with a 0.7 V voltage source con-


Figure 4-15 Transistor states defined by junction biasing


Figure 4-16 Regions of operation for the four transistor states in terms of the output characteristic curves

(a)

(b)

Figure 4-17 Model for BJT in reverse-active mode of operation
nected between the base and the collector, and the dependent source directed from the emitter to the collector.

The emitter current is $\beta_{R} i_{B}$.

Here,

$$
\begin{equation*}
\beta_{R}=\frac{\alpha_{R}}{1-\alpha_{R}} \tag{4-26}
\end{equation*}
$$



Figure 4-18 Large signal cut-off model: (a) simple model (b) model for high temperatures


Figure 4-19 Circuit model for a saturated transistor
This defines the reverse $\beta$ of the transistor. Now, the cut-off region is defined as that region where the collector current is 0 ampere (A). Moreover in the cut-off region the collector-base and base-emitter junctions of a transistor are both reverse-biased. Figure 4-18 shows the cut-off model for the transistor.

This circuit is consistent with the operation in the cut-off region, $I_{C}=I_{B}=0$. At high temperatures, a temperature sensitive dc current, $I_{C B O}$ flows from the collector to the base. Open-circuiting the emitter lead and calculating the collector-to-base current that results from reverse-biasing the collector-base junction measures this $I_{C B O}$ as quite small and is of the order of picoamperes.

The saturation region is defined as the region of the characteristics that lies to the left of $V_{C B}=0$ V. The horizontal scale in this region was expanded to clearly show the dramatic change in the characteristics in this region. The collector current increases exponentially as the voltage $V_{C B}$ increases toward 0 V . In the saturation region the collector-base and base-emitter junctions are forward-biased. A necessary condition for a transistor to be saturated is:

$$
\begin{equation*}
\beta i_{B} \geq i_{C} \tag{4-27}
\end{equation*}
$$

Figure 4-19 shows the circuit model for a saturated transistor.

Since the curves merge into a constant $V_{C E}$ line in the saturation region, a battery of $V_{C E \text { sat }} H$ $\approx 0.2 \mathrm{~V}$ is connected between the collector and the emitter in the saturation model. Since the base-emitter junction is forward-biased, the model also employs a dc input source of $V_{B E}=0.7$ V between the base and the emitter.

## 4-9 OPERATING POINT AND THE CONCEPT OF LOAD LINE

In the case of transistor amplifiers, the operating point refers to the particular condition of the circuit where, with some definite values of voltage and current, we can define the region or the point of operation of the circuit. Lexically, quiescent means stationary, i.e., the voltage or the current should be such that it sets the stage for proper operation of the circuit when a signal is applied. By proper operation we mean that the circuit performs the desired operation. Since most of the time transistors are used for amplification, the region should be so selected that at the output we obtain a faithful and an amplified representation of the input signal. One important attribute of this case is the region of operation of the circuit. This can be readily understood from Figure 4-20.

Figure 4-20 depicts the general output characteristics of a BJT with three operating points as indicated. These threepoints indicate that the biasing circuits canberealized for all the indicated operating points in the active region. The maximum ratings for the transistor being operated are indicated by the horizontal line for maximum collector current, and the horizontal line for maximum collector-to-emitter voltage. Keeping the operation confined within this active region, one can select many operating points, but their selection depends on the intended operation.

If no bias is given, the device would be initially in the OFF state. But, if under such a circumstance a signal is applied at the input, the device would not be able to trace the entire signal. The judicious selection for the operating point should be such that the device can vary in current and voltage from the operating point, and allowing the device to react to both the positive and the negative excursions of the input signal. Also, it should be kept in mind that the selection of the input signal should be such that it does not drive the device in the cut-off and the saturation regions. In general, the operating point should be such that its operation is in that region where the gain is fairly constant.

Having selected the operating point and the input signal, ample measures should be taken for nullifying the effect of temperature while shifting the operating region. Higher temperatures cause a rapid change in the operating conditions of the device. As a result, a factor called the stability factor is introduced (we will study this in much detail in the later chapters).

The load line is a graphical function used to find the device cur-


Figure 4-20 Region of operation of a BJT


Figure 4-21 A common-emitter amplifier
rents and voltages when the device is described by its characteristic curves. Even when the characteristic curves of the device are not available, the load line solves the purpose as it gives the locus of all such points on the curve where the device can be operated and a corresponding output can be obtained. Let us first consider the circuit as shown in Figure 4-21.

Here, $R_{C}$ is the resistor at the collector and $R_{B}$ is the resistance at the base terminal. The respective currents are shown by $i_{C}$ and $i_{B}$ with two voltage sources for proper biasing.
From Figure 4-21, we find that for this common-emitter circuit, the equation for the output voltage, i.e., the collector-to-emitter voltage, $\left(V_{C E}\right)$ can be obtained by applying KVL.

$$
\begin{equation*}
v_{C E}=V_{C C}-i_{C} R_{L} \tag{4-28}
\end{equation*}
$$

And this can be written as:

$$
\begin{equation*}
i_{C}=\frac{V_{C C}}{R_{L}}-\frac{1}{R_{L}} v_{C E} \tag{4-29}
\end{equation*}
$$

From Equation (4-29) we find that it represents the output of the circuit. If this equation is plotted on the output characteristic, we obtain a straight line. The intercept on the $y$-axis is $V_{C C} / R_{L}$ and that on the $x$-axis is $V_{C C}$ as shown in Figure 4-20. For any such given system, a relation between the output voltage and the output current can always be found and can be superimposed on the output characteristics to judge its conditions for operation.

On the $i_{B}$ versus $v_{B E}$ coordinate system, we obtain a straight line for Equation (4-29). The straight line has a slope of $-1 / R_{B}$, which is called the input load line. It is the locus of the points in which the device can be operated. The intersection of this load line with the characteristic curve gives the quiescent operating point $Q$, as shown in Figure 4-20. We can change the operating point by suitably changing various parameters such as $V_{B B}$ and $R_{B}$.

An analysis of Equation (4-29) indicates that any variation in the dc biasing voltage and the circuit elements can have a heavy impact on the operation of the device. But, a judicious selection would be required to place it in the active region, i.e., where the device characteristics also change according to the changes in the input signal.

## 4-10 EARLY EFFECT

In the operating region of a transistor or for a normal operation of the transistor, the emitter-base junction is forward-biased. So the emitter current variation with the emitter-to-base voltage will be similar to the forward characteristic of a $p-n$ junction diode. An increase in the magnitude of the collector-to-base voltage $\left(V_{C B}\right)$ causes the emitter current to increase for a fixed $V_{E B}$. When $\left|V_{C B}\right|$ increases, the depletion region in the collector-base junction widens and reduces the base width. This is known as the Early effect. As a result of this effect, the gradient of the injected hole in the base region increases. The injected hole current across the emitter junction is proportional to the gradient of the hole concentration. So, an increase in the emitter current with an increase in $\left|V_{C B}\right|$ is obtained.


Figure 4-22 Graphical representation of early voltage

Again, since the collector is also dependent on the emitter current, the collector current also sees a sharp increase. The graphical representation of Early effect is shown in Figure 4-22.

By including a resistance $r_{o}$ in parallel with the controlled source, we can represent the linear dependence of $I_{C}$ on $V_{C E}$ in a condition where there is no current flow since the channel is completely void of electrons. This condition is known as pinch-off. If the early voltage is greater than the pinchoff voltage, then:

$$
r_{o} \approx \frac{V_{A}}{I_{C}}
$$

## Solved Examples

Example 4-1 An $n-p-n$ transistor having current gain $\alpha=0.90$ is connected in the CB mode and gives a reverse saturation current $I_{C O}=15 \mu \mathrm{~A}$. Calculate the base and the collector currents for an emitter current of 4 mA .

## Solution:

From Equation (4-12), we have:

$$
I_{C}=I_{C O}-\alpha I_{E}
$$

$I_{E}$ is negative for an $n-p-n$ transistor, therefore:

$$
I_{C}=I_{C O}+\alpha I_{E}
$$

By substituting the required values, we get:

$$
\begin{aligned}
I_{C}= & 0.90 \times 4 \times 10^{-3}+15 \times 10^{-6} \\
& =3.615 \mathrm{~mA}
\end{aligned}
$$

From Equation (4-11), we have:
or,

$$
\begin{aligned}
& -I_{E}=-\left(I_{C}+I_{B}\right) \\
I_{B}= & I_{E}-I_{C}=(4-3.615) \mathrm{mA}=385 \mu \mathrm{~A}
\end{aligned}
$$

Example 4-2 What is the value of $\alpha$ for a BJT that has a $\beta$ of 90 ? Find the base and the emitter current if the collector current is 4 mA .

## Solution:

From Equation (4-19), the common-emitter current gain $\beta$ is given by:

$$
\beta=\frac{\alpha}{1-\alpha}
$$

We find $\alpha=0.989$ by putting $\beta=90$ :

$$
\begin{aligned}
& I_{B}=I_{C} / \beta=44.44 \mu \mathrm{~A} \\
& I_{E}=I_{C}+I_{B}=4.04 \mathrm{~mA}
\end{aligned}
$$

Example 4-3 When used in the common-base configuration mode, a transistor with $\alpha=0.90$ gives a reverse saturation current $I_{C O}=15 \mu \mathrm{~A}$. Calculate the collector current when the transistor is connected in the common-emitter mode with a base current of 0.5 mA .

## Solution:

From Equation (4-19), the common-emitter current gain $\beta$ is given by:

$$
\beta=\frac{\alpha}{1-\alpha}=\frac{0.90}{1-0.90}=9
$$

From Equation (4-17), it follows that:

$$
I_{C}=\beta I_{B}+(\beta+1) I_{C O}
$$

By substituting the adequate values, we have:

$$
\begin{aligned}
I_{C} & =[9 \times 0.5+(9+1) \times 0.015] \mathrm{mA} \\
& =4.65 \mathrm{~mA}
\end{aligned}
$$

Example 4-4 For a particular transistor having a very thin base, a base current of $20 \mu \mathrm{~A}$ and a corresponding collector current of 5 mA are measured. What is $\beta$ for this device?

## Solution:

We know that: $\quad \beta=\frac{I_{C}}{I_{B}}$
Therefore: $\quad \beta=\frac{5 \times 10^{-3}}{20 \times 10^{-6}}$

$$
=250
$$

Example 4-5 For a BJT having a base current of $50 \mu \mathrm{~A}$ and a collector current of 5 mA , what is the emitter current? What is $\beta$ for this transistor? Using your computed value of $I_{E}$. With the given value of $I_{C}$, find the value of $I_{E}$. With the given value of $I_{C}$, find the value of the common-base current gain $\alpha$. Verify that $\alpha=\beta /(\beta+1)$ and that $\beta=\alpha /(1-\alpha)$.

## Solution:

From Equation (4-4), we have:

$$
I_{E}=I_{C}+I_{B}=5+.05=5.05 \mathrm{~mA}
$$

$$
\begin{aligned}
\beta & =\frac{I_{C}}{I_{B}}=\left(5 \times 10^{-3}\right) /\left(50 \times 10^{-6}\right)=100 \\
\alpha & =\frac{I_{C}}{I_{E}} \\
& =(5 / 5.05)=0.990
\end{aligned}
$$

Verification:

$$
\begin{aligned}
\alpha & =\frac{\beta}{\beta+1} \\
& =\frac{100}{100+1} \\
\alpha & =\frac{100}{101}=0.990099 \\
\beta & =\frac{\alpha}{1-\alpha} \\
& =\frac{\frac{100}{101}}{1-\frac{100}{101}} \\
\beta & =\frac{0.990099}{1-0.990099}=100
\end{aligned}
$$

Example 4-6 From the following figure we note that the transistor is not a symmetrical device; therefore, interchanging the collector and the emitter terminals will result in a device with different values of $\alpha$ and $\beta$, known as the inverse or reverse values and denoted as $\alpha_{R}$ and $\beta_{R}$ respectively. An $n-p-n$ transistor is accidentally connected with the collector and emitter leads interchanged. The resulting emitter and base currents are 10 mA and 5 mA , respectively. What are the values of $\alpha_{R}$ and $\beta_{R}$ ?

## Solution:

$$
I_{E}=10 \mathrm{~mA}, I_{B}=5 \mathrm{~mA}
$$

So,

$$
\begin{aligned}
& I_{C}=I_{E}-I_{B}=5 \mathrm{~mA} \\
& \beta_{R}=\frac{I_{C}}{I_{B}}=1 \\
& \alpha_{R}=\frac{I_{C}}{I_{E}}=2
\end{aligned}
$$

Example 4-7 Find the labeled currents and voltages for the circuits, as shown in the following diagrams. Let $\beta=100$ and $\left|V_{B E}\right|$ $=0.7 \mathrm{~V}$.

Solution:
(a) $V_{E}=-0.700 \mathrm{~V}$

$$
I_{E}=(10-0.7) / 10 \mathrm{~K}=0.93 \mathrm{~mA}
$$


(a)

(b)

$$
\begin{aligned}
I_{B} & =\frac{I_{E}}{\beta}+1=\frac{0.93}{101}=9.2 \mu \mathrm{~A} \\
V_{C} & =10-10(0.930-0.0092)=0.792 \mathrm{~V}
\end{aligned}
$$

(b) $V_{E}=-0.700 \mathrm{~V}$

$$
\begin{aligned}
& I_{E}=\frac{10-0.7}{5 \mathrm{~K}}=1.86 \mathrm{~mA} \\
& I_{C}=\frac{\beta}{\beta+1}=\frac{100}{101}(1.86)=1.842 \mathrm{~mA} \\
& V_{C}=-15+5(1.842)=-5.79 \mathrm{~V}
\end{aligned}
$$

Example 4-8 With reference to the following diagrams, we may assume that base currents are negligibly small, since the transistors shown in the circuits have very large values of $\beta$. Find the values of the labeled voltages if they are determined by the measurement $\left|V_{B E}\right|=0.7 \mathrm{~V}$.

Solution:

$$
\beta=\infty,\left|V_{B E}\right|=0.7
$$

(a) $V_{B}=0.0 \mathrm{~V}, V_{E}=-0.7 \mathrm{~V}$

(a)

(b)
(b) $V_{E}=+0.7 \mathrm{~V}, V_{C}=-15+5\left(\frac{10-0.7}{5}\right)=-5.7 \mathrm{~V}$

Example 4-9 The emitter voltage of the transistor in the circuit as shown in the following diagram is 1.0 V . Find $V_{B}, I_{B}, I_{E}, I_{C}, \beta$ and $\alpha$ under the assumption that $V_{B E}=0.7 \mathrm{~V}$.

## Solution:

$$
\begin{aligned}
& V_{E}=1.0 \mathrm{~V} \\
& V_{B}=1.0-0.7=0.3 \mathrm{~V} \\
& I_{B}=\frac{0.3}{20 \mathrm{~K}}=0.015 \mathrm{~mA} \\
& I_{E}=\frac{5-1}{5 \mathrm{~K}}=0.80 \mathrm{~mA} \\
& I_{C}=0.80-0.015=0.785 \mathrm{~mA} \\
& V_{C}=-5+5(0.785)=-1.075 \mathrm{~V} \\
& \beta=\frac{0.785}{0.015}=52.3
\end{aligned}
$$



$$
\alpha=\frac{0.785}{0.800}=0.98
$$

Example 4-10 An $n-p-n$ transistor has its base connected to -5 V, its collector is connected to ground via a $1 \mathrm{k} \Omega$ resistor and its emitter is connected to a 2 mA constant current source that pulls current out of the emitter terminal. If the base voltage is raised by 0.4 V , what voltage changes are measured at the emitter and at the collector?


Solution:

$$
\begin{aligned}
\Delta V_{B} & =+0.4 \mathrm{~V} \\
\Delta V_{E} & =+0.4 \mathrm{~V} \\
\Delta V_{C} & =0.0 \mathrm{~V}
\end{aligned}
$$

Example 4-11 With reference to the circuits, as shown in the following diagrams, identify whether they operate in the active mode or saturation mode. What is the emitter voltage in each case? If active, what is the collector voltage? Given $\left|V_{B E}\right|=0.7 \mathrm{~V}, \beta=100$.

(a)

(b)

(c)

(d)

Solution:

$$
\left|V_{B E}\right|=0.7, \beta=100
$$

(a) Assume active: $V_{E}=2-0.7=1.3 \mathrm{~V}$

$$
\begin{aligned}
I_{E} & =1 \mathrm{~mA} ; I_{C}=1 \times \frac{100}{101}=0.99 \mathrm{~mA} \\
V_{E} & =6-3(0.99)=3.03 \mathrm{~V}
\end{aligned}
$$

Thus, the circuit operates in an active mode.
(b) Assume active: $V_{E}=1.0+0.7=1.7 \mathrm{~V}$

$$
\begin{aligned}
I_{E} & =\frac{6-1.7}{10 \mathrm{~K}}=0.43 \mathrm{~mA} \approx I_{C} \\
V_{C} & =0+10(0.43) \gg V_{B}
\end{aligned}
$$

Thus, the circuit operates in a saturated mode.
(c) Assume active: $V_{E}=-5+0.7=-4.3 \mathrm{~V}$

$$
\begin{aligned}
& I_{E}=\frac{9.5+4.3}{200 \mathrm{~K}}=0.4965 \mathrm{~mA} \\
& I_{C}=I_{E} \frac{100}{101}=0.492 \mathrm{~mA} \\
& V_{C}=-50+0.492(20 \mathrm{~K})=-40.2 \mathrm{~V}
\end{aligned}
$$

Therefore, the circuit operates in an active mode.
(d) Assume active: $V_{E}=-20.7 \mathrm{~V}$

$$
\begin{aligned}
I_{E} & =\frac{30-20.7}{5 \mathrm{~K}}=1.86 \mathrm{~mA} \\
V_{C} & =-1.86\left(\frac{100}{101}\right)(2 \mathrm{~K})-10=-13.68 \mathrm{~V}
\end{aligned}
$$

Therefore, the circuit operates in an active mode.

## 4-11 TRANSISTOR AS AMPLIFIER

A load resistor $R_{L}$ is in series with the collector supply voltage $V_{c c}$, as shown in Figure 4-24.
A small voltage change, $\Delta V_{i}$, between the emitter and the base causes quite a large emitter-current change, given by $\Delta I_{E}$. We define by the symbol $\alpha$ as the fraction of this current change or the effective current which is collected at the collector and passes through $R_{L}$ or $\Delta I_{C}=\alpha \Delta I_{E}$, i.e., that which reaches the collector region. Consequently the change in output voltage across the load resistor can be given by:

$$
\begin{equation*}
\Delta V_{L}=-R_{L} \Delta I_{C}=-\alpha R_{L} \Delta I_{E} \tag{4-30}
\end{equation*}
$$

and this may be many times the change in input voltage $V_{i}$. Under these circumstances, the voltage amplification $A \equiv \Delta V_{L} / \Delta V_{i}$ will be greater than unity and thus, the transistor acts as an amplifier. If the dynamic resistance of the emitter junction is given by $r_{e}$, then corresponding change in the input voltage $\Delta V_{i}=r_{e} \Delta I_{E}$, and thus, the gain is given by:

$$
\begin{equation*}
A \equiv \frac{\alpha^{\prime} R_{L} \Delta I_{E}}{r_{e} \Delta I_{E}}=-\frac{\alpha^{\prime} R_{L}}{r_{e}} \tag{4-31}
\end{equation*}
$$

We know that the resistance of the emitter is the forward resistance of a diode, i.e, $r_{e}=26 / I_{E}$ where, $I_{E}$ is the quiescent emitter current (in milliamperes). For example, if $r_{e}=40 \Omega, \alpha^{\prime}=-1$ and $R_{L}=3,000$ $\Omega$, we have $A=+75$. This calculation has been simplified a lot, but in essence it gives a physical explanation as to why the transistor acts as an amplifier. The transistor provides power gain as well as voltage or current amplification. From this explanation we reach the conclusion that the current in the low-resistance input circuit is transferred to the high-resistance output circuit which occurs mainly because the emitter junction has a very low dynamic resistance. The word "transistor" originated as a contraction of "transfer resistor" and is based upon the physical nature of the device outlined here.


Figure 4-23 Common-emitter and common-base configuration: (a) graphic symbol (b) hybrid equivalent circuit


Figure 4-24 An $n-p-n$ transistor in the common-base bias mode

## 4-11-1 The Parameter $\alpha^{\prime}$

The parameter $\alpha^{\prime}$ is defined as the ratio of the change in the collector current to the change in the emitter current at constant collector-to-base voltage and is called the negative of the small-signal short-circuit current transfer ratio or gain. Qualitatively, it gives us a figure of the amount of current carriers that move from the emitter and are collected at the collector. More specifically:

$$
\begin{equation*}
\alpha^{\prime}=\left.\frac{\Delta I_{C}}{\Delta I_{E}}\right|_{C c s} \tag{4-32}
\end{equation*}
$$

where, $V_{C B}=$ constant.

## 4-12 EXPRESSIONS OF CURRENT GAIN, INPUT RESISTANCE, VOLTAGE GAIN AND OUTPUT RESISTANCE

Figure 4-25 shows the $h$-parameter equivalent circuit of a transistor amplifier having a voltage source $V_{g}$, withits inputresistance $R_{g}$ connected to the inputterminals andaloadresistance $R_{L}$ connected to the output terminals.

Now we will derive expressions for the current gain $\left(A_{I}\right)$, the input resistance $\left(R_{I}\right)$, the voltage gain $\left(A_{V}\right)$ and the output resistance $\left(R_{o}\right)$.

## 4-12-1 Current Gain $\left(A_{1}\right)$

Current gain is defined as the ratio of the output current to input current. If the load current is $I_{L}$ and it is assumed to flow from the top to the bottom through $R_{L}$, as shown in Figure 4-25, then:

$$
\begin{equation*}
A_{I}=\frac{I_{L}}{I_{1}}=-\frac{I_{2}}{I_{1}} \tag{4-33}
\end{equation*}
$$

Again, applying Kirchoff's current rule for the output circuit we get:

$$
\begin{equation*}
I_{2}=h_{o} V_{2}+h_{f} I_{1} \tag{4-34}
\end{equation*}
$$

where,

$$
\begin{equation*}
V_{2}=I_{L} R_{L}=-I_{2} R_{L} \tag{4-35}
\end{equation*}
$$

From Equations (4-34) and (4-35) we get:

$$
I_{2}=-h_{o} I_{2} R_{L}+h_{f} I_{1}
$$

or,

$$
I_{2}\left(1+h_{o} R_{L}\right)=h_{f} I_{1}
$$



Figure 4-25 $h$-Parameter equivalent circuit of a transistor
or,

$$
\begin{align*}
& \frac{I_{2}}{I_{1}}=\frac{h_{f}}{\left(1+h_{o} R_{L}\right)} \\
& \quad A_{I}=-\frac{I_{2}}{I_{1}}=-\frac{h_{f}}{\left(1+h_{o} R_{L}\right)}  \tag{4-36}\\
& A_{I}=\frac{-h_{f}}{\left(1+h_{o} R_{L}\right)}
\end{align*}
$$

or,

## 4-12-2 Input Resistance ( $R_{\boldsymbol{J}}$ )

Input resistance is defined as the ratio of the input voltage across the input terminals of the amplifier to the current $I_{1}$. Therefore:

$$
\begin{equation*}
R_{I}=\frac{V_{1}}{I_{1}} \tag{4-37a}
\end{equation*}
$$

From the input circuit we get by applying KVL:

$$
\begin{gather*}
V_{1}=h_{i} I_{1}+h_{r} V_{2}  \tag{4-37b}\\
\text { or, }  \tag{4-38}\\
\text { Hence, } \frac{V_{1}}{I_{1}}=h_{i}+h_{r} \frac{V_{2}}{I_{1}}=h_{i}-h_{r} \frac{I_{2}}{I_{1}} R_{L} \quad\left(\because V_{2}=-I_{2} R_{L}\right)  \tag{4-39}\\
R_{I}=h_{i}+A_{I} h_{r} R_{L} \quad\left(\because A_{I}=-\frac{I_{2}}{I_{1}}\right)
\end{gather*}
$$

Substituting the value of $A_{I}$ from Equation (4-36) we get:

$$
\begin{equation*}
R_{I}=h_{i}-\frac{h_{f} h_{r} R_{L}}{1+h_{o} R_{L}} \tag{4-40}
\end{equation*}
$$

## 4-12-3 Voltage Gain $\left(A_{v}\right)$

Voltage gain or voltage amplification is defined as the ratio of the output voltage $V_{2}$ to the input voltage $V_{1}$.

Since

$$
\begin{equation*}
A_{V}=\frac{V_{2}}{V_{1}} \tag{4-41}
\end{equation*}
$$

$$
\begin{equation*}
V_{2}=-I_{2} R_{L}=A_{I} I_{1} R_{l} \tag{4-42}
\end{equation*}
$$

we get,

$$
\begin{equation*}
A_{V}=A_{I} R_{L} \frac{I_{1}}{V_{1}}=\frac{A_{I} R_{L}}{R_{I}} \tag{4-43}
\end{equation*}
$$

$$
\begin{equation*}
A_{V}=-\frac{h_{f} R_{L}}{h_{i}+\Delta h R_{L}} \tag{4-44}
\end{equation*}
$$

where,

$$
\Delta h=h_{i} h_{o}-h_{f} h_{r}
$$

## 4-12-4 Output Resistance ( $R_{0}$ )

The output resistance is defined as the ratio of $V_{2}$ and $I_{2}$, where $I_{2}$ is the current delivered by the generator $V_{2}$. In order to find this, we set the source voltage $V_{g}$ to zero and replace the load resistance $R_{L}$ by a voltage generator $V_{2}$. Therefore:

$$
\begin{equation*}
R_{o}=\frac{V_{2}}{I_{2}} \tag{4-45}
\end{equation*}
$$

Considering the output circuit of Figure 4-25 we obtain:

$$
\begin{equation*}
I_{2}=h_{o} V_{2}+h_{f} I_{1} \tag{4-46}
\end{equation*}
$$

From the input mesh, we can write: $\left(R_{g}+h_{i}\right) I_{1}+h_{r} V_{2}=0$
or,

$$
\begin{equation*}
I_{1}=-\frac{h_{r} V_{2}}{R_{g}+h_{i}} \tag{4-47}
\end{equation*}
$$

Hence,

$$
\begin{equation*}
I_{2}=h_{o} V_{2}-\frac{h_{f} h_{r} V_{2}}{R_{g}+h_{i}} \tag{4-49}
\end{equation*}
$$

or,

$$
I_{2}=V_{2}\left(h_{o}-\frac{h_{f} h_{r}}{R_{g}+h_{i}}\right)
$$

## 4-13 FREQUENCY RESPONSE FOR CE AMPLIFIER WITH AND WITHOUT SOURCE IMPEDANCE

At different frequencies of the input signal, the performance of the device is different. The analysis till now has been limited to the mid-frequency spectrum. Frequency response of an amplifier refers to the variation of the magnitude and phase of the amplifier with frequency. A plot of gain vs. frequency for a CE amplifier is shown in Figure 4-26(a) and phase angle vs. frequency for a CE amplifier is shown in Figure 4-26(b).

## 4-13-1 Conclusions

I. The frequency response can be divided into three ranges.
(i) High-frequency range: The magnitude of voltage gain decreases slowly with the increase in frequency and the phase angle decreases below 180 degrees.
(ii) Mid-frequency range: Both gain and phase remain nearly constant.

(b)

Figure 4-26 (a) Gain vs. frequency for a CE amplifier (b) Phase angle vs. frequency for a CE amplifier
(iii) Low-frequency range: The magnitude of voltage gain increases slowly with the increase in frequency and the phase angle increases up to 180 degrees but below 270 degrees.
II. Bandwidth of the amplifier is the difference between upper and lower cut-off frequency range:

$$
\begin{equation*}
B W=f_{u}-f_{l} \tag{4-51}
\end{equation*}
$$

III. Upper cut-off frequency: For which voltage gain is 0.707 time of its maximum gain at upper frequency range, as shown in Figure 4-26(a). It is also known as half-power frequency.
IV. Lower cut-off frequency: For which voltage gain is 0.707 time of its maximum gain at lower frequency range, as shown in Figure 4-26(a). It is also known as half-power frequency.

## 4-14 EMITTER FOLLOWER

The emitter follower transistor is a design which is basically a CC amplifier. As seen from Figure 4-27, the output signal is taken from the emitter with respect to ground and the collector is


Figure 4-27 An emitter follower configuration with biasing connected directly to $V_{c c}$. Since $V_{c c}$ is at signal ground in the ac equivalent circuit, we have the name common-collector. This is further illustrated in Figure 4-27.

From Figure 4-27, we find that the direction of the emitter current for the transistor is opposite to the reference (stipulated) direction. Again, we see that with an increase in the base voltage, the emitter-base junction becomes more forward-biased, giving rise to an increase in the emitter current. The output emitter voltage, follows the input base voltage, with zero phase shift; thus, the significance of the name emitter follower. The expressions for current gain, input resistance, voltage gain and output resistance of the CC amplifier are as follows. The detailed derivation is left for the reader to perform as they can be obtained by a simple $h$-parameter model of the respective circuit.
(i) Current gain:

$$
\begin{equation*}
A_{i}=-\frac{I_{e}}{I_{b}}=1+\frac{h_{f e}}{1+h_{o e} R_{L}} \tag{4-52}
\end{equation*}
$$

(ii) Input resistance:

$$
\begin{equation*}
R_{i}=\frac{V_{i}}{I_{b}}=h_{i e}+A_{i} R_{L} \tag{4-53}
\end{equation*}
$$

(iii) Voltage gain:

$$
\begin{equation*}
A_{V}=\frac{V_{L}}{V_{i}}=\frac{A_{i} R_{L}}{R_{i}} \tag{4-54}
\end{equation*}
$$

(iv) Output resistance:

$$
\begin{equation*}
R_{o}=\frac{R_{G}+h_{i e}}{1+R_{G} h_{o e}+h_{i e} h_{o e}+h_{f e}} \tag{4-55}
\end{equation*}
$$

Also, in Figure 4-27, we find that the there are two capacitors which solve the purposes of coupling. The emitter follower is used for impedance matching.

## Solved Examples

Example 4-12 Consider an emitter follower. Neglect $h_{r e}$ and show that as $\operatorname{Re} \rightarrow \infty$
(a) $R_{i}=h_{i e}+\frac{1+h_{f e}}{h_{o e}}=\frac{1}{h_{o b}}$

> Explain the result physically.
(b) $1-A_{V} \approx \frac{h_{i e} h_{o e}}{1+h_{f e}}$

Evaluate $A_{V}$ using $h$-parameter values given in the following table.

| $h$-parameters | Values |
| :--- | :--- |
| $h_{i e}$ | $1.1 \mathrm{k} \Omega$ |
| $h_{r e}$ | $2.5 \times 10^{-4}$ |
| $h_{f e}$ | 50 |
| $1 / h_{o e}$ | $40 \mathrm{k} \Omega$ |

## Solution:

(a) From the equation for current amplification for a emitter follower connection,

$$
A_{I}=\frac{1+h_{f e}}{1+h_{o e} R_{e}}=\frac{1+h_{f e}}{h_{o e} R_{e}}\left(\text { for very large } R_{e}\right)
$$

From equation of input resistance:

But,

$$
R_{i}=h_{i e}+A_{I} R_{e}=h_{i e}+\frac{1+h_{f e}}{h_{o e}}
$$

$$
h_{o b}=\frac{h_{o e}}{1+h_{f e}}
$$

Hence,

$$
R_{i}=\frac{1}{h_{o b}} \approx 2 \mathrm{M}>h_{i e}=1 \mathrm{~K}
$$

(b) $A_{V}=1-\frac{h_{i e}}{R_{i}}=1-\frac{h_{i e} h_{o e}}{1+h_{i e}} \quad$ where, use of its voltage gain and result in part (a) has been made.

$$
A_{V}=1-\frac{\frac{1.1}{40}}{1+50}=1-\frac{1.1}{2040}=0.99946
$$

Example 4-13 For the emitter follower with $R_{s}=0.5 \mathrm{~K}$ and $R_{L}=5 \mathrm{~K}$, calculate $A_{I,} R_{i,} A_{V}, A_{V S}$, and $R_{o}$. Assume $h_{f e}=50, h_{i e}=1 \mathrm{~K}, h_{o e}=25 \mu \mathrm{~A} / \mathrm{V}$.

## Solution:

From the equation for current gain:

$$
A_{I}=\frac{1+h_{f e}}{1+h_{o e} R_{L}}=\frac{51}{1+0.185}=45.3
$$

From the equation for input resistance:

$$
R_{i}=h_{i e}+A_{I} R_{L}=1+226=227 \mathrm{~K}
$$

From the equation for voltage gain:

$$
\begin{gathered}
A_{V}=1-\frac{h_{i e}}{R_{i}}=1-\frac{1}{227}=0.9956 \\
A_{V S}=A_{V} \frac{R_{i}}{R_{i}+R_{S}}=A_{V} \frac{227}{227+0.5} \approx 0.9956\left(1-\frac{0.5}{227.5}\right)=0.9934
\end{gathered}
$$

Example 4-14 (a) Design an emitter follower having $R_{i}=500 \mathrm{~K}$, and $R_{o}=20 \Omega$. Assume $h_{f e}=50$, $h_{i e}=1 \mathrm{~K}, h_{o e}=25 \mu \mathrm{~A} / \mathrm{V}$.
(b) Find $A_{I}$ and $A_{V}$ for the emitter follower of part (a).
(c) Find $R_{i}$ and the necessary $R_{L}$ so that $A_{V}=0.999$.

## Solution:

(a) From input resistance, $R_{i}=h_{i e}+A_{I} R_{L}$
or, $\quad A_{I} R_{L}=499 \mathrm{~K}$
From the equation of current gain $\quad A_{I}=\frac{1+h_{f e}}{1+h_{o e} R_{L}}$
or,

$$
\begin{equation*}
A_{I}+A_{I} h_{o e} R_{L}=1+h_{f e} \tag{1}
\end{equation*}
$$



Substituting the given values in Equation (1) we obtain:
or,

$$
A_{I}+499 \times 10^{3} \times 25 \times 10^{-6}=1+50
$$

Hence

$$
R_{L}=\frac{499 \mathrm{~K}}{38.5}=13 \mathrm{~K}
$$

Using of the equation for output conductance we have:

$$
Y_{0}=0.05=25 \times 10^{-6}+\frac{51}{1000+R_{S}}
$$

or,

$$
R_{S}=20 \Omega
$$

(b) We found $A_{I}$ in part (a), $A_{I}=38.5$. From the equation for voltage gain we obtain:

$$
A_{V}=1-\frac{1 \times 10^{3}}{0.5 \times 10^{6}}=0.998
$$

(c) From the equation for voltage gain with $A_{V}=0.999$ :

$$
\frac{h_{i e}}{R_{i}}=1-A_{V}=0.001, R_{i}=\frac{1000}{0.001}=10^{6}=1 \mathrm{M} \Omega
$$

From the equation for input resistance $R_{i}=h_{i e}+A_{I} R_{L}=10^{6}$

$$
\begin{aligned}
& \text { For } h_{i e}=10^{3}, A_{I} R_{L} \approx 10^{6}=\frac{1+h_{f e}}{1+h_{o e} R_{L}} \\
& 10^{6}+25 R_{L}=51 R_{L} ; R_{L}=38.4 \mathrm{~K}
\end{aligned}
$$

Example 4-15 For the transistor circuit of a transistor in hybrid mode show that:
(a) $A_{I S(\max )}=-h_{f}\left(\right.$ if $R_{L}=0$ and $\left.R_{s}=\infty\right)$
(b) $R_{i}=h_{i}\left(\right.$ if $\left.R_{L}=0\right)$
(c) $R_{i}=\frac{h_{i} h_{o}-h_{r} h_{f}}{h_{o}}$, (if $R_{L}=\infty$ )
(d) $\quad\left(A_{V S}\right)_{\max }=\frac{-h_{f}}{h_{i} h_{o}-h_{r} h_{f}}\left(\right.$ if $R_{L}=\infty$ and $\left.R_{s}=0\right)$
(e) $R_{0}=\frac{h_{i}}{h_{i} h_{o}-h_{r} h_{f}}\left(\right.$ if $\left.R_{s}=0\right)$
(f) $Y_{0}=h_{o}$ (if $R_{S}=\infty$ )

## Solution:

(a) For current gain, taking into account the source resistance:

$$
A_{I S}=A_{I} \frac{R_{S}}{R_{i}+R_{S}}=-\frac{h_{f}}{1+h_{o} R_{L}} \times \frac{R_{S}}{R_{S}+h_{i}+h_{r} A_{I} R_{L}}=-\frac{h_{f} R_{S}}{R_{S}+h_{i}}
$$

Since $\quad R_{L}=0, \lim _{x \rightarrow \infty} A_{I S}=-h_{f}=A_{I S(\max )}$
(b) For input impedance, $R_{i}=h_{i}+h_{r} A_{I} R_{L}=h_{i}$ for $\left(R_{L}=0\right)$
(c) $R_{i}=h_{i}-\frac{h_{f} h_{r}}{\frac{1}{R_{L}}+h_{o}}=h_{i}-\frac{h_{f} h_{r}}{h_{o}}=\frac{h_{i} h_{o}-h_{f} h_{r}}{h_{o}}$
(d) $A_{V S}=A_{I} \frac{R_{S}}{R_{i}+R_{S}} \frac{R_{L}}{R_{S}}$

So, $\quad A_{V S}=\frac{-h_{f}}{\frac{1}{R_{L}}+h_{o}} \times \frac{1}{h_{i}-\frac{h_{r} h_{f}}{\frac{1}{R_{L}}+h_{o}}}$ since $R_{S}=0$ but for $R_{L}=\infty$
Hence $A_{V S}=\frac{-h_{f}}{h_{i} h_{o}-h_{r} h_{f}}$
(e) Also $Y_{0}=h_{o}-\frac{h_{f} h_{r}}{h_{i}}+R_{S}=\frac{h_{i} h_{o}-h_{r} h_{f}}{h_{i}}$ since $R_{S}=0$ or $R_{0}=\frac{h_{f}}{h_{i} h_{o}-h_{r} h_{f}}$
(f) Using previous result, if $R_{S}=\infty, Y_{0}=h_{o}$

## POINTS TO REMEMBER

1. A bipolar junction transistor (BJT) is a three-terminal active device and can be considered to be made up of two $p-n$ junctions connected back-to-back.
2. The operation of a BJT depends mainly on the active participation of both the majority and minority carriers. Thus, the significance of the term bipolar.
3. For normal operation, the emitter-base junction is forward-biased and the collector-base junction is reverse-biased.
4. Consequently, the width of the depletion region of the emitter-base junction is less and that of the collector-base junction is high.
5. In the common-base mode, the base terminal is common to both the input and the output terminals.
6. In the common-emitter mode, the emitter terminal is common to both the input and the output terminals.
7. When the collector terminal of the transistor is made common to the input and output terminals, the mode of operation is called commoncollector mode.
8. The factor or the current gain in the common-base mode gives the fraction of the total emitter current injected into the base
and reaching the collector. Its value ranges between 0.9-0.995.
9. The factor gives the current gain when the transistor is in the common-emitter mode. Typically, its value ranges from 20-200.
10. The Ebers-Moll model is a generalized model of a transistor. The model involves two diodes connected back-to-back with two independent current sources.
11. The Ebers-Moll model provides a model for the forward-active and reverse-active modes.
12. In the active mode, the emitter-base junction is forward-biased and the collector-base junction is reverse-biased.
13. In the saturation mode, both the emitter-base and the collector-base junctions are forwardbiased.
14. In cut-off mode, both the emitter-base and the collector-base junctions are reversebiased.
15. Active region is mainly employed for linear operation of the device and when it is so required that the device parameters change with changes in the input.
16. The junction temperature of a transistor rises due to self heating and ambient temperature. Due to junction temperature, the collector
current may rise, which in turn increases the power dissipation. This is called thermal runaway.
17. In an emitter follower circuit, the output at the emitter follows the input signal and thus, the name.

## IMPORTANT FORMULAE

1. Components of the emitter current are:

$$
I_{E}=I_{\text {minority }}+I_{\text {majority }}
$$

2. Total emitter current:

$$
I_{E}=I_{C}+I_{B}
$$

3. Total collector current:

$$
I_{C}=I_{C O}-\alpha I_{E}
$$

4. Forward current gain in the common base configuration is given by:

$$
\alpha=\frac{-I_{C}}{I_{B}}
$$

5. Forward current gain in the common emitter configuration is given by:

$$
\beta=\frac{I_{C}}{I_{B}}
$$

6. The relationship between $\alpha$ and $\beta$ is given by:

$$
\beta=\frac{\alpha}{1-\alpha}
$$

7. The input resistance of the amplifier is given by:

$$
R_{I}=h_{i}-\frac{h_{f} h_{r} R_{L}}{1+h_{o} R_{L}}
$$

8. The output resistance is given by:

$$
R_{o}=\frac{V_{2}}{I_{2}}=\frac{R_{g}+h_{i}}{R_{g} h_{o}+h_{i} h_{o}-h_{f} h_{r}}
$$

9. For emitter follower:
(a) Current gain, $A_{i}=-\frac{I_{e}}{I_{b}}=\frac{1+h_{f e}}{1+h_{o e} R_{L}}$
(b) Input resistance:

$$
R_{i}=\frac{V_{i}}{I_{b}}=h_{i e}+A_{i} R_{L}
$$

(c) Voltage gain:

$$
A_{V}=\frac{V_{L}}{V_{i}}=A_{i} R_{L} / R_{i}
$$

From these expressions of current gain, and also by making approximations that $h_{f e} \gg 1$ and $h_{o e} \approx 0, A_{v}=h_{f e} R_{L} / h_{i e}+h_{f e} R_{L}$
(d) Output resistance:

$$
R_{o}=R_{G}+h_{i e} /\left(1+R_{G} h_{o e}+h_{i e} h_{o e}+h_{f e}\right)
$$

## OBJECTIVE QUESTIONS

1. BJT is a:
(a) Current-controlled device
(b) Voltage-controlled device
(c) Power-controlled device
(d) None of the above
2. A BJT is in the saturation region if:
(a) Base-emitter junction is reverse-biased and base-collector junction is forwardbiased
(b) Both the junctions are reverse-biased
(c) Both the junctions are forwardbiased
(d) Base-emitter junction is forward-biased and base-collector junction is reversebiased
3. Doping concentration of BJT is high in the:
(a) Emitter region
(b) Base region
(c) Collector region
(d) None of the above
4. The Ebers-Moll model is valid for:
(a) Bipolar junction transistors
(b) MOS transistors
(c) Unipolar junction transistors
(d) Junction field-effect transistors
5. If a transistor is operating with both of its junctions forward-biased, but with the collectorbase forward-bias greater than emitter-base forward-bias, then it is operating in the:
(a) Forward-active mode
(b) Reverse-saturation mode
(c) Reverse-active mode
(d) Forward-saturation mode
6. In a bipolar transistor at room temperature, if the emitter current is doubled, the voltage across its base-emitter junction:
(a) Doubles
(b) Halves
(c) Increases by $1 / 3$ Volt
(d) No change occurs
7. The Early effect in a bipolar transistor is caused by:
(a) Base width modulation
(b) Large collector-base reverse-bias
(c) Large emitter-base forward-bias
(d) Increase in junction temperature
8. $\beta$ is the symbol of current gain for:
(a) Common-base mode
(b) Common-emitter mode
(c) Common-collector mode
(d) None of the above
9. $\alpha$ is the symbol of current gain for:
(a) Common-base mode
(b) Common-emitter mode
(c) Common-collector mode
(d) None of the above
10. Magnitude of $\alpha$ is:
(a) $<1$
(b) $>1$
(c) $<0$
(d) None of the above
11. Magnitude of $\beta$ is:
(a) $<1$
(b) $>0$ and $<1$
(c) $\gg 1$ (high value)
(d) None of the above
12. For the BJT, the impurity concentration in the emitter $(E)$, base $(B)$ and collector $(C)$ are such that:
(a) $E>B>C$
(b) $B>C>E$
(c) $C=E=B$
(d) $C>E>B$
13. When a junction transistor is operated under saturated conditions:
(a) Both the CB and EB junction are for-ward-biased
(b) The CB junction is forward-biased but the EB junction is reverse-biased
(c) The CB junction is forward-biased but the EB junction is forward-biased
14. The modulation of effective base width by collector voltage is known as Early effect. Hence reverse collector voltage:
(a) Increases both $\alpha$ and $\beta$
(b) Decreases both $\alpha$ and $\beta$
(c) Increases $\alpha$ but decreases $\beta$
(d) Decreases $\beta$ but increases $\alpha$
15. If $\alpha=0.995, I_{E}=10 \mathrm{~mA}$ and $I_{C O}=0.5 \mathrm{~mA}$, then $I_{C E O}$ will be:
(a) $100 \mu \mathrm{~A}$
(b) $25 \mu \mathrm{~A}$
(c) 10.1 mA
(d) 10.5 mA
16. Match list A (transistor parameter) with list B (typical value):

## List-A

(a) $R_{B}$
(b) $R_{C}$
(c) $\alpha$
(d) $\beta$
17. In a transistor as an amplifier, the reverse saturation current:
(a) Doubles for every $C$ rise in temperature
(b) Doubles for every $10^{\circ} \mathrm{C}$ rise in temperature
(c) Decreases linearly with temperature
(d) Increase linearly with temperature
18. Which configuration of bipolar transistors of similar geometry has the highest current gain, bandwidth product?
(a) $n-p-n$ Ge transistor
(b) $p-n-p$ Si transistor
(c) $p-n-p$ Ge transistor
(d) $n-p-n$ Si transistor
19. Base-to-emitter voltage in forward-biased transistor decreases with the increase of temperature at the rate of:
(a) $2.5 \mathrm{mv} /{ }^{\circ} \mathrm{C}$
(b) $25 \mathrm{mv} /{ }^{\circ} \mathrm{C}$
(c) $0.25 \mathrm{mv} /{ }^{\circ} \mathrm{C}$
(d) $0.6 \mathrm{mv} /{ }^{\circ} \mathrm{C}$
20. In the BJT amplifier, the transistor is biased in the forward active region putting a capacitor across $R_{E}$ will:
(a) Decrease the voltage gain and decrease the input impedance
(b) Increase the voltage gain and decrease the input impedance
(c) Decrease the voltage gain and increase the input impedance
(d) Increase the voltage gain and increase the input impedance
21. In a common emitter BJT amplifier, the maximum usable supply voltage is limited by:
(a) Avalanche breakdown of base-emitter junction
(b) Collector-base breakdown voltage with emitter open (BVCBO)
(c) Collector-emitter breakdown voltage with base open (BVCEO)
(d) Zener breakdown voltage of the emit-ter-base junction
22. The transconductance $g_{m}$ is defined as $g_{m}=\partial i_{o} / \partial V_{B E}$. Its value in terms of $h$-parameters is:
(a) $\frac{h_{i e}}{h_{f e}}$
(b) $\frac{h_{f e}}{25}$
(c) $\frac{h_{t e}}{h_{i e}}$
(d) None of the above
23. Introducing a resistor in the emitter of a common emitter amplifier stabilizes the dc operating point against variations in:
(a) Only the temperature
(b) Only the $\beta$ of the transistor
(c) Both temperature and $\beta$
(d) None of the above
24. In a CE transistor amplifier, if collectoremitter voltage increases the instantaneous operating point:
(a) Moves up the load line
(b) Moves down the load line
(c) Moves at right angle to the load line
(d) Remains stationary
25. The $h$-parameter equivalent circuit of a junction transistor is valid for:
(a) High-frequency, large-signal operation
(b) High-frequency, small-signal operation
(c) Low-frequency, small-signal operation
(d) Low-frequency, large-signal operation
26. In a transistor $h_{f e}=50, h_{i e}=830$ ohms, $h_{o e}=10-4$ mho. When used as in the CB mode, then its output resistance will be:
(a) 2 mohms
(b) 500 K
(c) 2.5 mohms
(d) 780 K
27. The small-signal input impedance of a transistor when the output is shorted for the measuring signal, is: (where the symbols have then usual measuring)
(a) $h_{11}=\left.\frac{V_{1}}{I_{1}}\right|_{V_{2}=0}$
(b) $h_{12}=\left.\frac{V_{1}}{i_{1}}\right|_{V=0}$
(c) $h_{21}=\left.\frac{i_{2}}{i_{1}}\right|_{V_{2}=0}$
(d) $h_{22}=\left.\frac{i_{2}}{i_{1}}\right|_{V_{1}=0}$
28. For obtaining hybrid parameters of a transistor:
(a) Variable $V_{b e}$ and $I_{e}$ are taken as independent variables
(b) The two independent variables are the ones that are most easily measurable for a CE configuration
(c) Variable $i_{b}$ and $v_{c e}$ ie are taken as dependent variables
(d) Variable $v_{b e}$ and $i_{e}$ are taken as dependent variables
29. The condition necessary to calculate $h_{o e}$ of a transistor:
(a) DC base current is to be zero
(b) Base to emitter voltage is to be constant
(c) Collector current is to be constant
(d) Base current is to be constant
30. The approximate value of input impedance of a common-emitter amplifier with emitter resistance $R_{e}$ is given by:
(a) $h_{i e}+A_{1} R_{e}$
(b) $h_{i e}+\left(1+h_{f e}\right) R_{e}$
(c) $h_{\text {ie }}$
(d) $\left(1+h_{f e}\right) R_{e}$

## REVIEW QUESTIONS

1. What is a transistor?
2. The metal lead of the $p$-side of a $p-n$ diode is soldered to the metal lead of the $p$-side of another $p-n$ junction diode. Will the structure form an $n-p-n$ transistor? If not, why?
3. Indicate the reference current directions and voltage polarities of a transistor. Give the signs of the actual current directions for an $n-p-n$ and $p-n-p$ transistor operating normally?
4. Why are junction transistors called bipolar devices?
5. The emitter region of the transistor is more heavily doped compared to the base region. Why?
6. Mention briefly the different techniques used in the manufacture of transistors.
7. Show the doping profile in the emitter, base and collector regions of a transistor. Why is the width of the base thin?
8. Discuss the mechanism of amplification obtained in a transistor. What is the origin of the name "transistor"?
9. Give the physical arrangement of a $p-n-p$ junction transistor and discuss how it provides current amplification.
10. Discuss how a transistor is to be used as a current amplifier.
11. Explain how voltage amplification is obtained in a transistor CB amplifier although the current gain is less than unity.
12. Show the different current components of a $p-n-p$ transistor when the emitter junction is forward-biased and the collector junction is reverse-biased.
13. Give the minority carrier concentration profile in a $p-n-p$ transistor operating normally.
14. Draw the energy variation curve in the conduction band for an open circuited $n-p-n$ transistor. How is the curve modified when the transistor is operating in the active region?
15. What do you mean by the static characteristics of a transistor? Draw the circuit diagram of a transistor operating in the common-base configuration and sketch the output characteristics.
16. Drawthe common-baseinputcharacteristics of the transistor. What is an Early effect and how can it account for the CB input characteristics?
17. With respect to $C B$ output characteristics of a transistor, explain the active, saturation and cut-off regions.
18. Draw the common-emitter circuit of a junction transistor. Sketch its output character-
istics and indicate the active, saturation and cut-off regions.
19. Define base-spreading resistance and saturation resistance in connection with a transistor.
20. Explain the phenomenon of punch-through in a transistor.
21. Explain the current amplification factors for CB and CE configurations of a $p-n-p$ transistor. Obtain a relation between them.
22. How can you find the CE output characteristics of a transistor?
23. Explain the various switching times when a transistor makes a transition from the cut-off state to the saturation state and back.
24. The value of $\alpha$ increases with the increasing reverse-bias voltage of the collector junction. Why?
25. Draw the low-frequency $h$-equivalent circuit of a transistor amplifier operating in the CE mode. Why is this circuit not valid for high frequencies?
26. Draw and label the circuit diagram of a smallsignal single stage low-frequency transistor amplifier in the CE mode. Using $h$-parameters obtain expression for current gain, input impedance, voltage gain and output impedance.
27. Show that the power gain in the above problem is the product of the current gain and the voltage gain.
28. Draw the circuit diagram of an emitter follower. Why is the circuit called so? Obtain the expressions for current gain, voltage gain, input impedance and output impedance.
29. Draw the approximate hybrid model for any transistor configuration at low frequencies. Show that only $h_{i e}$ and $h_{f e}$ are important in the model. Is the approximation justified?

## PRACTICE PROBLEMS

1. An $n-p-n$ transistor has an emitter area of $10 \mu \mathrm{~m} \times 10 \mu \mathrm{~m}$. The doping concentrations are as follows: In the emitter $N_{D}=10^{19} / \mathrm{cm}^{3}$, in the base $N_{A}=10^{17} / \mathrm{cm}^{3}$, and in the collector $N_{D}=10^{15} / \mathrm{cm}^{3}$. The transistor is operating at $\mathrm{T}=300 \mathrm{~K}$ where, $n_{i}=1.5 \times 10^{10} / \mathrm{cm}^{3}$. For electrons diffusing in the emitter, $L_{n}=19 \mu \mathrm{~m}$ and $D_{n}=21.3 \mathrm{~cm}^{2} / \mathrm{s}$. For holes diffusing in the emitter, $L_{p}=0.6 \mu \mathrm{~m}$ and $D_{p}=1.7 \mathrm{~cm}^{2} / \mathrm{s}$. Calculate $I_{s}$ and $\beta$ assuming the base width $W$ is:
(a) $1 \mu \mathrm{~m}$
(b) $2 \mu \mathrm{~m}$
(c) $5 \mu \mathrm{~m}$
2. Two transistors, fabricated with the same, technique, but having different junction areas, when operated at a base-emitter voltage of 0.69 V , have collector currents of 0.13 and 10.9 mA . Find $I_{S}$ for each device. What are the relative junction areas?
3. In a particular BJT, the base current is $7.5 \mu \mathrm{~A}$ and the collector current is $940 \mu \mathrm{~A}$. Find $\beta$ and $\alpha$ for the device.
4. For a properly biased $n-p-n$ transistor, the collector current is measured to be 1 mA and 10 mA for base-to-emitter voltages of 0.63 V and 0.7 V respectively. Find the corresponding values for $n$ and $I_{S}$ for this transistor. If two such devices are connected in parallel, and 0.65 V is applied between the combined base and the emitter in the conducting direction, what total current do you expect?
5. Show that in a transistor with $\alpha$ close to unity, if $\alpha$ changes by a small per unit amount $\Delta \alpha / \alpha$, the corresponding per unit change in $\beta$ is given by:

$$
\frac{\Delta \beta}{\beta}=\beta\left(\frac{\Delta \alpha}{\alpha}\right)
$$

6. From Problem 5, find $\Delta \beta / \beta$ when $\beta=100$ and $\alpha$ changes by 0.1 percent.
7. Consider the following diagrams.


What are the relative sizes of the diodes $D_{E}$ and $D_{B}$ for the transistors for which $\beta=10$ and $\beta=100$ ?
8. A particular BJT when conducting a collector current of 10 mA is known to have $v_{B E}=0.7 \mathrm{~V}$ and $i_{B}=100 \mu \mathrm{~A}$. Use this data to create a transistor model along the same lines as shown in the Problem 7.
9. The current $I_{C B O}$ of a small transistor is measured to be 15 mA at $25^{\circ} \mathrm{C}$. If the temperature of the device is raised to $75^{\circ} \mathrm{C}$, what do you expect $I_{C B O}$ to become?
10. Using the model of the transistor, as shown in the following diagram, consider the case of a transistor for which the base is connected to the ground, the collector is connected to a 10 V dc source through a $1 \mathrm{k} \Omega$ resistor and
a 5 mA current source is connected to the emitter so that the current is drawn out of the emitter terminal. If $\beta=100$ and $I_{S}=10^{-14} \mathrm{~A}$, find the voltages at the emitter and the collector, and calculate the base current.

11. A $p-n-p$ transistor has $V_{E B}=0.8 \mathrm{~V}$ at collector current 1 A . What do you expect the voltage to become at collector current 10 mA and 5 mA ?
12. A $p-n-p$ transistor has a common-emitter current gain of 50 . What is the common-base current gain?
13. Augment the model of the $n-p-n$ BJT, as shown in the following diagram, by a base current source representing $I_{C B O}$. In terms of this addition what do the terminal currents $i_{B}$, $i_{C}$ and $i_{E}$ become?

14. In Problem 13, if the base lead is open circuited while the emitter is connected to ground, and the collector is connected to a positive supply, find the emitter and collector currents.
15. The following diagram shows two large signal models of $p-n-p$ transistors operat-
ing in the active region. And this large signal model is applied to the transistor having $I_{S}=10^{-13} \mathrm{~A}$ and $\beta=40$. If the emitter is connected to ground, the base is connected to a current source that pulls out of the base terminal a current of $10 \mu \mathrm{~A}$, and the collector is connected to a negative supply of -10 V via a $10 \mathrm{k} \Omega$ resistor, find the base voltage, the collector voltage and the emitter current.

16. In the large signal models, as shown in the following diagrams, contrast the sizes of the two diodes for the situation in which $\beta=99$.


(c)

(d)
18. Measurements on the circuits, as shown in the following diagrams produce labeled voltages as indicated. Find the value of $\beta$ for each transistor.

(a)

4-42 | Basic Electronics

19. A particular $p-n-p$ transistor operating at an emitter current of 0.5 mA at $20^{\circ} \mathrm{C}$ has an emitter-base voltage of 692 mV .
(a) What does $v_{E B}$ become if the junction temperature rises to $50^{\circ} \mathrm{C}$ ?
(b) If the transistor has $n=1$ and is operated at a fixed emitter-base voltage of 700 mV , what emitter current flows at $20^{\circ} \mathrm{C}$ and at $50^{\circ} \mathrm{C}$ ?
20. For a particular $p-n-p$ transistor operating at a $v_{B E}$ of 670 mV and $I_{C}=3 \mathrm{~mA}$, the $i_{C}-v_{C E}$ characteristics has a slope of $3 \times 10^{-5} \mathrm{mho}$. To what value of output resistance does this correspond? What is the value of the Early voltage for this transistor? For operation at 30 mA , what should be the output resistance?
21. For a BJT having an early voltage of 200 V , what is the output resistance at 1 mA and at 100 A ?
22. For a BJT having an output resistance of $10 \mathrm{M} \Omega$ at $10 \mu \mathrm{~A}$, what will the early voltage be? If the current is raised to 10 mA , what does the output resistance become?
23. A BJT whose emitter current is fixed at 1 mA has the base-emitter voltage of 0.67 V at $25^{\circ} \mathrm{C}$. What base emitter voltage do you expect at $0^{\circ} \mathrm{C}$ and $100^{\circ} \mathrm{C}$ ?
24. The $p-n-p$ transistor, as shown in the following diagram, has $\beta=90$. Find the value of $R_{C}$ to obtain $V_{C}=5 \mathrm{~V}$. What happens when the transistor is replaced by another having $\beta=50$.

25. For the circuit, as shown in the following diagram, find the labeled node voltages for the following situations where:
(a) $\beta=$ infinity
(b) $\beta=89$
(c) $\beta=10$

26. Find the labeled voltages for the given values of $\beta=$ infinity and for $\beta=99$.


## SUGGESTED READINGS

1. Singh, J. 1994. Semiconductor Devices: An Introduction. New York: McGraw-Hill.
2. Streetman, B. G. and S. Banerjee. 2000. Solid State Electronic Devices. New Delhi: Pearson Education.
3. Millman, Jacob and ChristosC.Halkias. 1986. Integrated Electronics: Analog and Digital

Circuits and Systems. New Delhi: McGraw Hill Book Company.
4. Pierret R. F. and G.W. Neudeck. 1989. Modular Series on Solid State Devices. Boston, M.A.: Addison Wesley.

This page is intentionally left blank.

## 5

## BJT Circuits

## Outline

5-1 Introduction
5-2 Biasing and Bias Stability
5-3 Calculation of Stability Factors
5-4 CE, CB Modes and Their Properties
5-5 Small-Signal Low-Frequency Operation
of Transistors

5-6 Equivalent Circuits through<br>Hybrid Parameters as a Two-Port Network

5-7 Darlington Pair
5-8 Transistor at High Frequencies
5-9 Real-Life Applications of the Transistor

## Objectives

This chapter introduces biasing of BJT and bias stability. Biasing ensures that the transistor has proper gain and input impedance with undistorted output voltage when used as an amplifier. After the $Q$-point is established, maintaining the stability of the $Q$-point with respect to variations in temperature leads us to the concept of stability. Next, the small-signal low-frequency operation of the transistor is analysed. Here the circuit operates in the linear region and the calculations can be done using Kirchoff's voltage law and Kirchoff's circuit law. Transistor circuit models are described and designed using hybrid ( $h$ ) parameters. Finally, the frequency response for CE amplifier (with and without source impedance) for finding the bandwidth of the amplifier and few applications of transistors like emitter follower and Darlington pair are discussed in detail.

## 5-1 INTRODUCTION

The BJT as a circuit element operates various circuits with many major and minor modifications. For the analysis of such circuits, we obtain the various conditions for proper operation of the device, and also determine the projected range of operation of the device. A detailed study of the device in a two-port mode simplifies the circuit analysis of the device to a large extent. Thus, we calculate the various parameters of the devices' performance, namely voltage gain, current gain, input impedance, and output impedance. The frequency response of the device is dealt with in detail, and a study of the various regions of operation in the frequency scale is also explained.

Finally, we will discuss the various configurations of the device and take a look into the highfrequency operation of the device and its performance in those regions.

## 5-2 BIASING AND BIAS STABILITY

Biasing refers to the establishment of suitable dc values of different currents and voltages of a transistor. Through proper biasing, a desired quiescent operating point of the transistor amplifier in the active region (linear region) of the characteristics is obtained. The selection of a proper quiescent point generally depends on the following factors:
(a) The amplitude of the signal to be handled by the amplifier and distortion level in signal
(b) The load to which the amplifier is to work for a corresponding supply voltage

It is desired that the quiescent point be stable irrespective of changes in temperature or transistor characteristics. With the change in the input signal, the characteristics of the device should also change keeping the output of the device linear, i.e., undistorted.

The operating point of a transistor amplifier shifts mainly with changes in temperature, since the transistor parameters - $\beta, I_{C O}$ and $V_{B E}$ (where the symbols carry their usual meaning)-are functions of temperature.

The stability of a system is a measure of the sensitivity of a network or the transistor circuit to variations in parameters (mainly due to change in temperature). In any amplifier employing a transistor, the collector current $I_{C}$ is sensitive to each of the following parameters:
(a) $\beta$ increases with increase in temperature.
(b) $I_{C O}$ doubles in value for every 10 degree Celsius increase in temperature. This is the intrinsic current flowing, which is a strong function of temperature. The variation of silicon transistor parameters are shown in Table 5-1.

| Table 5-1 | Variation of silicon transistor <br> parameters with temperature |  |  |
| ---: | :---: | :---: | :--- |
| $T$ | $I_{C O}(\mathrm{nA})$ | $B$ | $V_{B E}(\mathrm{~V})$ |
| -65 | 0.0002 | 20 | 0.85 |
| 25 | 0.1 | 50 | 0.65 |
| 100 | 20 | 80 | 0.48 |
| 175 | 0.0033 | 120 | 0.3 |

Any or all of these factors can cause the bias point to drift from the designed or desired point of operation, thus, limiting the operation of the device in the linear region. This shift in the operating point may greatly vary the operation of the device and the output rather than changing the undistorted voltage swing to a distorted voltage swing.

## 5-2-1 Circuit Configurations

Here we study some of the circuit configurations where we design and analyse these particular configurations and their stability of operation.

## Fixed-bias circuit

The configuration, as shown in Figure 5-1(a), provides a relatively simple and easy introduction to the concept of biasing and their analysis. We consider the $n-p-n$ transistor and this method equally applies to the analysis of $p-n-p$ transistor. In the CE mode, for dc analysis, the circuit is made devoid of the ac source and the capacitor, as indicated in the equivalent circuit in Figure 5-1(b). We simply isolate the input and output, and analyse both of them independently.
$R_{B}$ indicates the resistance connected to the base lead, $R_{C}$ indicates the resistance connected to the collector leg of the transistor, and the respective currents are indicated as $I_{B}$ and $I_{C}$.


Figure 5-1 (a) Representation of fixed-bias circuit (b) Equivalent circuit

Base-emitter loop. From Figure 5-1, applying KVL to the input circuit, we obtain the following equation:

$$
\begin{gather*}
V_{C C}=I_{B} R_{B}+V_{B E}  \tag{5-1}\\
I_{B}=\frac{V_{C C}-V_{B E}}{R_{B}} \tag{5-2}
\end{gather*}
$$

Solving Equation (5-2) will result in obtaining the base current for this particular circuit configuration. Also, we see that the value of $I_{B}$ changes with the change in the value of the base resistor and the value of the dc voltage source.

Collector-emitter loop. In the collector-emitter loop, i.e., the output loop, applying KVL we obtain the following equation:

$$
\begin{equation*}
V_{C E}=V_{C C}-I_{C} R_{C} \tag{5-3}
\end{equation*}
$$

and,

$$
\begin{equation*}
I_{C}=\beta I_{B} \tag{5-4}
\end{equation*}
$$

Also,

$$
\begin{equation*}
V_{C E}=V_{C}-V_{E} \tag{5-5}
\end{equation*}
$$

In this case we have:

$$
V_{C E}=V_{C}
$$

Similarly, for $V_{B E}$ we obtain:

$$
\begin{equation*}
V_{B E}=V_{B}-V_{E} \tag{5-6}
\end{equation*}
$$

which, is equal to $V_{B}$, since $V_{E}$ is zero because in Figure 5-1 there is no resistance between the emitter terminal and ground.

It is worth mentioning that the voltage is measured with respect to ground. $V_{E}$ is the voltage between emitter and ground. $V_{B}$ is the voltage between base and ground. $V_{C}$ is the voltage between collector and ground.

The transistor saturation corresponds to the operation of the transistor in the saturation region. This stage corresponds to the operation when the collector is shorted to the emitter region and $V_{C E}=0 \mathrm{~V}$. Thus, from Equation (5-3) we get:

$$
I_{\mathrm{C}}=\frac{V_{C C}-V_{C E}}{R_{C}}
$$

Substituting $V_{C E}=0$ and $I_{C} \rightarrow I_{C \text { sat }}$, we get:

$$
\begin{equation*}
I_{C \text { sat }}=\frac{V_{C C}-0}{R_{C}}=\frac{V_{C C}}{R_{C}} \tag{5-7}
\end{equation*}
$$

## Fixed bias with emitter resistance

The only modification in the circuit is that an emitter resistor is kept at the emitter lead of the transistor. The analysis is very simple; only the resistor is kept at the emitter terminal. The circuit is as shown in Figure 5-2.

Figure 5-2 shows only a minor change from the previous configuration, i.e., a resistor $R_{E}$ is connected to the emitter leg of the transistor, and the current flowing through this resistor is given by $I_{E}$. All the other circuit components carry their usual meaning.

Base-emitter loop. For the base-emitter loop, we obtain the following equation:

$$
\begin{equation*}
V_{C C}=I_{B} R_{B}+V_{B E}+I_{E} R_{E} \tag{5-8}
\end{equation*}
$$

and the emitter current can be written as $I_{E}=(\beta+1) I_{B}$


Figure 5-2 Fixed-bias circuit with emitter resistance

Putting this value of $I_{E}$ in Equation (5-8) yields:

$$
\begin{equation*}
I_{B}=\frac{V_{C C}-V_{B E}}{R_{B}+(\beta+1) R_{E}} \tag{5-9}
\end{equation*}
$$

This circuit is very similar to the previous bias circuit; however, we have the extra term $(\beta+1) R_{E}$ as the only difference.

Collector-emitter loop. Applying KVL to the output loop, we obtain:

$$
\begin{equation*}
V_{C E}=V_{C C}-I_{C}\left(R_{C}+R_{E}\right) \tag{5-10}
\end{equation*}
$$

with the base current known, $I_{C}$ can be easily calculated by the relation $I_{C}=\beta I_{B}$. With this value of $I_{C}$, we can obtain the value of the collector current and collector voltage that gives a location on the output characteristics, and also provides the operating point. This location gives an indication whether the biasing of the BJT is proper at that point or not.

## Voltage-divider bias

The study of the previous circuits shows that the quiescent current and the quiescent voltage are dependent on the current gain $\beta$ of the transistor. However, knowing that $\beta$ is a temperature dependent factor, the design of such a circuit with these factors independent of $\beta$ is required. Such a design is provided in Figure 5-3.

This circuit is also called the self-bias circuit. In this circuit, we find that the voltage at the base is provided with the help of a voltage divider where, the resistors are indicated by $R_{1}$ and $R_{2}$.

The analysis of the input side is made exclusively by representing it through the Thevenins equivalent circuit. Thus, the Thevenins equivalent voltage for the input side is given by:

$$
\begin{equation*}
V_{T H}=V_{C C} \frac{R_{2}}{R_{1}+R_{2}} \tag{5-11}
\end{equation*}
$$



Figure 5-3 Voltage-divider bias circuit

The Thevenin resistance is given by:

$$
\begin{equation*}
R_{T H}=\frac{R_{1} R_{2}}{R_{1}+R_{2}} \tag{5-12}
\end{equation*}
$$

The equivalent circuit is shown in Figure 5-4.
The KVL equation for the input circuit [see Equation (5-9)] is given as:

$$
\begin{equation*}
I_{B}=\frac{V_{T H}-V_{B E}}{R_{T H}+(\beta+1) R_{E}} \tag{5-13}
\end{equation*}
$$

The KVL equation for the output circuit gives:

$$
I_{C}\left(R_{C}+R_{E}\right)+I_{B} R_{E}+V_{C E}=V_{C C}
$$

The output equation results in determining the collector-to-emitter voltage which is given by:

$$
\begin{equation*}
V_{C E}=V_{C C}-I_{C}\left(R_{C}+R_{E}\right) \tag{5-14}
\end{equation*}
$$

This gives us the quiescent operating point.

## Voltage-feedback biasing

The objective behind discussing these different topologies is to obtain a better stability. In our desire to obtain a more stable circuit, we end up with the circuit, which has a resistance $R_{B}$, included in the path connecting the base and the collector. The circuit for such a case is represented by Figure 5-5.


Figure 5-5 Representation of Voltage-feedback biased circuit

Base-emitter loop. The analysis for the base-emitter loop is as follows.
Applying KVL for this part, we get:

$$
\begin{equation*}
V_{C C}=I_{C}^{\prime} R_{C}+I_{B} R_{B}+V_{B E}+I_{E} R_{E}=\left(I_{C}+I_{B}\right) R_{C}+I_{B} R_{B}+V_{B E}+I_{E} R_{E} \tag{5-15}
\end{equation*}
$$

Neglecting $I_{B}$ for the reasons stated, we obtain:

$$
V_{C C}=I_{C} R_{C}+I_{B} R_{B}+V_{B E}+I_{E} R_{E}
$$

Here, it is important to note that the current $I_{C}^{\prime}=I_{C}+I_{B}$ is the sum of the current entering the base and the collector terminal of the BJT. But due to the design constraint of the transistor, the value of $I_{C}$ and $I_{C}^{\prime}$ far exceed the value of the base current. For a simpler analysis, we equate $I_{C}$ and $I_{C}^{\prime}$. Putting the values of $I_{C}$ and $I_{C}^{\prime}$ in Equation (5-15) results in:

$$
\begin{equation*}
V_{C C}=\beta I_{B} R_{C}+I_{B} R_{B}+V_{B E}+\beta I_{B} R_{E} \tag{5-16}
\end{equation*}
$$

Rearranging the terms of Equation (5-16) will result into:

$$
\begin{equation*}
V_{C C}-V_{B E}=I_{B}\left[R_{B}+\beta\left(R_{C}+R_{E}\right)\right] \tag{5-17}
\end{equation*}
$$

Thus, the base current can be obtained as:

$$
\begin{equation*}
I_{B}=\frac{V_{C C}-V_{B E}}{R_{B}+\beta\left(R_{C}+R_{E}\right)} \tag{5-18}
\end{equation*}
$$

## 5-2-2 Stabilization Against Variations in $I_{C O}, V_{B E}$, and $\beta$

Our focus should always be on the operation of the device under varying temperature conditions. In this regard, the following temperature dependent sources cause instability of the collector current $I_{C}$. These include:
(i) the reverse saturation current $I_{C O}$, which doubles itself for every $10^{\circ} \mathrm{C}$ increase in temperature;
(ii) the base-to-emitter voltage $V_{B E}$, which decreases at the rate of $2.5 \mathrm{mV} /{ }^{\circ} \mathrm{C}$ for both Ge and Si transistors;
(iii) $\beta$, which is a strong function of temperature, and increases with an increase in temperature.

We shall neglect the effect of the change of $V_{C E}$ with temperature because this variation is very small, and we can assume that the transistor operates in the active region where $I_{C}$ is approximately independent of $V_{C E}$. Under normal operation this value is near about 0.3 V when the transistor is operating in the saturation region.

## Transfer characteristic

In this particular characteristic, the output current $I_{C}$ is plotted (see Figure 5-6) as a function of input voltage for the germanium transistor. Thus, the word "transfer" is used for this characteristic.

Transfer characteristic in the case of a silicon transistor is shown in Figure 5-7.
In Figure 5-7 we can see that there is a shift of the curves towards the left at a rate of $2.5 \mathrm{mV} /{ }^{\circ} \mathrm{C}$ with constant $I_{C}$ and with an increase in temperature. We now examine in detail the effect of the shift in transfer characteristics and the variation of $\beta$ and $I_{C O}$ with temperature. This analysis makes it simpler


Figure 5-6 Transfer characteristics for germanium $p-n-p$ alloy type transistor


Figure 5-7 Collector current vs. base-to-emitter voltage for a silicon transistor
for us to analyse the variation of the operating point with all of these factors taken into consideration. For easy analysis and evaluation of various stability factors, we consider a self-bias circuit.

If the equation obtained from Figure 5-8-by applying KVL around the base-emitter circuit of the self-bias circuit-is combined with the equation obtained by applying KVL around the collector circuit that represents the collector characteristics in the active region, the resultant equation will be:

$$
\begin{equation*}
V_{B E}=V+\left(R_{b}+R_{e}\right) \frac{\beta+1}{\beta} I_{C O}-\frac{R_{b}+R_{e}(1+\beta)}{\beta} I_{C} \tag{5-19}
\end{equation*}
$$

Equation (5-19) represents a load line in the $I_{C}-V_{B E}$ plane, and is indicated in Figure 5-9. The intercept on the $V_{B E}$ axis is $V+V_{1}^{\prime}$, where:

$$
\begin{equation*}
V_{1}^{\prime}=\left(R_{b}+R_{e}\right) \frac{\beta+1}{\beta} I_{C O} \approx\left(R_{b}+R_{e}\right) I_{C O} \tag{5-20}
\end{equation*}
$$

$\beta \gg 1$, therefore, $\frac{\beta+1}{\beta}=1$.
If we put $T=T_{1}\left(T_{2}\right), I_{C O}=I_{C O_{1}}\left(I_{C O_{2}}\right)$ and $\beta=\beta_{1}\left(\beta_{2}\right)$, then we have:

$$
\begin{equation*}
V_{1}^{\prime} \approx\left(R_{b}+R_{e}\right) I_{C O_{1}} \tag{5-21}
\end{equation*}
$$

And consequently we obtain:

$$
\begin{equation*}
V_{2}^{\prime} \approx\left(R_{b}+R_{e}\right) I_{\mathrm{CO}_{2}} \tag{5-22}
\end{equation*}
$$

Thus, the intercept of the load line on the $V_{B E}$ axis is found to be dependent on temperature because $I_{C O}$ increases with $T$. The slope of the load line as obtained is:


Figure 5-8 Self-bias circuit


Figure 5-9 Variation of the collector current with temperature because of $V_{B E}, I_{C O}$ and $\beta$

$$
\begin{equation*}
\sigma=\frac{-\beta}{R_{b}+R_{e}(1+\beta)} \tag{5-23}
\end{equation*}
$$

and, as is evident, $|\sigma|$ increases with $T$ since $\beta$ increases with $T$. The transfer characteristic for $T=$ $T_{2}>T_{1}$ shifts to the left of the corresponding curve for $T=T_{1}$ as $V_{B E}$ (at constant $I_{C}$ ) varies with $T$, which is indicated above. The intersection of the load line with the transfer characteristic gives us the collector current $I_{C}$. We also see that $I_{C 2}>I_{C 1}$ because $I_{C O}, \beta$ and $V_{B E}$ all vary with temperature.

From Equation (5-19) it is seen that with $I_{C}$ being a function of $I_{C O}, V_{B E}$ and $\beta$, it is possible to introduce the three partial derivatives of $I_{C}$ with respect to these variables in order to indicate the variation of $I_{C}$ with respect to each of the independent parameters, taken one at a time. These derivatives are called the stability factors $S, S^{\prime}$ and $S^{\prime \prime}$.

## 5-3 CALCULATION OF STABILITY FACTORS

## 5-3-1 Stability Factor $S$

We here define the stability factor $S$, as the change of collector current with respect to the reverse saturation current, keeping $\beta$ and $V_{B E}$ constant. This can be written as:

$$
\begin{equation*}
S \equiv \frac{\partial I_{C}}{\partial I_{C O}} \tag{5-24}
\end{equation*}
$$

The larger the value of $S$, the more likely it is for the circuit to be thermally unstable, i.e., the operation of the device will be marked by the change in operating temperature. Using the above definition and Equation (5-19), we find:

$$
\begin{equation*}
S=(1+\beta) \frac{1+R_{b} / R_{e}}{1+\beta+R_{b} / R_{e}} \tag{5-25}
\end{equation*}
$$

If $R_{b} / R_{e} \simeq 1, S \approx 1, R_{b} / R_{e} \rightarrow \infty$ and $S \approx 1+\beta, S$ remains between 1 and $1+\beta$.

If $(\beta+1) \gg R_{b} / R_{e}$, then Equation (5-25) reduces to:

$$
\begin{equation*}
S=1+\frac{R_{b}}{R_{e}} \tag{5-26}
\end{equation*}
$$

Thus, for constant $\beta, V_{B E}$ and small $S$, we obtain:

$$
\begin{equation*}
\frac{\Delta I_{C}}{I_{c}} \approx S \frac{\Delta I_{C O}}{I_{c}} \approx \frac{\Delta I_{C O}}{I_{C}}+\frac{R_{b}}{R_{e}} \frac{\Delta I_{C O}}{I_{C}} \tag{5-27}
\end{equation*}
$$

For the typical design $R_{b} / R_{e}>1$, we make the second term in Equation (5-28) larger than the first term. The denominator of the second term is the dc voltage drop across $R_{e}$ (since $\left|I_{C}\right| \approx\left|I_{e}\right|$ ) and should always be under the circuit designer's supervision for its operation to be controlled.

## 5-3-2 Stability Factor $S^{\prime}$

The variation of $I_{C}$ with $V_{B E}$ is given by the stability factor $S^{\prime}$ defined by the partial derivative:

$$
\begin{equation*}
S^{\prime} \equiv \frac{\partial I_{C}}{\partial V_{B E}} \approx \frac{\Delta I_{C}}{\Delta V_{B E}} \tag{5-28}
\end{equation*}
$$

where, both $I_{C O}$ and $\beta$ are considered to be constant.
From Equation (5-19) we find:

$$
\begin{equation*}
S^{\prime}=\frac{-\beta}{R_{b}+R_{e}(1+\beta)}=\frac{-\beta / R_{e}}{1+\beta+R_{b} / R_{e}} \tag{5-29}
\end{equation*}
$$

Again, if we assume that $\beta+1 \gg R_{b} / R_{e}$ and also that $\beta \gg 1$, then from Equation (5-29) we obtain:

$$
\begin{align*}
& S^{\prime} \approx \frac{\Delta I_{C}}{\Delta V_{B E}} \approx-\frac{1}{R_{e}}  \tag{5-30}\\
& \quad \frac{\Delta I_{C}}{I_{C}} \approx \frac{S^{\prime} \Delta V_{B E}}{I_{C}} \approx-\frac{\Delta V_{B E}}{I_{C} R_{e}} \tag{5-31}
\end{align*}
$$

From Equation (5-31) and Equation (5-27) we find that the dominant factor is stabilising against $I_{C O}$ and $V_{B E}$ is the quiescent voltage drop across the emitter resistance $R_{e}$. The larger the drop, the smaller is the percentage change in collector current because of the changes in $I_{C O}$ and $V_{B E}$.

## 5-3-3 Stability Factor $S^{\prime \prime}$

The variation of $I_{C}$ with respect to $\beta$ is represented by the stability factor, $S^{\prime \prime}$, given as:

$$
\begin{equation*}
S^{\prime \prime} \equiv \frac{\partial I_{C}}{\partial \beta} \approx \frac{\Delta I_{C}}{\Delta \beta} \tag{5-32}
\end{equation*}
$$

where, both $I_{C O}$ and $V_{B E}$ need to be considered constant. From Eq (5-19):

$$
\begin{equation*}
I_{C}=\frac{\beta\left(V+V^{\prime}-V_{B E}\right)}{R_{b}+R_{e}(1+\beta)} \tag{5-33}
\end{equation*}
$$

From Equation (5-20), $V^{\prime}$ may be taken to be independent of $\beta$. After differentiation and algebraic manipulation we obtain:

$$
\begin{equation*}
S^{\prime \prime}=\frac{\partial I_{C}}{\partial \beta}=\frac{I_{C} S}{\beta(1+\beta)} \tag{5-34}
\end{equation*}
$$

The change in the collector current due to a change in $\beta$ is given by:

$$
\begin{equation*}
\Delta I_{C} \approx S^{\prime \prime} \Delta \beta=\frac{I_{C} S}{\beta(1+\beta)} \Delta \beta \tag{5-35}
\end{equation*}
$$

where, $\Delta \beta=\beta_{2}-\beta_{1}$ may represent a large change in $\beta$. Thus, it is not clear whether to use $\beta_{1}, \beta_{2}$ or some average value of $\beta$ in the expressions for $S^{\prime \prime}$. This difficulty is avoided if $S^{\prime \prime}$ is obtained by taking finite differences rather than by evaluating a derivative. Thus:

$$
\begin{equation*}
S^{\prime \prime} \approx \frac{I_{C 2}-I_{C 1}}{\beta_{2}-\beta_{1}}=\frac{\Delta I_{C}}{\Delta \beta} \tag{5-36}
\end{equation*}
$$

From Equation (5-33) we have:

$$
\begin{equation*}
\frac{I_{C 2}}{I_{C 1}}=\frac{\beta_{2}}{\beta_{1}} \frac{R_{b}+R_{e}\left(1+\beta_{1}\right)}{R_{b}+R_{e}\left(1+\beta_{2}\right)} \tag{5-37}
\end{equation*}
$$

Subtracting 1 from both sides of Equation (5-33) yields:

$$
\begin{array}{r}
\frac{I_{C 2}}{I_{C 1}}-1=\left(\frac{\beta_{2}}{\beta_{2}}-1\right) \frac{R_{b}+R_{e}}{R_{b}+R_{e}\left(1+\beta_{2}\right)} \\
S^{\prime \prime}=\frac{\Delta I_{C}}{\Delta \beta}=\frac{I_{C 1} S_{2}}{\beta_{1}\left(1+\beta_{2}\right)} \tag{5-39}
\end{array}
$$

or,

It is clear that $R_{b} / R_{e}$ should be kept small. Also, for a given spread in the value of $\beta$, a high- $\beta$ circuit will be more stable than one using a lower- $\beta$ transistor.

## 5-3-4 General Remarks on Collector Current Stability

The stability factors have been defined earlier keeping in mind the change in collector current with respect to changes in $I_{C O}, V_{B E}$ and $\beta$. These stability factors are repeated here for simplicity.

$$
\begin{equation*}
S=\frac{\Delta I_{C}}{\Delta I_{C O}}, \quad S^{\prime}=\frac{\Delta I_{C}}{\Delta V_{B E}}, \quad S^{\prime \prime}=\frac{\Delta I_{C}}{\Delta \beta} \tag{5-42}
\end{equation*}
$$

Each differential quotient is calculated with all other parameters kept constant. If we desire to obtain the total change in collector current over a specified temperature range, we can do so by expressing this change as the sum of the individual changes due to the stability factors calculated from the variation of $I_{C O}, V_{B E}$ and $\beta$. Thus, by taking the total differential of $I_{C}=f\left(I_{C O}, V_{B E}, \beta\right)$, we obtain:

$$
\begin{align*}
\Delta I_{C} & =\frac{\partial I_{C}}{\partial I_{C O}} \Delta I_{C O}+\frac{\partial I_{C}}{\partial V_{B E}} \Delta V_{B E}+\frac{\partial I_{C}}{\partial \beta} \Delta \beta  \tag{5-43}\\
& =S \Delta I_{C O}+S^{\prime} \Delta V_{B E}+S^{\prime \prime} \Delta \beta \tag{5-44}
\end{align*}
$$

Equation (5-44) gives the summary of all the explanations given earlier regarding change in collector current or in other words, the essence of stability factors. The stability factors may be expressed in terms of the parameter $M$ defined by:

$$
\begin{equation*}
\mathrm{M} \equiv \frac{1}{1+R_{b} /\left[R_{e}(1+\beta)\right]} \approx \frac{1}{1+R_{b} / \beta R_{e}} \tag{5-45}
\end{equation*}
$$

In this case we assume $\beta \gg 1$. Note that if, $\beta R_{e} \gg R_{b}$, then $M \approx 1$. Substituting Equations (5-22), (5-26) and (5-36) in Equation (5-39) for the fractional (minute) change in collector current we get:

$$
\begin{equation*}
\frac{\Delta I_{C}}{\Delta_{C 1}}=\left(1+\frac{R_{b}}{R_{e}}\right) \frac{M_{1} \Delta I_{C O}}{I_{C 1}}-\frac{M_{1} \Delta V_{B E}}{I_{C 1} R_{e}}+\left(1+\frac{R_{b}}{R_{e}}\right) \frac{M_{2} \Delta \beta}{\beta_{1} \beta_{2}} \tag{5-46}
\end{equation*}
$$

where $M_{1}\left(M_{2}\right)$ corresponds to $\beta_{1}\left(\beta_{2}\right)$. As $T$ increases, $\Delta I_{C O} / I_{C_{1}}$ and $\Delta \beta$ increase, and $\Delta V_{B E} / I_{C_{1}}$ decreases. Hence all the terms in Equation (5-42) are positive for an increase in $T$ and negative for a decrease in $T$.

## 5-4 CE, CB MODES AND THEIR PROPERTIES

## 5-4-1 Common-Emitter (CE) Mode

## Input characteristics

The input characteristiscs are as shown in Figure $5-10$. Here $I_{B}$ is the input current, $V_{B E}$ is the input voltage and $V_{C E}$ is the output voltage. The variation of the base current $I_{B}$ with respect to the base-to-emitter voltage $V_{B E}$, considering $V_{C E}$ as a constant is shown in Figure 5-10. This set of curves represents the CE input characteristics. The characteristics are similar to that of a forward-biased diode. However, for a constant $V_{B E}$, the magnitude of the base current decreases with an increase in $V_{C E}$. This is because, with an


Figure 5-10 Input characteristic for commonemitter configuration
increasing $V_{C E}$ the effective base width decreases and thus, the recombination base current also decreases.

## Output characteristics

The output characteristics are as shown in Figure 5-11(a).

Here the collector current $I_{C}$ is plotted against the collector-toemitter voltage $V_{C E}$ with base current $I_{B}$ as parameter. The characteristics can be divided into three regions:

Active region. In this region the transistor works in a mode where the emitter-base junction is forwardbiased and the collector-base junction reverse-biased. A transistor when


Figure 5-11(a) Plot of the collector current against the collector-to-emitter voltage operated in the active region can be used to amplify signals almost faithfully, as this region corresponds to the linear region or rather the device bears a linear relationship between the input and the output signals. In this region the characteristics of the device change according to the changes in the input signal, thus keeping the output a faithful replication of the input signal. The output characteristics in the active region are not horizontal lines. This is because, for a fixed value of the base current $I_{B}$ the magnitude of the collector current increases with $V_{C E}$ (due to Early effect).

Cut-off region. For operation in the CE mode, only by making the base current $I_{B}=0$, the cut-off collector current or $I_{C O}$ is not obtained. It is also necessary to reverse-bias the emitter-base junction only for it to be zero; the collector current can be equal to $I_{C O}$ (applicable only for germanium transistors). Thus, this region of operation corresponds to the operation of the device in which the both the emitter-base and the collector-base junctions are reverse-biased, and the current is solely in the reverse saturation region. Its magnitude is very small.

Saturation region. A transistor operating in this particular region has both the collector-base and the emitter-base junctions forward-biased by at least the cutin $(V \gamma)$ voltage. Under this condition the

Table 5-2 Definitions of transistor states

| Transistor State or | Junction Biasing |  |
| :--- | :---: | :---: |
| Operating Mode | Base-Emitter | Base-Collector |
| Forward active | Forward | Reverse |
| Reverse active | Reverse | Forward |
| Cut-off | Reverse | Reverse |
| Saturation | Forward | Forward |



Figure 5-11(b) Transistor states defined by junction biasing
collector current becomes approximately independent of the base current, and the current at the collector attains an overall saturation value.

Table 5-2 provides the four different transistor states under four different combinations of biasing, and Figure 5-11(b) illustrates the operating modes.

## 5-4-2 Common-Base Mode

This configuration corresponds to the arrangement in which the base is common to both the input and the output of the circuit concerned.

## Input characteristics

The input characteristics are as shown in Figure 5-12. In this case, the emitter current is the input current, and the emitter-base voltage is the input voltage. The collector -base voltage is the output voltage. The variation of the emitter current with respect to the emitter-to-base voltage is equivalent to the situation in a forward-biased $p-n$ junction. But due to Early effect, an increase in the magnitude of the collector voltage $V_{C B}$ causes the emitter current to increase for a definite $V_{E B}$.


Figure 5-12 Input characteristics


Figure 5-13 Output characteristics

## Output characteristics

The output characteristics are as shown in Figure 5-13. Here the current flowing in the collector is the output current, and the collector-to-base voltage is the output voltage. The emitter current is the input current in this case. Again there are three regions in the characteristic curve that can be clearly distinguished.

Active region. In this region the collector junction is biased in the reverse direction and the emitter junction in the forward direction. Let us first assume that the emitter current is zero. Then, as is evident, the collector current is small and equals the reverse saturation current $I_{C O}$ (microamperes for Ge and nanoamperes for Si ) of the collector junction, which might be considered as a diode. Now, suppose that the forward emitter current $I_{E}$ is made to flow in the emitter circuit. Then a fraction of $-\alpha I_{E}$ of this current will reach the collector, and the actual value of the collector current $I_{C}$ is thus given by:

$$
\begin{equation*}
I_{C}=I_{C O}-\alpha I_{E} \tag{5-47}
\end{equation*}
$$

In the active region the collector current is mostly independent of the collector voltage and depends on the emitter current. However, because of Early effect there is actually a change and thus, an increase in $\left|I_{C}\right|$ with respect to $\left|V_{C B}\right|$. Because $\alpha$ is less than but almost equal to 1 , the magnitude of the collector current is slightly less than the emitter current. Physically, it can be clearly realised that a part of the emitter current goes on to recombine with the carriers in the base region.

Saturation region. This region is located to the left of the line $V_{C B}=0$ and above the output characteristic of $I_{E}=0$. This region is realised by forward-biasing of both the emitter-base and the collector-base junctions. Forward-biasing of the collector-base junction results in an exponential variation in the collector current, and thus, accounts for a large change in the collector current with $V_{C B}$ in the saturation region.

Cut-off region. The region to the right of the line $V_{C B}=0$ and below the characteristic for $I_{E}=0$ is the cut-off region of the transistor. In this region the operation of the transistor is realised by reversebiasing both the emitter-base and the collector-base junctions.

## Solved Examples

Example 5-1 For the circuit shown in the diagram:
(a) Calculate $I_{B}, I_{C}$, and $V_{C E}$ if a silicon transistor is used with $\beta=100$.
(b) Specify a value for $R_{b}$ so that $V_{C E}=7 \mathrm{~V}$.


## Solution:

(a) Applying KVL around the loop $V_{C C}-C-B-E$, we have:

$$
V_{C C}=R_{C}\left(I_{B}+I_{C}\right)+I_{B} R_{b}+V_{B E}
$$

or,

$$
I_{B}=\frac{V_{C C}-V_{B E}}{\beta R_{C}+R_{C}+R_{B}}
$$

But the transistor is in the active region, hence, $I_{C}=100 I_{B}$ and $V_{B E}=0.70$.
Substituting these values yields:

$$
I_{B}=\frac{10 \mathrm{~V}-0.7 \mathrm{~V}}{100 \times 2 \mathrm{k} \Omega+2 \mathrm{k} \Omega+100 \mathrm{k} \Omega}
$$

or,

$$
I_{B}=\frac{9.30 \mathrm{~V}}{302 \mathrm{k} \Omega}=0.031 \mathrm{~mA}
$$

and

$$
I_{C}=100 \times 0.031 \mathrm{~mA}=3.1 \mathrm{~mA}
$$

Then

$$
V_{C E}=V_{C C}-\left(I_{B}+I_{C}\right) R_{C}=3.74 \mathrm{~V}
$$


(b) Given $V_{C E}=7 \mathrm{~V}$

We apply KVL in the collector-emitter circuit and we have:

$$
I_{C}+I_{B}=\frac{V_{C C}-V_{C E}}{R_{C}}=\frac{3 \mathrm{~V}}{2 \mathrm{k} \Omega}=1.5 \mathrm{~mA}
$$

or,

$$
I_{B}=\frac{1.5 \mathrm{~mA}}{101}=0.01485 \mathrm{~mA}
$$

and

$$
I_{C}=100 I_{B}=1.485 \mathrm{~mA}
$$

Applying KVL around the loop $V_{C C}-C-B-E$, we have:

$$
\begin{aligned}
& V_{C C}=R_{C}\left(I_{B}+I_{C}\right)+I_{B} R_{b}+V_{B E} \\
& \quad R_{b}=\frac{V_{C C}-V_{B E}-R_{B}\left(I_{C}+I_{B}\right)}{I_{B}} \\
& R_{b}=\frac{10 \mathrm{~V}-0.7 \mathrm{~V}-2 \mathrm{k} \Omega \times 1.5 \mathrm{~mA}}{0.01485 \mathrm{~mA}}=424.24 \Omega
\end{aligned}
$$

or,
Example 5-2 (a) In Figure 5-8 verify the stability factor $S=(1+\beta) \frac{1+\frac{R_{b}}{R_{e}}}{1+\beta+\frac{R_{b}}{R_{e}}}$
(b) Show that for the circuit of Example 5-1, S is given by:

$$
S=\frac{\beta+1}{1+\beta R_{c} /\left(R_{c}+R_{b}\right)}
$$

Solution:
Solution:
(a) From Figure 5-8, solving for $I_{B}$ we get: $\quad I_{B}=\frac{V-V_{B E}-I_{C} R_{e}}{R_{e}+R_{b}}$
From Equation (5-19) we have:
or,

$$
I_{C}=(1+\beta) I_{C O}+\beta I_{B}=(1+\beta) I_{C O}+\frac{\beta}{R_{e}+R_{b}}\left(V-V_{B E}-I_{C} R_{e}\right)
$$

$$
I_{C}\left(1+\frac{\beta R_{e}}{R_{e}+R_{b}}\right)=(1+\beta) I_{C O}+\frac{\beta}{R_{e}+R_{b}}\left(V-V_{B E}\right)
$$

Then,

$$
s=\frac{\partial I_{C}}{\partial I_{C O}}=\frac{1+\beta}{1+\frac{\beta R_{e}}{R_{e}+R_{b}}}=(1+\beta) \frac{1+\frac{R_{b}}{R_{e}}}{1+\beta+\frac{R_{b}}{R_{e}}}
$$

(b) Applying KVL around $V_{C C}-C-B-E$, we have:

$$
V_{C C}=I_{C} R_{c}+\left(\mathrm{R}_{b}+\mathrm{R}_{c}\right) I_{B}+V_{B E}
$$

But,

$$
I_{C}=\beta I_{B}+(1+\beta) I_{C O}
$$

Thus, we have:

$$
V_{C C}=I_{C} R_{c}+\frac{R_{b}+R_{c}}{\beta} I_{C}-\left(R_{b}+R_{c}\right) \frac{(1+\beta)}{\beta} I_{C O}+V_{B E}
$$

Differentiating the equation for $V_{C C}$ with respect to $I_{C O}$, we obtain:

$$
\begin{aligned}
& {\left[R_{c}+\frac{R_{b}+R_{c}}{\beta}\right] \frac{\partial I_{C}}{\partial I_{C O}}=\left(R_{b}+R_{c}\right) \frac{(1+\beta)}{\beta}} \\
& \text { or, } \quad S=\frac{\partial I_{C}}{\partial I_{C O}}=\frac{\left(R_{b}+R_{c}\right)(1+\beta)}{R_{b}+R_{c}+\beta R_{c}}=\frac{(1+\beta)}{1+\frac{\beta R_{c}}{\left(R_{b}+R_{c}\right)}}
\end{aligned}
$$

Example 5-3 For the two-battery transistor circuit as shown in the diagram, prove that the stabilization factor $S$ is given by:

$$
S=\frac{1+\beta}{\frac{1+\beta R_{e}}{R_{e}+R_{b}}}
$$

## Solution:

Neglecting $V_{B E}$ we obtain from the base circuit:

$$
V_{1}=I_{E} R_{e}-I_{B} R_{b}
$$

But $I_{E}=-\left(I_{B}+I_{C}\right)$; thus, $V_{1}=-\left(I_{B}+I_{C}\right) R_{e}-I_{B} R_{b}$
 or, $\quad I_{B}=-\frac{I_{C} R_{e}+V_{1}}{R_{e}+R_{b}}$

$$
\begin{aligned}
I_{C} & =(1+\beta) I_{C O}+\beta I_{B} \\
& =(1+\beta) I_{C O}-\frac{\beta}{R_{e}+R_{b}}\left(I_{C} R_{e}+V_{1}\right)
\end{aligned}
$$

or, $I_{C}\left(1+\frac{\beta R_{e}}{R_{e}+R_{b}}\right)=(1+\beta) I_{C O}-\frac{\beta V_{1}}{R_{e}+R_{b}}$

$$
S=\frac{\partial I_{C}}{\partial I_{C O}}=\frac{(1+\beta)}{1+\frac{\beta \mathrm{R}_{e}}{R_{e}+R_{b}}}
$$



Example 5-4 Assume that a silicon transistor with $\beta=50, V_{B E(a c t i v e)}=0.7 \mathrm{~V}, V_{C C}=22.5 \mathrm{~V}$ and $R_{c}=5.6 \mathrm{~K}$ is used in the given diagram. It is desired to establish a $Q$-point at $V_{C E}=12 \mathrm{~V}$, $I_{C}=1.5 \mathrm{~mA}$, and stability factor $S \leq 3$. Find $R_{e}, R_{1}$ and $R_{2}$.


## Solution:

The dc equivalent of the given diagram is as shown.
The current in $R_{e}$ is $I_{C}+I_{B} \approx I_{C}$. Hence, from the collector circuit, we obtain:

$$
R_{e}+R_{c}=\frac{V_{C C}-V_{C E}}{I_{C}}=\frac{22.5 \mathrm{~V}-12 \mathrm{~V}}{1.5 \mathrm{~mA}}=7.0 \mathrm{k} \Omega
$$

or, $\quad R_{e}=(7.0-5.6) \mathrm{k} \Omega=1.4 \mathrm{k} \Omega$. Solving for $R_{b} / R_{e}$, we get:

$$
3=51 \times \frac{1+R_{b} R_{e}}{51+R_{b} / R_{e}} \quad(\text { Considering } S=3)
$$

or,

$$
R_{b} / R_{e}=2.12
$$

Hence,

$$
R_{b}=(2.12 \times 1.4) \mathrm{k} \Omega=2.96 \mathrm{k} \Omega
$$

If $R_{b}<2.96$ then $S<3$.
The base current is:

$$
I_{B}=\frac{I_{C}}{\beta}=\frac{1.5}{50}=30 \mu \mathrm{~A}
$$



Solving for $R_{1}$ and $R_{2}$, we find:

$$
R_{1}=R_{b} \times \frac{V_{C C}}{V} \text { and } R_{2}=\frac{R_{1} V}{V_{C C}-V}
$$

But we have:

$$
V=0.030 \times 2.96+0.7+(0.03+1.5) \times 1.4=2.93 \mathrm{~V}
$$

Thus,

$$
R_{1}=\frac{2.96 \times 22.5}{2.93}=22.8 \mathrm{~K} \text { and } R_{2}=\frac{22.8 \times 2.93}{22.5-2.93}=3.4 \mathrm{~K}
$$

Example 5-5 (a) A germanium transistor is used in the self-biasing arrangement, as shown in the following figure, with $V_{C C}=20 \mathrm{~V}$ and $R_{c}=1.5 \mathrm{~K}$. The quiescent point is chosen to be $V_{C E}=8 \mathrm{~V}$ and $I_{C}=4 \mathrm{~mA}$. A stability factor $S=12$ is desired. If $\beta=50$, find $R_{1}, R_{2}$ and $R_{e}$.
(b) Repeat part (a) for $S=3$.

## Solution:

(a) $I_{B}=\frac{I_{C}}{\beta}=\frac{4}{50}=80 \mu \mathrm{~A}$

Hence, $\quad R_{e}=\frac{V_{C C}-V_{C E}-I_{C} R_{c}}{I_{B}+I_{C}}$

$$
=\frac{20 \mathrm{~V}-8 \mathrm{~V}-4 \mathrm{~mA} \times 1.5 \mathrm{k} \Omega}{4.08 \mathrm{~mA}}=1.47 \mathrm{k} \Omega
$$

$$
S=12=51 \times \frac{1+\frac{R_{b}}{R_{e}}}{51+\frac{R_{b}}{R_{e}}}
$$

or, $\quad \frac{R_{b}}{R_{e}}=14.4$ and $R_{b}=21.17 \mathrm{k} \Omega$


The base-to-ground voltage:

$$
V_{B N}=V_{B E}-I_{E} R_{e}=0.2 \mathrm{~V}+4.08 \mathrm{~mA} \times 1.47 \mathrm{k} \Omega=5.91 \mathrm{~V}
$$

The Thevenin voltage is:

$$
V=V_{B N}+I_{B} R_{b}=5.91 \mathrm{~V}+0.08 \mathrm{~mA} \times 21.17 \mathrm{k} \Omega=7.60 \mathrm{~V}
$$

We have:

$$
\frac{V}{R_{b}}=\frac{V_{C C}}{R_{1}}=\frac{20}{R_{1}}
$$

$$
\begin{array}{ll}
\therefore & R_{1}=\frac{20 \mathrm{~V} \times R_{b}}{V} \\
& =\frac{20 \mathrm{~V} \times 21.17 \mathrm{k} \Omega}{7.60 \mathrm{~V}}=55.71 \mathrm{k} \Omega
\end{array}
$$

Then,

$$
I_{R 1}=\frac{V_{C C}-V_{B N}}{R_{1}}=\frac{20 \mathrm{~V}-5.91 \mathrm{~V}}{55.71 \mathrm{k} \Omega}=0.253 \mathrm{~mA}
$$

and

$$
I_{R 2}=I_{R 1}-I_{B}=0.173 \mathrm{~mA}
$$

Hence,

$$
R_{2}=\frac{V_{B N}}{I_{R 2}}=\frac{5.91 \mathrm{~V}}{0.173 \mathrm{~mA}}=34.16 \mathrm{k} \Omega
$$

(b) $R_{e}=1.47 \mathrm{k} \Omega$

$$
S=3=51 \times \frac{1+\frac{R_{b}}{R_{e}}}{51+\frac{R_{b}}{R_{e}}}
$$

or,

$$
\frac{R_{b}}{R_{e}}=2.13 \quad \text { and } \quad R_{b}=3.13 \mathrm{k} \Omega
$$

Then,

$$
V=5.91 \mathrm{~V}+0.08 \mathrm{~mA} \times 3.13 \mathrm{k} \Omega+6.16 \mathrm{~V}
$$

Thus,

$$
\frac{V}{R_{b}}=\frac{V_{C C}}{R_{1}}
$$

$$
\therefore \quad R_{1}=\frac{V_{C C} R_{b}}{V}=\frac{20 \mathrm{~V} \times 3.13 \mathrm{k} \Omega}{6.16 \mathrm{~V}}=10.16 \mathrm{k} \Omega
$$

$$
I_{R 1}=\frac{20 \mathrm{~V}-5.91 \mathrm{~V}}{10.16 \mathrm{k} \Omega}=1.387 \mathrm{~mA}
$$

$$
I_{R 2}=1.387 \mathrm{~mA}-0.08 \mathrm{~mA}=1.307 \mathrm{~mA}
$$

$$
\therefore \quad R_{2}=\frac{5.91 \mathrm{~V}}{1.307 \mathrm{~mA}}=4.52 \mathrm{k} \Omega
$$

Example 5-6 In the transformer coupled amplifier stage, as shown, $V_{B E}=0.7 \mathrm{~V}, \beta=50$, and the quiescent voltage is $V_{C E}=4 \mathrm{~V}$. Determine (a) $R_{e}$ (b) the stability factor $S$.


## Solution:

(a) Collector-emitter circuit:

$$
V_{C C}-V_{E E}=R_{c} I_{C}+R_{e}\left(I_{C}+I_{B}\right)+V_{C E}
$$

or,

$$
\begin{equation*}
18 \mathrm{~V}=4.3 \mathrm{k} \Omega \times I_{C}+R_{e}\left(1+\frac{1}{50}\right) I_{C}+4 \mathrm{~V} \tag{1}
\end{equation*}
$$

Base-emitter circuit:

$$
-V_{E E}=\left(I_{C}+I_{B}\right) R_{e}+V_{B E}
$$

or,

$$
\begin{equation*}
6=\left(1+\frac{1}{50}\right) I_{C} R_{e}+0.7 \tag{2}
\end{equation*}
$$

Solving Equations (1) and (2) simultaneously, we get $I_{C}=2 \mathrm{~mA}$ and $R_{e}=2.74 \mathrm{~K}$
(b) Comparing the circuit given with that in the following diagram:

we see that they are similar except here $R_{b}=0$. The equation for $S$, therefore, is valid with $R_{b}=0$. Under this condition $S=1$.


## 5-5 SMALL-SIGNAL LOW-FREQUENCY OPERATION OF TRANSISTORS

The small signal model of a transistor operates with reasonable linearity and consequently, requires a small-signal linear model that can represent the operation of the transistor in the active region. This small-signal model is required for the analysis of the system where the input signal has amplitude, which is small in relation to the proximity of the region in the output characteristics where the device operates linearly. One such important model is the $h$-parameter model that makes the analysis of these particular types of transistors excessively easy and lucid.

## 5-5-1 Hybrid Parameters and Two-Port Network

For the hybrid equivalent model to be described, the parameters are defined at an operating point that may or may not give an actual picture of the operating condition of the amplifier. The quantities $h_{i e}, h_{r e}$, $h_{f e}$ and $h_{o e}$ are called the hybrid parameters and are the components of a small-signal equivalent circuit.

The description of the hybrid equivalent model begins with the general two-port system as shown in Figure 5-14.

$$
\begin{align*}
& V_{i}=h_{11} I_{i}+h_{12} V_{o} \\
& I_{o}=h_{21} I_{i}+h_{22} V_{o} \tag{5-48}
\end{align*}
$$

Figure 5-14 is a black box model realization of the whole circuit. The parameters relating the four variables are called $h$-parameters, derived from the word "hybrid". The term hybrid was chosen because the mixture of variables ( $V$ and $I$ ) in each equation results in a "hybrid" set of units of measurement for these $h$-parameters.
Now, setting $V_{o}=0$ (short circuit the output terminals) and solving for $h_{11}$ we obtain:

$$
\begin{equation*}
h_{11}=\left.\frac{V_{i}}{I_{i}}\right|_{V_{o}=0} \text { ohms } \tag{5-49}
\end{equation*}
$$



Figure 5-14 Two-port system representation (Black model realisation)

Since $h_{11}$ is the ratio of the input voltage to the input current with the output terminals shorted, it is termed as the short-circuit input-impedance parameter. The subscript 11 of $h_{11}$ defines the fact that the parameter is determined by a ratio of quantities measured at the input terminals.

If $I_{i}$ is set to zero, i.e., by opening the input leads and replacing this condition in Equation (5-49), we get the value of $h_{12}$ as:

$$
\begin{equation*}
h_{12}=\frac{V_{i}}{\left.V_{o}\right|_{i}=0} \tag{5-50}
\end{equation*}
$$

It has no units since it is a ratio of voltage levels and is called the open-circuit reverse transfer voltage ratio parameter. The subscript 12 of $h_{12}$ reveals the fact that the parameter is a transfer quantity determined by the ratio of input to output measurements.

Now, we set $V_{o}=0$ by shorting the output terminals. The following will result for $h_{21}$ :

$$
\begin{equation*}
h_{21}=\left.\frac{I_{o}}{I_{i}}\right|_{V_{o}=0} \tag{5-51}
\end{equation*}
$$

It is also a unit less since it is the ratio of the current levels. It is formally called the short-circuit forward transfer current ratio parameter. The subscript 21 indicates that it is a transfer parameter with the ratio of output to input quantity.

The last parameter $h_{22}$, which can be found by again opening the input leads to set $I_{i}=0$. Thus, by replacing this condition in the basic sets of equations, we obtain:

$$
\begin{equation*}
h_{22}=\left.\frac{I_{o}}{V_{o}}\right|_{I_{i}=0} \text { siemens } \tag{5-52}
\end{equation*}
$$

Since it is the ratio of output current to the output voltage, it is the output conductance parameter, and is measured in siemens (S). It is called the open-circuit output admittance parameter. The subscript 22 reveals that it is determined by a ratio of output quantities. Therefore, we have:
(i) $h_{11} \rightarrow$ input impedance $\rightarrow h_{i}$
(ii) $h_{12} \rightarrow$ reverse transfer voltage ratio $\rightarrow h_{r}$
(iii) $h_{21} \rightarrow$ forward transfer current gain $\rightarrow h_{f}$
(iv) $h_{22} \rightarrow$ output admittance $\rightarrow h_{o}$

Figure 5-15 shows the complete hybrid equivalent circuit.


Figure 5-15 Complete hybrid equivalent model

(a)

(b)

Figure 5-16 Darlington pair: (a) basic circuit (b) darlington amplifier

## 5-6 EQUIVALENT CIRCUITS THROUGH HYBRID PARAMETERS AS A TWO-PORT NETWORK

For the transistor, even though it has three basic configurations, they are all four-terminal configurations, and thus, the resulting equivalent circuit will have the same format as shown in Figure 5-15. The $h$-parameter will however change with each configuration. To distinguish which parameter has been used or which is available, a second subscript has been added to the $h$-parameter notation.
(i) For the common-base configuration: the lower case letter $b$
(ii) For the common-emitter configuration: the lower case letter $e$
(iii) For the common-collector configuration: the lower case letter $c$

The hybrid equivalent network for the common-emitter and common-base is shown in Figure 5-16. For common-emitter $I_{i}=I_{b}, I_{o}=I_{c}$, and through an application of Kirchoff's current law we have:

$$
\begin{equation*}
I_{e}=I_{b}+I_{c} \tag{5-53}
\end{equation*}
$$

For the common-base configuration, $I_{i}=I_{e}, I_{o}=I_{c}$ with $V_{e b}=V_{i}$ and $V_{c b}=V_{o}$

## 5-7 DARLINGTON PAIR

The Darlington pair is achieved by connecting the collectors of the transistors where, the emitter of one transistor is connected to the base of the other transistor. Figure 5-16 gives the essence of the Darlington connection.

Input resistance of the second transistor is $\left(h_{i e}+h_{f e} R_{L}\right)$. This is the load resistance of the first stage. Overall current gain is the product of the current gains of the two transistors. As a result, the overall current gain is very high. This is the prime advantage of this type of connection. The effective input resistance of the Darlington connection is higher and the output value is lower. In digital circuits such as the "totem-pole" connection, often the diode following the emitter of a transistor at
the output stage can be replaced by an arrangement of a Darlington pair. This helps in increasing the current gain and also the input impedance-the two desired features.

## 5-8 TRANSISTOR AT HIGH FREQUENCIES

Till now we have considered the fact that the carriers responded at once to changes in the input signal. Also, we had neglected the junction capacitance of the transistor for simplicity. These were the approximations that we made for the transistor at low frequencies. But at higher frequencies these capacitances have profound effect and must be included in the analysis of the circuits. Also, at higher frequencies, the time delay between the emitter and the collector currents introduced by the movement of the charges is important and has to be taken into account. The time delay that occurs causes a phase shift between the emitter and the collector currents. Further, the transit time is different in many cases which, in turn, increases such distortion.

At high frequencies a significant amount of current carriers injected into the base fail to reach the collector as the polarity of the input signal reverses by the time the carriers reach. Consequently, a number of carriers can get trapped in this process and take an enormously long time to reach and get cleared from the base region. As the carriers remain in the base region for such a long time, a considerable fraction of current is lost. The current gains of the transistors decrease. This puts an upper limit to the proper operation of the device and results in it behaving in an unexpected manner. Also, there is an increase in the noise which has to be well taken care of.

## 5-9 REAL-LIFE APPLICATIONS OF THE TRANSISTOR

Transistor circuits are the basic component of any convenient electronics circuit. They are widely used in the case of signal amplification, switching, microprocessor and microcontroller designing, etc. These are the most common applications of transistors that go a long way in building powerful microprocessors and other appliances. Microprocessors are the real brains of most electronic appliances around us and a vital role is played by their grey cells-the transistors. The full potential of these transistors is realized through the various appliances they revolutionized, from the simplest of digital watches to the most complex computer hardware.

The first devices that were invented as a direct result of the transistor were phone receivers and broadcasters. Without phones, phone lines would never have come into existence. This, in turn, would have rendered impossible the invention of the Internet or the e-mail or the fax. The lack of signal receivers in phones meant that there would have never been any cell phones that today play a large role in the working world. The ability of a transistor to act as a semiconductor or as an insulator helped solve many problems that inventors had to face while working with the various crystal elements.

Of all the military appliances, the handheld radio was probably the most frequently used when troops went out to the battlefield. It was necessary for them to remain in contact with their commanders, with the base and with the other members of their troop. The transistor was instrumental in the development of this radio. Because of its broadcasting and receiving qualities, the transistor was used in the same manner as it is now used in telephones. In the hi-tech world that we live in today, the global positioning system, better known as GPS, would not have existed were it not for the transistor. The GPS is used extensively in the military to track their naval and air forces, and provides assistance in air-traffic control. In addition to this, the GPS also assists in mapping better routes for the different
types of road transport. This technology is now also used in expensive luxury cars. Speaking of cars, car ignition would not have been possible were it not for the invention of the transistor. It's all well and good to build a car, but the most important thing is that it works, and to do that, you have to start it!

The world of computers is probably the largest and most expansive area that the invention of the transistor has graced. There are so many different sub-sections to this one, but we will name a few. A computer is basically made up of only transistors. Computers use small devices like microprocessors and integrated circuits. These hold millions of transistors, and in fact, an entry-level Intel chip (microprocessor) consists of about 10 million transistors, so you can just imagine how many there are in the entire computer. From graphics cards that run the latest games to 800 W speakers, anything that has a circuit has transistors.

Another huge form of entertainment is the radio. Hi-fi's, radios and car radios would definitely not be in existence were it not for the transistor. In fact, one of the first transistorized inventions-the fully transistorized radio-was released in 1954, just a year after the first transistor device-the hearing aid-was invented. We all realise how much the radio is used, and not just for entertainment. Undoubtedly this was an invention much needed for the progress of mankind.

The press, the most widely used media format, would also not be in existence, because the mechanical devices that are used today (computers, printing machines, etc.) would not have been invented. We would be getting a weekly or monthly newspaper telling us what happened two weeks earlier, and even this would not be possible due to the lack of machinery to print this. And finally, one of the most widely used tools today, the Internet, would not have existed for obvious reasons.

What all this tells you, and we are sure you are aware, is that without the invention of the transistor basically everything that contains a circuit would either not be in existence, or they would definitely not be as developed as they are today. Computers, probably the most important device used in the world today, would not be around and it could have been very detrimental to the development of our world. As you can see, behind every electronic device that we use is a tiny, microscopic semiconductor device-the transistor.

## POINTS TO REMEMBER

1. Biasing is the establishment of suitable dc values of different current and voltages of a transistor by connecting it to an external voltage source through suitable circuits.
2. Proper biasing renders a desired operating point in the operating region of the device; either in the active or in the saturation or in the cut-off region.
3. The selection of the $Q$-point depends on (a) the amplitude of the signal to be handled by the amplifier, (b) the load to which the amplifier is to work, (c) the available supply potentials, and (d) the allowable distortion in the signal.
4. The $Q$-point of the transistor should be stable irrespective of changes in temperature or transistor characteristics.
5. The operating point mainly shifts due to changes in temperature. The temperature depends on the $\beta, I_{C O}$ and $V . \beta$ increases with increase in temperature. $\left|V_{B E}\right|$ decreases about 7.5 mV per degree Celsius increase in temperature. $I_{C O}$, which is the reverse saturation current, doubles in value for every 10 degree Celsius increase in temperature.
6. Stability factor determines the stability of the collector current due to the changes in $\beta$, $I_{C O}$ and $V_{B E}$.
7. The $h$-parameter gives a two-port model of a transistor.
8. Gain decreases in the low-frequency region because of parasitic capacitances of the network and frequency dependence of the gain of the transistor.
9. Darlington pair is a special type of connection where the collectors of the
transistors are connected together and the emitter of one is connected to the base of the other.
10. Input resistance of Darlington pair circuit increases and the overall gain of the system is high.
11. Typical $h$-parameters of a transistor (at $I_{E}=1.3 \mathrm{~mA}$ ).

| Parameters | $\mathbf{C E}$ | $\mathbf{C C}$ | CB |
| :--- | :--- | :--- | :--- |
| $H_{11}=h_{i}$ | $1,100 \Omega$ | $1,100 \Omega$ | $21.6 \Omega$ |
| $H_{12}=h_{r}$ | $2.5 \times 10^{-4}$ | $\sim 1$ | $2.9 \times 10^{-4}$ |
| $H_{21}=h_{f}$ | 50 | -51 | -0.98 |
| $H_{22}=h_{o}$ | $24 \mu \mathrm{~A} / \mathrm{V}$ | $25 \mu \mathrm{~A} / \mathrm{V}$ | $0.49 \mu \mathrm{~A} / \mathrm{V}$ |
| $1 / h_{o}$ | $40 \mathrm{k} \Omega$ | $40 \mathrm{k} \Omega$ | $2.04 \mathrm{M} \Omega$ |

## IMPORTANT FORMULAE

1. The value of the stability factor when the variation is taken w.r.t $I_{C O}$ :

$$
S \equiv \frac{\delta I_{C}}{\delta I_{C O}}
$$

2. $S=(1+\beta) \frac{1+R_{b} / R_{e}}{1+\beta+R_{b} / R_{e}}$
3. For constant $\beta, V_{B E}$, and small $S$, we have:

$$
\frac{\Delta I_{c}}{I_{c}} \approx S \frac{\Delta I_{c o}}{I_{c}} \approx \frac{\Delta I_{c o}}{I_{c}}+\frac{R_{b}}{R_{e}} \frac{\Delta I_{c o}}{I_{c}} .
$$

4. $S^{\prime} \equiv \frac{\delta I_{c}}{\delta V_{B E}} \approx \frac{\Delta I_{c}}{\Delta V_{B E}}$
5. The collector current is given by:

$$
I_{c}=\frac{\beta\left(V+V^{\prime}-V_{B E}\right)}{R_{b}+R_{e}(1+\beta)}
$$

6. The variation of the collector current w.r.t $\beta$ is given by:

$$
I_{c}=\frac{\beta\left(V+V^{\prime}-V_{B E}\right)}{R_{b}+R_{e}(1+\beta)}
$$

7. By taking the total differential of $I_{C}=f\left(I_{C O}\right.$, $V_{B E}, \beta$ ), we obtain:

$$
\Delta I_{c}=\frac{\delta I_{c}}{\delta I_{c o}} \Delta I_{c o}+\frac{\delta I_{c}}{\delta V_{B E}} \Delta V_{B E}+\frac{\delta I_{c}}{\delta \beta} \Delta \beta
$$

8. The current gain of a transistor amplifier using $h$-parameters is given by:

$$
A_{I}=-\frac{I_{2}}{I_{1}}=-\frac{h_{f}}{1+h_{o} R_{L}}
$$

9. The voltage gain is given by:

$$
A_{V}=-\frac{h_{f} R_{L}}{h_{i}+\Delta h R_{L}}
$$

where, $\Delta h=h_{i} h_{o}-h_{f} h_{r}$

## OBJECTIVE QUESTIONS

1. For good stabilized biasing of the transistor of the CE amplifier of figure. We should have:
(a) $\frac{R_{E}}{R_{B}} \ll 1$
(b) $\frac{R_{E}}{R_{B}} \gg 1$
(c) $\frac{R_{E}^{B}}{R_{B}} \ll h_{r b}$
(d) $\frac{R_{E}^{B}}{R_{B}} \gg h_{r b}$
2. Current stability of a CC amplifier can be increased by:
(a) Reducing both emitter and base resistance
(b) Increasing both emitter and base resistance
(c) Reducing emitter resistance and increasing base resistance
(d) Increasing emitter resistance and decreasing base resistance
3. Which of the following statements are correct for basic transistor amplifier configuration?
(a) CB amplifier has low input impedance and a low current gain
(b) CC amplifier has low output impedance and a low current gain
(c) CE amplifier has very poor voltage gain but very high input impedance
(d) The current gain of CB amplifier is higher than the current gain OF CC amplifier
4. Which of the following configuration ifs normally used in cascading?
(a) Common-emitter configuration
(b) Common-base configuration
(c) Common-collector configuration
(d) None of the above
5. A transistor has $h_{f e}=27$, then its $h_{f e}$ will be:
(a) -0.96
(b) 0.96
(c) -27
(d) -28

## REVIEW QUESTIONS

1. What do you mean by the quiescent point of a transistor?
2. Draw the circuit diagram of a common emitter transistor amplifier and explain its operation graphically.
3. What do you mean by the term load line? Explain its significance.
4. What do you mean by distortion in amplifiers? Discuss the origin of the input and outputnonlinearities in transistor amplifiers. What is the desired position of the $Q$-point for minimum distortion and why?
5. Explain the term transistor biasing. What are the factors affecting the position of $Q$-points?
6. Is the operating point of the transistor fixed? If not, what are the factors responsible for its change or shift?
7. What are the factors responsible for affecting the bias stability of a transistor?
8. Define the stability factors with respect to the changes in $I_{C O}, V_{B E}$ and $\beta$.
9. Why is stability with respect to changes in $V_{C E}$ not considered?
10. What is thermal runaway?
11. Draw the circuit for fixed bias by considering an $n-p-n$ transistor in the CE mode. Derive the expressions for stability factors. What are the functions of the coupling capacitors?
12. Draw the circuit diagram for the collector to base arrangement for an $n-p-n$ transistor. Obtain the stability factors and mention the demerits of the circuit.
13. What is self bias? Draw the circuit showing self bias of an $n-p-n$ transistor in the CE
mode. Explain physically how the self bias improves stability.
14. What is bias curve? How is the $Q$-point in a self bias circuit determined with and without the help of bias curve?
15. Derive the expressions for stability factors in the case of self bias of a CE mode transistor.
16. How is the transistor represented as a twoport device?
17. Define the hybrid parameters for a basic transistor circuit in any configuration and give its hybrid model.
18. What is Darlington pair? Compare between Darlington pair and emitter follower.
19. Explain how the model of transistor changes in high frequency. What are the prime reasons for such a change?

## PRACTICE PROBLEMS

1. The transistor, as shown in the following diagram has a very high $\beta$.


Find $V_{E}$ and $V_{C}$ for $V_{B}$ equal to:
(a) 3 V
(b) 1 V
(c) 0 V
2. The transistor, as shown in Problem 1, has a very high $\beta$. Find the highest value of $V_{B}$ for which the transistor still operates in the active mode.
3. Consider the circuit, as shown in the following diagram with the base voltage $V_{B}$ obtained using a voltage divider across the 9 V supply.


Assuming that the transistor has a very high value of $\beta$, design the voltage divider to obtain $V_{B}=3 \mathrm{~V}$. Design for a 0.2 mA current in the voltage divider.
4. For the circuits, as shown in the following diagrams, find the values of the labeled node voltages and branch currents.

(a)

required to obtain $V_{C}=5 \mathrm{~V}$. What happens if the transistor is replaced with another having $\beta=100$ ?


## SUGGESTED READINGS

1. Grove, A. S. 1967. Physics and Technology of Semiconductor Devices. New York: Wiley.
2. Sze, S. M. 1981. Physics of Semiconductor Devices. New York: Wiley.
3. Singh, J. 1994. Semiconductor Devices: An Introduction. New York, NY: McGraw-Hill.
4. Streetman, B. G. and S. Banerjee. 2000. Solid State Electronic Devices. New Delhi: Pearson Education.
5. Millman, Jacob and Christos C. Halkias. 1986. Integrated Electronics: Analog and Digital Circuits and Systems. New Delhi: McGraw Hill Book Company.
6. Pierret, R. F. and G.W. Neudeck. 1989. Modular Series on Solid State Devices Boston, MA: Addison Wesley.
7. Singh, B. P. and Rekha Singh. 2006. Electronic Devices and Integrated Circuits. New Delhi: Pearson Education.

## 6

## Feedback Amplifier

## Outline

6-1 Introduction

## 6-2 Conceptual Development Through Block Diagrams

6-3 Properties of Negative Feedback
6-4 Calculations of Open-Loop Gain, ClosedLoop Gain and Feedback Factors
6-5 Topologies of the Feedback Amplifier

6-6 Effect of Feedback on Gain, Input and Output Impedances
6-7 Practical Implementation of the Feedback Topologies
6-8 Sensitivity
6-9 Bandwidth Stability
6-10 Effect of Positive Feedback

## Objectives

In this chapter we will address the concept of feedback. Feedback is the fundamental concept in the design of a stable amplifier and an unstable oscillator circuit. Beginning with the conceptual development of feedback through block diagrams, this chapter explains both negative and positive feedback, and their effects on different circuit parameters. Calculations of open-loop gain and closed-loop gain have been done in detail, followed by a discussion on the effects of feedback on gain, input and output impedances. An overview of the practical implementation of feedback topologies, and the sensitivity and bandwidth stability of the feedback amplifier has also been provided. The chapter ends with an examination of the effects of positive feedback with emphasis on the Nyquist and Barkhausen criteria.

## 6-1 INTRODUCTION

Feedback is one of the fundamental processes in electronics. It is defined as the process whereby a portion of the output signal is fed to the input signal in order to form a part of the system-output control. This action tends to make the system self-regulating. Feedback is used to make the operating point of a transistor insensitive to both manufacturing variations in $\beta$ as well as temperature.

The feedback system has many advantages especially in the control of impedance levels, bandwidth improvement, and in rendering the circuit performance relatively insensitive to manufacturing as well as to environmental changes. This is of principal importance in modern electronics because a controlled and precise circuit performance can be obtained without resorting to costly precision components.These are the advantages of negative or degenerative feedback in which the signal feedback from output to input is $180^{\circ}$ out of phase with the applied excitation. It increases bandwidth and input impedance, and lowers the output impedance.

There is another type of feedback called positive or regenerative feedback in which the overall gain of the amplifier is increased. Positive feedback is useful in oscillators and while establishing the two stable states of flip-flop.

## 6-2 CONCEPTUAL DEVELOPMENT THROUGH BLOCK DIAGRAMS

The block diagram of a basic feedback amplifier is shown in Figure 6-1. It consists of five basic elements. These are input and output signals, the measure of the output, comparison between input and the sampled feedback, which gives rise to four possible types of feedback circuits, and the processing of the compared signal by the basic amplifier.

## 6-2-1 Input Signal

The block in Figure 6-1 represents the signal to be amplified. The signal source is modeled either by a voltage source $V_{s}$ in series with a resistance $R_{s}$, or by a current source $I_{s}$ in parallel with a resistance $R_{s}$.

## 6-2-2 Output Signal

The output can either be the voltage across the load resistance or the current through it. It is the output signal that is desired to be independent of the load and insensitive to parameter variations in the basic amplifier.

## 6-2-3 Sampling Network

The function of the sampling network is to provide a measure of the output signal, i.e., a signal that is proportional to the output. Two sampling networks are shown in Figure 6-2. In Figure 6-2(a) the output voltage is sampled by connecting the output port to the feedback network in parallel with the load. This configuration is called shunt connection. In Figure 6-2(b) the output current is


Figure 6-1 Block diagram of a basic feedback amplifier


Figure 6-2 Feedback connections at the output of a basic amplifier (a) the measure of the output voltage (b) the measure of the output current
sampled and the output port of the feedback network is connected in series with the load. This is a series connection.

## 6-2-4 Comparison or Summing Network

The two very common networks used for the summing of input and feedback signals are displayed in Figure 6-3.

The circuit shown in Figure 6-3(a) is a series connection and it is used to compare the signal voltage $V_{s}$ and feedback signal $V_{f}$. The amplifier input signal $V_{i}$ is proportional to the voltage difference $V_{s}-V_{f}$ that results from the comparison. A differential amplifier is used for comparison as its output voltage is proportional to the difference between the signals at the two inputs. A shunt connection is shown in Figure 6-3(b) in which the source current $I_{s}$ and feedback current $I_{f}$ are compared. The amplifier input current $I_{i}$ is proportional to the difference $I_{s}-I_{f}$.


Figure 6-3 Feedback connections at the input of a basic amplifier (a) voltage summing (series comparison) (b) current summing (shunt comparison)

## 6-2-5 Basic Amplifier

The basic amplifier is one of the important parts of the feedback amplifier. The circuit amplifies the difference signal that results from comparison and this process is responsible for de-sensitivity and control of the output in a feedback system.

## 6-3 PROPERTIES OF NEGATIVE FEEDBACK

A comparative study of the advantages and disadvantages of negative feedback illustrates the basic properties of negative feedback. Negative feedback has the following advantages:
(i) Negative feedback increases the input impedance of the voltage amplifier.
(ii) The output impedance of the voltage amplifier can be further lowered by negative feedback.
(iii) The transfer gain $A_{f}$ of the amplifier with a feedback can be stabilized against the variations of $h$ or hybrid parameters of the transistors, or the parameters of the other active devices used in the amplifier.
(iv) Negative feedback increases the frequency response and the bandwidth of the amplifier.
(v) Negative feedback increases the linear range of operation of the amplifier.
(vi) Negative feedback causes reduction in noise.
(vii) Phase distortion is reduced.

However, the gain $A_{f}$ of the amplifier with negative feedback is lower compared to an amplifier without a feedback. This is the only disadvantage of a negative feedback system.

Negative feedback has a lot of advantages which nullify its disadvantages. Negative feedback is used in amplifiers with the objective of obtaining stability of operation. It is important to design amplifiers with negative feedback correctly because inaccuracy in design can cause undesired oscillation.

## 6-4 CALCULATIONS OF OPEN-LOOP GAIN, CLOSED-LOOP GAIN AND FEEDBACK FACTORS

The general block diagram of an ideal feedback amplifier indicating basic amplifier, feedback network, external load and corresponding signals is shown in Figure 6-4.


Figure 6-4 Block diagram of ideal feedback amplifier

Table 6-1 Signals and transfer ratios in feedback amplifiers
Feedback Topology

| Signals | Series-Shunt <br> (Voltage-Series) | Series-Series <br> (Current-Series) | Shunt-Series <br> (Current-Shunt) | Shunt-Shunt <br> (Voltage-Shunt) |
| :--- | :---: | :---: | :---: | :---: |
| $X_{o}$ | Voltage | Current | Current | Voltage |
| $X_{s}, X_{i}, X_{f}$ | Voltage | Voltage | Current | Current |
| Ratio or Gain |  |  |  |  |
| $A$ | $V_{o} / V_{i}$ | $I_{o} / V_{i}$ | $I_{o} / I_{i}$ | $V_{o} / I_{i}$ |
| $\beta$ | $V_{f} / V_{o}$ | $V_{f} / I_{o}$ | $I_{f} / I_{o}$ | $I_{f} / V_{o}$ |
| $A_{f}$ | $V_{o} / V_{s}$ | $I_{o} / V_{s}$ | $I_{o} / I_{s}$ | $V_{o} / I_{s}$ |

The ideal feedback amplifier can have any of the four configurations as listed in Table 6-1.
The input signal $X_{s}$, the output signal $X_{o}$, the feedback signal $X_{f}$ and the difference signal $X_{i}$ each represent either a voltage or a current. These signals and the transfer ratios $A$ and $\beta$ are summarized in Table 6-1 for different feedback topologies. The symbol indicated by the circle with the summation sign $\Sigma$ enclosed within (see Figure 6-4), represents the summing network whose output is the algebraic sum of inputs.

Thus, for a positive feedback, we get:

$$
\begin{equation*}
X_{i}=X_{s}+X_{f} \tag{6-1}
\end{equation*}
$$

The signal $X_{i}$, representing the output of the summing network is the amplifier input $X_{i}$. If the feedback signal $X_{f}$ is $180^{\circ}$ out of phase with the input $X_{s}$-as is true in negative feedback systems-then $X_{i}$ is a difference signal. Therefore, $X_{i}$ decreases as $\left|X_{f}\right|$ increases. The reverse transmission of the feedback network $\beta$ is defined by:

$$
\begin{equation*}
\beta=\frac{X_{f}}{X_{o}} \tag{6-2}
\end{equation*}
$$

The transfer function $\beta$ is a real number, but in general it is a function of frequency. The gain of the basic amplifier $A$ is defined as:

$$
\begin{equation*}
A=\frac{X_{o}}{X_{i}} \tag{6-3a}
\end{equation*}
$$

Now, from Equation (6-1), we get:

$$
X_{i}=X_{s}+X_{f}
$$

Substituting the value of $X_{f}$ from Equation (6-2) as $X_{f}=\beta X_{o}$ in Equation (6-1), we get:

$$
\begin{equation*}
X_{i}=X_{s}+X_{f}=X_{s}+\beta X_{o} \tag{6-3b}
\end{equation*}
$$

From Equation (6-3) we get:

$$
\begin{equation*}
X_{o}=A X_{i} \tag{6-3c}
\end{equation*}
$$

Substituting the value of $X_{i}$ from Equation (6-3a), we get:

$$
X_{o}=A X_{i}=A\left(X_{s}+\beta X_{o}\right)=A X_{s}+A \beta X_{o}
$$

6-6 | Basic Electronics
or,

$$
\begin{gather*}
X_{o}(1-A \beta)=A X_{s} \\
\frac{X_{o}}{X_{s}}=\frac{A}{1-A \beta} \tag{6-3d}
\end{gather*}
$$

The feedback gain $A_{f}$ is obtained from Equation (6-3c) as:

$$
\begin{equation*}
A_{f}=\frac{X_{o}}{X_{s}}=\frac{A}{1-A \beta} \tag{6-4a}
\end{equation*}
$$

The gain in Equation (6-3) represents the transfer function without feedback. If $\beta=0$; eliminating the feedback signal, no feedback exists and Equation (6-4) reduces to Equation (6-3). Frequently $A$ is referred to as the open-loop gain and is designated by $A_{O L}$. When $\beta \neq 0$, a feedback loop exists and $A_{F}$ is often called the closed-loop gain.

If $\left|A_{f}\right|<|A|$, the feedback is negative. If $\left|A_{f}\right|>|A|$, the feedback is positive. In case of a negative feedback, $|1-A \beta|>1$. The reason behind this being the Barkhausen criterion.

Similarly for negative feedback:

$$
X_{i}=X_{s}-X_{f}
$$

Calculating in the same manner as done for positive feedback, we can represent the feedback gain as:

$$
\begin{equation*}
A_{f}=\frac{A}{1+A \beta} \tag{6-4b}
\end{equation*}
$$

For negative feedback, $|1+A \beta|>1$. So, $A_{f}<A$, i.e., $A_{f}$ decreases. Therefore, the general equation of feedback can be written as:

$$
A_{f}=\frac{A}{1 \pm A \beta}
$$

## 6-4-1 Loop Gain or Return Ratio

The signal $\hat{X}_{i}$ in Figure 6-4 is multiplied by gain $A$ when passing through the amplifier and by $\beta$ in transmission through the feedback network. Such a path takes us from the amplifier input around the loop consisting of the amplifier and the feedback network. The product, $A \beta$, is called the loop gain or return ratio $T$. Equation (6-4) can be written in terms of $A_{O L}$ and $T$ as:

$$
\begin{equation*}
A_{F}=\frac{A}{1-A \beta}=\frac{A_{O L}}{1+T} \tag{6-5a}
\end{equation*}
$$

For negative feedback, $-A \beta=T>0$.
We can give a physical interpretation for the return ratio by considering the input signal $X_{s}=0$, and keeping the path between $X_{i}$ and $\hat{X}_{i}$ open. If a signal $\hat{X}_{i}$ is now applied to the amplifier input, then $X_{i}=X_{f}=A \beta$.

$$
\begin{equation*}
T=-A \beta=-\left.\frac{X_{i}}{\hat{X}_{i}}\right|_{X_{s}=0} \tag{6-5b}
\end{equation*}
$$

The return ratio is then the negative of the ratio of the feedback signal to the amplifier input. Often the quantity $F=1-A \beta=1+T$ is referred to as the return difference. If negative feedback is considered then both $F$ and $T$ are greater than zero.

## 6-5 TOPOLOGIES OF THE FEEDBACK AMPLIFIER

There are four basic amplifier types. Each of these is being approximated by the characteristics of an ideal controlled source. The four feedback topologies are as follows:

1. Series-shunt feedback
2. Series-series feedback
3. Shunt-series feedback
4. Shunt-shunt feedback

These designations correspond to the output- and input-port connections of the feedback network with the basic amplifier. For example, in the shunt-series amplifier, the input port of the feedback network is connected in series with the output port of the amplifier. An alternative nomenclature is based on the quantity sampled and input connection used. Thus, a current-shunt topology corresponds to the shunt-series connection. The alternative nomenclature used is as follows:

1. Voltage-series or series-shunt feedback
2. Current-series or series-series feedback
3. Current-shunt or shunt-series feedback
4. Voltage-shunt or shunt-shunt feedback

## 6-5-1 Voltage-Series or Series-Shunt Feedback

The configuration of voltage-series or series-shunt feedback circuit is illustrated in Figure 6-5.
The input voltage $V_{i}$ of the basic amplifier is the algebraic sum of input signal $V_{s}$ and the feedback signal $\beta V_{o}$, where $V_{o}$ is the output voltage.

## 6-5-2 Current-Series or Series-Series Feedback

The current-series or series-series feedback topology is illustrated in Figure 6-6.


Figure 6-5 Voltage amplifiers with voltage-series feedback


Figure 6-6 Transconductance amplifier with current-series feedback
As mentioned in Table 6-1, the transconductance feedback amplifier provides an output current $I_{o}$ which is proportional to the input voltage $V_{s}$. The feedback signal is the voltage $V_{f}$, which is added to $V_{s}$ at the input of the basic amplifier.

## 6-5-3 Current-Shunt or Shunt-Series Feedback

The current-shunt or shunt-series feedback amplifier, as shown in Figure 6-7, supplies an output current $I_{o}$ which is proportional to the input current $I_{i}$. This makes it a current amplifier.

The feedback signal is the current $I_{f}$. The input current of the basic amplifier is $I_{i}=I_{s}+I_{f}$ and the output current is $I_{o}=I_{L}$.

## 6-5-4 Voltage-Shunt or Shunt-Shunt Feedback

The voltage-shunt or shunt-shunt feedback amplifier is illustrated in Figure 6-8.
This provides an output voltage $V_{o}$ in proportion to the input current $I_{s}$. The input current $I_{i}$ of the basic amplifier is the algebraic sum of $I_{s}$ and the feedback current $I_{f}$.


Figure 6-7 Current amplifiers with current-shunt feedback


Figure 6-8 Trans resistance amplifier with voltage-shunt feedback

## 6-6 EFFECT OF FEEDBACK ON GAIN, INPUT AND OUTPUT IMPEDANCES

Feedback is applied with the objective of improving the performance of an amplifier. The operation of an amplifier is regulated by controlling the gain and impedance. The effect of feedback on gain and impedance for the different topologies-voltage-series, current-series, current-shunt, voltage-shunt-are discussed in the following sections.

## 6-6-1 Effect of Feedback on Input Impedance

## Voltage-series feedback

Figure 6-9 shows the equivalent Thevenin's model of the voltage-series amplifier of Figure 6-5. In this circuit $A_{v}$ represents open-circuit voltage gain taking $Z_{S}$ into account. From Figure 6-9 the input impedance with the feedback is:

$$
\begin{equation*}
Z_{i f}=\frac{V_{S}}{I_{i}} \tag{6-6}
\end{equation*}
$$



Figure 6-9 Voltage-series feedback circuit used to calculate input and output resistance
and,

$$
\begin{equation*}
V_{S}=I_{i} Z_{i}+V_{f}=I_{i} Z_{i}+\beta V_{o} \tag{6-7}
\end{equation*}
$$

Using voltage divider rule, we get:

$$
\begin{equation*}
V_{o}=\frac{A_{V} V_{i} Z_{L}}{Z_{o}+Z_{L}}=A_{V} I_{i} Z_{L} \tag{6-8}
\end{equation*}
$$

where,

$$
I_{i}=\frac{V_{i}}{Z_{o}+Z_{L}}
$$

Now,

$$
V_{o}=A_{V} I_{i} Z_{L}=A_{V} V_{i}
$$

or,

$$
A_{V}=\frac{V_{o}}{I_{i}}
$$

From Figure 6-9, the input impedance without feedback is:

Now,

$$
\begin{gather*}
Z_{i}=\frac{V_{i}}{I_{i}}  \tag{6-9}\\
Z_{i f}=\frac{V_{S}}{I_{i}}=\frac{V_{i}\left(1+A_{V} \beta\right)}{I_{i}}
\end{gather*}
$$

From Equations (6-6) and (6-7) we have:

$$
\begin{equation*}
Z_{i f}=\frac{V_{S}}{I_{i}}=Z_{i}\left(1+\beta A_{V}\right) \tag{6-10}
\end{equation*}
$$

Thus, the input impedance is increased.
Although $A_{v}$ represents the open-circuit voltage gain without feedback, Equation (6-6) indicates that $A_{V}$ is the voltage gain without feedback taking the load $Z_{L}$ into account.

## Current-series feedback

In a similar manner as for voltage series, for current series feedback as shown in Figure 6-6, we obtain:

$$
\begin{equation*}
Z_{i f}=Z_{i}\left(1+\beta Y_{M}\right) \tag{6-11a}
\end{equation*}
$$

where, $Y_{M}$ is the short-circuit transadmittance without feedback considering the load impedance, and is given by:

$$
\begin{equation*}
Y_{M}=\frac{I_{o}}{V_{i}}=\frac{Y_{m} Z_{o}}{Z_{o}+Z_{L}} \tag{6-11b}
\end{equation*}
$$

where, $Y_{m}$ is the short-circuit transadmittance without feedback.
From Equation (6-11a) it is clear that for series mixing $Z_{i f}>Z_{i}$.

## Current-shunt feedback

Figure 6-10 shows the current-shunt feedback in which the amplifier is replaced by its Norton equivalent circuit. If $A_{i}$ is the short-circuit current gain then from Figure 6-10:


Figure 6-10 Current-shunt feedback circuit used to calculate input and output resistance
and,

$$
\begin{equation*}
I_{s}=I_{i}+I_{f}=I_{i}+\beta I_{0} \tag{6-12}
\end{equation*}
$$

where,

$$
\begin{equation*}
I_{o}=\frac{A_{i} I_{i}}{Z_{o}+Z_{L}}=A_{I} I_{i} \tag{6-13}
\end{equation*}
$$

$$
\begin{equation*}
A_{i}=\frac{I_{o}}{I_{i}}=\frac{A_{i} Z_{o}}{Z_{o}+Z_{L}} \tag{6-14}
\end{equation*}
$$

From Figure 6-10:

$$
\begin{gather*}
I_{S}=I_{i}\left(1+\beta A_{I}\right)  \tag{6-15}\\
Z_{i f}=\frac{V_{i}}{I_{S}} \quad \text { and } \quad Z_{i}=\frac{V_{i}}{I_{i}}
\end{gather*}
$$

Using Equation (6-15) we obtain:

$$
\begin{equation*}
Z_{i f}=\frac{V_{i}}{I_{i}\left(1+\beta A_{I}\right)}=\frac{Z_{i}}{1+\beta A_{I}} \tag{6-16}
\end{equation*}
$$

where, $A_{i}$ represents the short-circuit current gain.

## Voltage-shunt feedback

For voltage-shunt feedback, proceeding in a similar way as we have done in the previous sections, we obtain:

$$
\begin{equation*}
Z_{i f}=\frac{Z_{i}}{1+\beta Z_{M}} \tag{6-17a}
\end{equation*}
$$

where, $Z_{M}$ is the transimpedance without feedback considering the load, and is given by:

$$
\begin{equation*}
Z_{M}=\frac{V_{o}}{I_{i}}=\frac{Z_{m} Z_{L}}{Z_{o}+Z_{L}} \tag{6-17b}
\end{equation*}
$$

where, $Z_{m}$ is the open-circuit transimpedance without feedback.
From Equation (6-17 b) it is clear that for shunt comparison $Z_{i f}<Z_{i}$.

## 6-6-2 Effect of Feedback on Output Impedance

## Voltage-series feedback

To find the output resistance with feedback $Z_{\text {of }}$-looking into output terminals with $Z_{L}$ discon-nected-external signals must be removed $\left(V_{s}=0\right.$ or $\left.I_{s}=0\right)$. Let $Z_{L}=\infty$ impress a voltage $V$ across the output terminals which delivers current $I$.

Therefore:

$$
\begin{equation*}
Z_{o f}=\frac{V}{L} \tag{6-18}
\end{equation*}
$$

Replacing $V_{0}$ by $V$ in Figure 6-10 we get:

$$
\begin{equation*}
I=\frac{V-A_{V} V_{i}}{Z_{o}}=\frac{V+\beta A_{V} V}{Z_{o}} \tag{6-19}
\end{equation*}
$$

with,

$$
V_{s}=0, V_{i}=-V_{f}=-\beta V
$$

Hence:

$$
\begin{equation*}
Z_{o f}=\frac{V}{I}=\frac{Z_{o}}{1+\beta A_{V}} \tag{6-20}
\end{equation*}
$$

The output resistance with feedback $Z_{o f}^{\prime}$, which includes $Z_{L}$, is given by $Z_{o f}$ in parallel with $Z_{L}$. So:

$$
\begin{align*}
Z_{o f}^{\prime}= & \frac{Z_{o f} Z_{L}}{Z_{o f}+Z_{L}}=\frac{Z_{o} Z_{L}}{1+\beta A_{V}} \frac{1}{Z_{o} \mid\left(1+\beta A_{V}\right)+Z_{L}} \\
& =\frac{Z_{o} Z_{L}}{Z_{o}+Z_{L}+\beta A_{V} Z_{L}}=\frac{Z_{o} Z_{L} / Z_{o}+Z_{L}}{1+\beta A_{V} Z_{L} /\left(Z_{o}+Z_{L}\right)} \tag{6-21}
\end{align*}
$$

It should be noted that $Z_{o}^{\prime}=Z_{0} \| Z_{L}$ is the output resistance without feedback.
Using Equation (6-9) in Equation (6-21) we obtain:

$$
\begin{equation*}
Z_{o f}^{\prime}=\frac{\mathrm{Z}_{o}^{\prime}}{1+\beta A_{V}} \tag{6-22}
\end{equation*}
$$

## Voltage-shunt feedback

Proceeding in the similar manner, we have:

$$
\begin{equation*}
Z_{o f}=\frac{Z_{o}}{1+\beta Z_{m}} \tag{6-23}
\end{equation*}
$$

and,

$$
\begin{equation*}
Z_{f}^{\prime}=\frac{Z_{0}^{\prime}}{1+\beta Z_{M}} \tag{6-24}
\end{equation*}
$$

For voltage sampling it is clear that $Z_{o f}<Z_{o}$.

## Current-shunt feedback

In Figure 6-10, replacing $V_{0}$ by $V$, we have:

$$
\begin{equation*}
I=\frac{V}{Z_{o}}-A_{i} I_{i} \tag{6-25}
\end{equation*}
$$

with,

$$
I_{s}=0, I_{i}=-I_{f}=-\beta I_{0}=\beta I
$$

hence,

$$
\begin{align*}
& I\left(1+\beta A_{i}\right)=\frac{V}{Z_{o}}  \tag{6-26}\\
& \quad Z_{o f}=\frac{V}{I}=Z_{o}\left(1+\beta A_{i}\right) \tag{6-27}
\end{align*}
$$

Equation (6-27) is the expression for the output impedance with feedback, and without load resistance $R_{L}$. To find $R^{\prime}{ }_{o f}$ :

$$
\begin{align*}
Z_{o f}^{\prime}= & \frac{Z_{o f} Z_{L}}{Z_{o f}+Z_{L}}=\frac{Z_{o}\left(1+\beta A_{i}\right) Z_{L}}{Z_{o}\left(1+\beta A_{i}\right)+Z_{L}} \\
& =\frac{Z_{o} Z_{L}}{Z_{o}+Z_{L}} \frac{1+\beta A_{i}}{1+\beta A_{i} Z_{o}^{l}\left(Z_{o}+Z_{L}\right)} \tag{6-28}
\end{align*}
$$

Using Equation (6-27), and with $Z^{\prime}{ }_{o}=Z_{o} \| Z_{L}$, we have:

$$
\begin{equation*}
Z_{o f}^{\prime}=Z_{o}^{\prime} \frac{1+\beta A_{i}}{1+\beta A_{i}} \tag{6-29}
\end{equation*}
$$

## Current-series feedback

Proceeding in the similar manner we have:
and,

$$
\begin{align*}
& Z_{o f}=Z_{o}\left(1+\beta Y_{m}\right)  \tag{6-30a}\\
& Z_{o f}^{\prime}=Z_{o}^{\prime} \frac{1+\beta Y_{m}}{1+\beta Y_{m}} \tag{6-30b}
\end{align*}
$$

From Equations (6-30a) and (6-30b) we see that for current sampling $Z_{\text {of }}>Z_{0}$.

## 6-7 PRACTICAL IMPLEMENTATIONS OF THE FEEDBACK TOPOLOGIES

The feedback topologies discussed so far have a variety of practical implementations. We will now proceed to discuss the applications of these different topologies with examples of transistors with different configurations.


Figure 6-11 Voltage-series feedback circuit

## 6-7-1 Voltage-Series Feedback Using Transistor

The emitter-follower circuit, as shown in Figure 6-11, is an example of voltage-series feedback.

The feedback signal $V_{f}$ and the output signal $V_{o}$ are both voltage quantities. According to Table 6-1, this is a voltage-series feedback circuit. To determine the gain of the basic amplifier without feedback we should consider $V_{o}=0$ for the input loop and $I_{b}=0$ for the output loop so that we obtain the approximate hybrid equivalent circuit, as given in Figure 6-12.

$$
\begin{equation*}
A_{v}=\frac{V_{o}}{V_{s}}=\frac{h_{f e} I_{b} Z_{e}}{V_{s}}=\frac{h_{f e} Z_{e}}{h_{i e}} \tag{6-31a}
\end{equation*}
$$

and, $\quad \beta=\frac{V_{f}}{V_{o}}=1$
Using Equations (6-9), (6-10), and (6-22) we can calculate $A_{V}, Z_{i f}$, and $Z_{f}^{\prime}$.

## 6-7-2 Current-Series Feedback Using Transistor

An example of current-series feedback is given in Figure 6-13.
In the circuit shown in Figure 6-13, the output signal is the load current $I_{o}$ and the feedback signal is the voltage $V_{f}$ across $R_{e}$. Referring to Table 6-1 it can be concluded that this is a currentseries feedback circuit. To obtain the transadmittance of the basic amplifier we consider $V_{f}=0$. The approximate $h$-parameter equivalent is illustrated in Figure 6-14.

According to Figure 6-14, the transfer gain of the basic amplifier is:

$$
\begin{equation*}
Y_{m}=\frac{I_{o}}{V_{s}}=\frac{-I_{b} h_{f e}}{I_{b}\left(h_{i e}+R_{e}\right)}=\frac{-h_{f e}}{h_{i e}+R_{e}} \tag{6-31c}
\end{equation*}
$$

and,

$$
\begin{equation*}
\beta=\frac{V_{f}}{I_{o}}=\frac{-I_{o} R_{e}}{I_{o}} \tag{6-32d}
\end{equation*}
$$



Figure 6-12 Approximate hybrid equivalent circuit of practical voltage-series feedback amplifier


Figure 6-13 Current-series feedback circuit using transistor


Figure 6-14 Simplified h-parameter circuit of the current-series feedback amplifier

Hence, from Equations (6-11a), (6-11b) and (6-31) the expressions of $Y_{M}, Z_{i f}$ and $Z^{\prime}{ }_{\text {of }}$ can be obtained.

## 6-7-3 Voltage-Shunt Feedback Using Transistor

The circuit diagram of a voltage-shunt feedback topology is given in Figure 6-15.

In the circuit given in Figure 6-15, the input current is proportional to the output voltage $V_{o}$. To determine the gain of the basic amplifier we consider that $R_{f}$ is open-circuited and we can draw the approximate $h$-parameter equivalent circuit as shown in Figure 6-16.

From Figure 6-16 we can write:

$$
I_{b}=I_{s} \times \frac{R_{s}}{R_{s}+h_{i e}}
$$

or, $\quad \frac{I_{b}}{I_{s}}=\frac{R_{s}}{R_{s}+h_{i e}}$


Figure 6-15 Implementation of voltage-shunt feedback

The gain of the amplifier is given by:


Figure 6-16 Approximate $h$-parameter equivalent circuit for voltage-shunt feedback circuit

$$
\begin{equation*}
Z_{m}=\frac{V_{o}}{I_{s}}=\frac{-h_{f e} I_{b} R_{c}}{I_{s}}=\frac{-h_{f e} R_{c} R_{s}}{R_{s}+h_{i e}} \tag{6-31e}
\end{equation*}
$$

Considering the resistance $R_{f}$ in Figure 6-16 we obtain:

$$
\begin{equation*}
I_{f}=\frac{h_{f e} I_{b} R_{c}}{h_{i e}+R_{c}+R_{f}} \tag{6-31f}
\end{equation*}
$$

From Equation (6-31f)

$$
\begin{gather*}
\beta=\frac{I_{f}}{V_{o}} \\
\beta=\frac{h_{f e} I_{b} R_{c}}{h_{i e}+R_{c}+R_{f}} \times \frac{-1}{h_{f e} I_{b} R_{c}}=\frac{-1}{h_{i e}+R_{c}+R_{f}} \tag{6-31~g}
\end{gather*}
$$

From Equations (6-31e) and (6-31g), and using Equations 6-17(a), 6-17(b) and 6-24, we can obtain $Z_{M}, Z_{i f}, Z_{o f}^{\prime}$.

## 6-7-4 Current-Shunt Feedback Using Transistor

A simple current-shunt feedback amplifier is shown in Figure 6-17.
Without feedback $I_{s}=I_{e}$, we can draw the approximate $h$-parameter circuit as shown in Figure 6-18.


Figure 6-17 Current-shunt feedback circuit

From Figure 6-18 we have:

$$
\begin{align*}
& I_{s}=-\left(h_{f e}+1\right) I_{b}  \tag{6-31h}\\
& \text { and } \\
& I_{o}=-h_{f e} i_{b} \tag{6-31i}
\end{align*}
$$

Substituting the values of $I_{s}$ and $I_{o}$ from Equations (6-31h) and (6-31i) in Equation 6-14, we get:


Figure 6-18 Approximate $h$-parameter circuit of current-shunt feedback circuit

$$
\begin{equation*}
A_{I}=\frac{I_{o}}{I_{s}}=\frac{h_{f e}}{1+h_{f e}}=\frac{A_{i} Z_{0}}{Z_{0}+Z_{L}} \tag{6-31j}
\end{equation*}
$$

Hence, we can write $A_{i}=h_{f e}$ and $\beta=1$. The values of $Z_{i f}$ and $Z^{\prime}{ }_{i f}$ can be determined from Equations (6-16) and (6-29) using the value of $A_{i}$ and $\beta$.

## 6-8 SENSITIVITY

The sensitivity of transfer gain of the feedback amplifier $A_{F}$ with respect to the variations in the internal amplifier gain $A$ is defined as the ratio of the fractional change in gain with the feedback to the fractional change in gain without the feedback. The gain sensitivity $S$ of the feedback amplifier is given by:

$$
\begin{equation*}
S=\frac{\frac{d A_{f}}{A_{f}}}{\frac{d A}{A}} \tag{6-32}
\end{equation*}
$$

where, $d A_{f} / A_{f}=$ fractional change in gain with the feedback; $d A / A=$ fractional change in gain without the feedback.

From Equation (6-4a) we have:

$$
A_{f}=\frac{A}{1+A \beta}
$$

Differentiating with respect to $A$ :

$$
\frac{d A_{f}}{A_{f}}=\frac{1}{1+A \beta} \frac{d A}{A}
$$

$$
\begin{equation*}
\therefore \quad S=\frac{\frac{d A_{f}}{A_{f}}}{\frac{d A}{A}}=\frac{1}{1+A \beta} \tag{6-33}
\end{equation*}
$$

From Equation (6-33), we can say that $1 / 1+A \beta$ is the sensitivity. The inverse or reciprocal of sensitivity is called de-sensitivity.

$$
\begin{equation*}
S=\frac{1}{1+A \beta}=\frac{1}{D} \tag{6-34}
\end{equation*}
$$

Again from Equation (6-4) we have:

$$
\begin{align*}
& A_{f}=\frac{A}{1+A \beta}=\frac{A}{D}  \tag{6-35}\\
& D=\frac{A}{A_{f}} \tag{6-36}
\end{align*}
$$

Equation (6-36) shows that de-sensitivity $(D)$ indicates the fraction by which the voltage gain has been reduced due to feedback.

## 6-9 BANDWIDTH STABILITY

The transfer gain of an amplifier having the feedback is given by:

$$
A_{f}=\frac{A}{1+\beta A}
$$

If $|\beta A| \gg 1$, then:

$$
\begin{equation*}
A_{f} \approx \frac{A}{\beta A}=\frac{1}{\beta} \tag{6-37}
\end{equation*}
$$

From Equation (6-37) we can directly conclude that the transfer gain can be made dependent entirely on the feedback network $\beta$. However, it is important to consider that while $\beta$ is a constant term, the gain $A$ is not constant and depends on the frequency. This means that at certain high or low frequencies $|\beta A|$ will be much larger than unity. To study the dependence we will consider the singlepole transfer function. The gain $A$ of single-pole transfer function is given by:

$$
\begin{equation*}
A=\frac{A_{0}}{1+j\left(f / f_{H}\right)} \tag{6-38}
\end{equation*}
$$

$A_{0}$ is the mid-band gain without the feedback and $f_{H}$ is the high frequency (where $A_{0}$ is decreased by 3 dB ). The gain $A$ of the single pole amplifier with the feedback is obtained from Equations (6-4) and (6-38) as:

$$
\begin{equation*}
A_{f}=\frac{A_{0} /\left[1+j\left(f / f_{H}\right)\right]}{1+\beta A_{0} /\left[1+j\left(f / f_{H}\right)\right]}=\frac{A_{0}}{1+\beta A_{0}+j\left(f / f_{H}\right)} \tag{6-39}
\end{equation*}
$$

By dividing the numerator and denominator by $1+\beta A_{0}$, Equation (6-39) can be written as:

$$
\begin{equation*}
A_{f}=\frac{A_{0 f}}{1+j\left(f l f_{H f}\right)} \tag{6-40}
\end{equation*}
$$

where,

$$
\begin{equation*}
A_{0 f} \equiv \frac{A_{0}}{1+\beta A_{0}} \tag{6-41}
\end{equation*}
$$

$$
\begin{equation*}
f_{H f} \equiv f_{H}\left(1+\beta A_{0}\right) \tag{6-42}
\end{equation*}
$$

It should be noted that $A_{0 f}$ is the mid-band gain with the feedback, and $f_{H f}$ is the high 3 dB frequency with the feedback.
From Equation (6-41), we have:

$$
\begin{equation*}
A_{0 f} f_{H f}=A_{0} f_{H} \tag{6-43}
\end{equation*}
$$

Similarly, it can be shown that the low 3 dB frequency with the feedback is given by:

$$
\begin{equation*}
f_{L f}=\frac{f_{L}}{1+\beta A_{0}} \tag{6-44}
\end{equation*}
$$

where, $f_{L}$ is the low 3 dB frequency without the feedback.


Figure 6-19 (a) Transfer gain is decreased and bandwidth is increased for an amplifier using negative feedback. (b) Idealized bode plot

For an video amplifier $f_{H} \gg f_{L}$; therefore, the bandwidth is $f_{H}-f_{L} \approx f_{H}$. Under these circumstances, Equation (6-43) may be interpreted to mean that the gain bandwidth product is constant with or without the feedback.

Also, from Equations (6-41) and (6-44) it is evident that the bandwidth has improved a lot. This can be shown by plotting the frequency versus gain in the logarithmic scale, as shown in Figure 6-19.

## 6-10 EFFECT OF POSITIVE FEEDBACK

If $|1+\beta A|>1$, it is considered to be negative feedback, and if $|1+\beta A|<1$, it is considered to be positive feedback. In second case, the resultant transfer gain $A_{f}$ will be greater than $A$-the nominal
gain without feedback-since $\left|A_{f}\right|=|A| /|1+\beta A|>|A|$. Positive feedback increases the amplification but at the cost of reduced stability.

To illustrate the instability in an amplifier with positive feedback, we will consider the following situation. No signal is applied, but because of some transient disturbance a signal $X_{0}$ appears at the output terminals. A portion of this signal $-\beta X_{0}$ will be the feedback to the input circuit, and will appear in the output as an increased signal $-A \beta X_{0}$. If this term just equals $X_{0}$, then the spurious output has regenerated itself. In other words, if $-A \beta X_{0}=X_{0} \Rightarrow-A \beta=1$, the amplifier will oscillate. If an attempt is made to obtain a large gain by making $|\beta A|$ almost equal to unity, there is a possibility that the amplifier may break into spontaneous oscillation. This situation may be created by the processes like variation in supply voltages, ageing of transistors, etc.

## 6-10-1 Instability and Oscillation

If an amplifier is designed to have negative feedback in a particular frequency range but breaks into oscillation at some high or low frequency, it is useless as an amplifier. While designing the amplifier, it must be ensured that the circuit is stable at all frequencies and not merely over the frequency range of interest.

The stability of a circuit lies in the pole of the transfer function of the circuit, which also determines the transient response of the circuit. A pole existing with a positive real part will result in a signal disturbance increasing with time. So the condition to be satisfied, if a system is to be stable, is that the poles of the transfer function must all lie in the left-hand half of the complex-frequency plane.

## 6-10-2 Nyquist Criterion

Harry Nyquist obtained a condition for stability, which may be expressed in terms of the steadystate or frequency-response characteristics. The loop gain factor $A \beta$ is a complex number; it may be represented as a point in the complex plane, the real component being plotted along the $x$-axis


Figure 6-20 The locus of $|1+A \beta|=1$ is a circle of unit radius with centre at $-1+j 0$ (when the vector $A \beta$ ends in the shaded region, the feedback is positive) and the $j$ component along $y$-axis. Also $A \beta$ is the function of the frequency. Consequently, points in the complex plane are obtained for the values of $A \beta$ corresponding to all values of $f$ from $-\infty$ to $+\infty$. The locus of all such points forms a closed curve. The Nyquist criterion states that the amplifier is unstable if this curve encloses $-1+j 0$, and the amplifier is stable if the curve does not enclose this point.

The criterion for positive or negative feedback is represented in the complex plane. Figure 6-20 shows that $|1+A \beta|=1$ represents a circle with radius equal to unity and centre at the point $-1+j 0$. For any frequency, $A \beta$ extends outside this circle and the feedback is negative; therefore $|1+A \beta|>1$. If the feedback is positive and the $A \beta$ value falls within the circle, then $|1+A \beta|<1$. Also, when the feedback is positive the system will not oscillate unless the Nyquist criterion is satisfied.


Figure 6-21 An amplifier with feedback gain $A$ and feedback network $\beta$ not yet connected to the network

## 6-10-3 Condition of Oscillation

To investigate the oscillation of the circuit consider Figure 6-21. It shows an amplifier, a feedback network and an input mixing circuit not connected to form a closed loop. The amplifier provides an output signal $x_{0}$ as a consequence of the signal $x_{i}$ applied directly to the amplifier input terminal. The output of feedback network is $x_{f}=\beta x_{0}=A \beta x_{i}$ and the output of the mixing circuit is:

$$
x_{f}^{\prime}=-x_{f}=-A \beta x_{i}
$$

From Figure 6-21, loop gain can be written as:

$$
\begin{equation*}
\frac{x_{f}^{\prime}}{x_{i}}=\frac{-x_{f}}{x_{i}}=-A \beta \tag{6-45}
\end{equation*}
$$

Suppose that the signal $x_{f}^{\prime}$ is adjusted such that it equals the externally applied signal $x_{i}$. Since the amplifier has no means of distinguishing the source of the input signal applied to it, it would appear that if the external source were removed and if terminal 2 were connected to terminal 1 the amplifier would continue to provide the same output signal $x_{0}$ as before.

The statement, $x_{f}^{\prime}=-x_{i}$, means that the instantaneous values of $x_{f}^{\prime}$ and $x_{i}$ are exactly equal at all times. The condition $x^{\prime}{ }_{f}=x_{i}$ is equivalent to $-A \beta=1$ or, the loop gain must be unity. This is the condition of oscillation.

## 6-10-4 Barkhausen Criterion

Let us consider that the entire circuit operates linearly and that the feedback or the amplifier network or both contain reactive elements. In such a case the only periodic waveform which will maintain its form is the sinusoidal waveform.

For a sinusoidal waveform the condition $x_{i}=x_{f}^{\prime}$ is equivalent to the condition that the amplitude, phase and frequency of $x_{i}$ and $x_{f}^{\prime}$ are identical. As the phase shift is introduced, any signal that is transmitted through a reactive network is always a function of the frequency. Hence we have the following important principle:

The frequency at which a sinusoidal oscillator will operate is the frequency for which the total shift introduced, as a signal proceeds from the input terminals, through the amplifier and feedbacknetwork, andbackagaintotheinput, ispreciselyzerooranintegralmultipleof $2 \pi$.Statedmoresimply, the frequency of a sinusoidal oscillator is determined by the condition that the loop gain phase shift is zero.

It might be noted parenthetically that it is not inconceivable that this condition might be satisfied for more than a single frequency. In such a contingency there is a possibility of simultaneous oscillations at several frequencies or an oscillation at one of the allowed frequencies.

The condition given here determines the frequency, provided that the circuit will oscillate at all. Another condition, which must clearly be met, is that the magnitude of $x_{i}$ and $x_{f}^{\prime}$ must be identical. This condition is then embodied in the following principle:

Oscillations will not be sustained if, at the oscillator frequency, the magnitude of the product of the transfer gain of the amplifier and the magnitude of the feedback factor of the feedback network (the magnitude of the loop gain) are less than unity.

The condition of unity loop gain $A \beta=1$ is called the Barkhausen criterion. This condition implies, of course, that $|A \beta|=1$, and that the phase of $-A \beta$ is zero. The two principles stated previously are consistent with the feedback formula $A_{f}=A /(1+\beta A)$. If $-\beta A=1$ then $A_{f} \rightarrow \infty$, which may be interpreted to mean that there exists an output voltage even in the absence of an externally applied signal voltage. Therefore, the conditions for Barkhausen criteria for oscillation are as follows:

1. Positive feedback
2. Loop gain is unity, $A \beta=1$; therefore, the feedback gain is infinite, $A_{f}=\infty$
3. Phase variation is zero or integral multiple of $360^{\circ}$

## Solved Examples

Example 6-1 An amplifier has an open-loop gain of 500 and a feedback of 0.1. If open-loop gain changes by $20 \%$ due to the temperature find the percentage change in the closed-loop gain.

## Solution:

Given: $A=500, \beta=0.1, \frac{d A}{A}=20$.
Change in closed-loop gain:

$$
\begin{aligned}
\frac{d A_{f}}{A_{f}} & =\frac{d A}{A} \times \frac{1}{1+\beta A} \\
& =20 \times \frac{1}{1+500 \times 0.1} \\
& =0.3921=39.21 \%
\end{aligned}
$$

Example 6-2 An amplifier has a voltage gain of 200. This gain is reduced to 50 when negative feedback is applied. Determine the reverse transmission factor and express the amount of feedback in dB .

## Solution:

Given: $A=200, A_{f}=50$.
We know that:

$$
A_{f}=\frac{A}{1+\beta A}
$$

$$
\begin{array}{ll}
\Rightarrow & 50=\frac{200}{1+\beta \times 200} \\
\therefore & \beta=0.015
\end{array}
$$

Feedback in dB:

$$
\begin{aligned}
N=20 \log _{10}\left|\frac{A_{f}}{A}\right| & =20 \log _{10}\left(\frac{50}{200}\right)=20 \log _{10}\left(\frac{1}{4}\right) \\
& =-12.042 \mathrm{~dB}
\end{aligned}
$$

Example 6-3 An amplifier has a voltage gain of 100. The feedback ratio is 0.05 . Find:
(a) The voltage gain with feedback in dB
(b) Feedback factor
(c) The output voltage, if input voltage is 1 volt
(d) The feedback voltage

## Solution:

(a) Voltage gain is $A_{f}=\frac{A}{1+\beta A}=\frac{100}{1+100 \times 0.05}=\frac{100}{6}=16.67 \mathrm{~dB}$

$$
F=20 \log _{10}\left|\frac{A_{f}}{A}\right|=20 \log _{10}\left|\frac{1}{6}\right|=-15.56 \mathrm{~dB}
$$

(b) $A \beta=100 \times 0.05=5$
(c) $V_{o}=A_{f} V_{i}=100 \times 0.05=5$
(d) $V_{f}=\beta V_{0}=0.05 \times 5=0.25$ Volt

Example 6-4 For the circuit shown in the diagram, $R_{c}=4 \mathrm{k} \Omega, R_{L}=4 \mathrm{k} \Omega, R_{B}=20 \mathrm{k} \Omega, R_{s}=1 \mathrm{k} \Omega$ and the transistor parameters are:

$$
h_{i e}=1 \mathrm{k} \Omega, h_{f e}=50, \quad h_{r e}=2.5 \times 10^{-4} \quad \text { and } \quad h_{o e}=24 \mu \mathrm{~S}
$$

Find:
(a) The current gain
(b) The voltage gain
(c) The transconductance
(d) The transresistance
(e) The input resistance seen by the source
(f) The output resistance seen by the load. Neglect all capacitive effects.


## Solution:

Given:

$$
R_{c}=4 \mathrm{k} \Omega, R_{L}=4 \mathrm{k} \Omega, R_{B}=20 \mathrm{k} \Omega, R_{s}=1 \mathrm{k} \Omega
$$

The ac equivalent of the circuit is shown in the following figure:
(a) Current gain: $A_{I}=\frac{I_{L}}{I_{s}}=\frac{I_{i}}{I_{s}} \frac{I_{b}}{I_{i}} \frac{I_{L}}{I_{b}}$

$$
\frac{I_{i}}{I_{s}}=\frac{R_{s}}{R_{s}+R_{i}}
$$

Input resistance:

$$
\begin{aligned}
& R_{i}=R_{b}\left\|h_{i e}=20 \mathrm{k}\right\| 1.1 \mathrm{k} \\
& \quad=\frac{20 \times 1.1}{20+1.1}=1.04 \mathrm{k} \Omega
\end{aligned}
$$



Then:

$$
\begin{aligned}
\frac{I_{i}}{I_{s}} & =\frac{1 \mathrm{k}}{1 \mathrm{k}+1.04 \mathrm{k}}=\frac{1}{2.04} \\
\frac{I_{b}}{I_{i}} & =\frac{R_{B}}{R_{B}+h_{i e}} \\
& =\frac{20}{20+1.1}=0.95 \\
\frac{I_{L}}{I_{b}} & =-h_{f e} \frac{R_{c}}{R_{c}+R_{L}} \\
& =-50 \times \frac{4}{4+4}=-25 \\
A_{I} & =\frac{I_{L}}{I_{s}}=\frac{1}{2.04} \times 0.95 \times(-25) \\
& =-11.65
\end{aligned}
$$

(b) Voltage gain:

$$
\begin{aligned}
A_{V} & =\frac{V_{0}}{V_{s}}=\frac{I_{L} R_{L}}{I_{s} R_{s}} \\
& =(-11.65) \times \frac{4 \mathrm{k}}{1 \mathrm{k}}=-46.6
\end{aligned}
$$

(c) Transconductance:

$$
\begin{aligned}
G_{m} & =\frac{I_{L}}{V_{s}}=\frac{V_{0}}{R_{L}} \frac{1}{V_{s}}=\frac{V_{0}}{V_{s}} \frac{1}{R_{L}} \\
& =\frac{-46.6}{4 k}=-11.65 \mathrm{~mA} / \mathrm{V}
\end{aligned}
$$

(d) Transresistance:

$$
\begin{aligned}
R_{m} & =\frac{V_{0}}{I_{s}}=\frac{R_{s}}{V_{s}} V_{0}=\frac{V_{0}}{V_{\mathrm{s}}} R_{s} \\
& =1 \mathrm{k} \times(-46.6)=-46.6 \mathrm{k} \Omega
\end{aligned}
$$

(e) Input resistance: $R_{i}=1.04 \mathrm{k} \Omega$
(f) Output resistance:

$$
R_{0}=R_{c}\left\|\frac{i}{h_{o e}}=4 \mathrm{k}\right\| 40 \mathrm{k}=3.64 \mathrm{k} \Omega
$$

Example 6-5 For the circuit, as given in the diagram, show that (a) the ac voltage $V_{i}$ is a function of $V_{s}$ and $V_{f}$. Assume that the inverting amplifier input resistance is infinite, that $A_{v}=A_{V}=-1000$, $\beta=V_{f} / V_{0}=1 / 100, R_{s}=R_{c}=1 \mathrm{k} \Omega R_{E}, h_{i e}=1 \mathrm{k} \Omega, h_{r e}=h_{o e}=0$ and $h_{f e}=100$. (b) Find $A_{V f}=V_{0} / V_{i}$ $=A V_{i} / V_{s}$.


## Solution:

Assume that the $\beta$ network can be represented by an ideal controlled voltage source with $V_{f}=\beta V_{0}$. From the equivalent circuit we have:

$$
\begin{aligned}
V_{i} & =-h_{f e} I_{b} R_{c} \quad \text { where, } \quad I_{b}=\frac{V_{s}-V_{f}}{R_{s}+h_{i e}} \\
V_{i} & =-h_{f e} R_{c} \frac{V_{s}-V_{f}}{R_{s}+h_{i e}} \\
& =-100 k \times 1 \mathrm{k} \frac{V_{s}-V_{f}}{(1+1) \mathrm{k}} \\
& =-50\left(V_{s}-V_{f}\right)
\end{aligned}
$$

(b) With the output of the inverting amplifier connected to the input of the $\beta$ network, we have:

$$
\begin{aligned}
V_{f} & =\beta V_{0} \text { and } V_{0}=A V_{i}=A_{v} V_{i} \\
\Rightarrow \quad V_{0} & =A_{V} \times(-50)\left(V_{s}-V_{f}\right)=-A_{V} \times 50\left(V_{s}-\beta V_{0}\right) \\
V_{0} & =5 \times 10^{4}\left(V_{s}-0.001 V_{0}\right) \\
A_{v f} & =\frac{V_{0}}{V_{s}}=100
\end{aligned}
$$

Example 6-6 An amplifier with open-loop voltage gain $A V=1000 \pm 100$ is available. It is necessary to have an amplifier whose voltage gain varies by no more than $\pm 0.1 \%$. Find (a) the feedback ratio and (b) the gain with feedback.

## Solution:

(a) We know that:

$$
\begin{aligned}
& \frac{d A_{f}}{A_{f}}=\frac{d A}{A} \times \frac{1}{1+\beta A} \\
\Rightarrow \quad & \frac{0.1}{100}=\frac{1}{1+\beta A} \times \frac{100}{1000}=\frac{1}{1+\beta A} \times \frac{1}{10} \\
\therefore \quad & \beta=0.099
\end{aligned}
$$

(b) Voltage gain with feedback is given by:

$$
A_{f}=\frac{A}{1+\beta A}=\frac{1000}{1+0.099 \times 1000}=10
$$

Example 6-7 An amplifier without feedback gives a fundamental output of 36 V with $7 \%$ second harmonic distortion when the input is 0.028 V .
(a) If $1.2 \%$ of the output is feedback into the input in a negative voltage-series feedback circuit, what is the output voltage?
(b) If the fundamental output is maintained at 36 V but the second harmonic distortion is reduced to $1 \%$, what is the input voltage?

## Solution:

$$
D / D^{\prime}=7, V_{f}=1.2 \% V_{0}
$$

(a) Voltage gain:

$$
|A|=\frac{V_{0}}{V_{i}}=\frac{36}{0.028}=1285
$$

Feedback ratio:

$$
\beta=\frac{V_{f}}{V_{0}}=\frac{1.2}{100}=0.012
$$

We know that:

$$
A_{f}=\frac{A}{1+\beta A}=\frac{1285}{1+0.012 \times 1285}=78.2
$$

Therefore, output voltage:

$$
V_{0}^{\prime}=A_{f} V_{s}=78.2 \times 0.028=2.19 \mathrm{~V}
$$

(b) If the output is maintained constant at 36 V then the distortion generated by the device is unchanged. The reduction of the total distortion is caused by the feedback.
We know that:

$$
\begin{array}{cc} 
& D^{\prime}=\frac{D}{1+\beta A} \\
\Rightarrow & 1+\beta A=\frac{D}{D^{\prime}}=7 \\
\Rightarrow & \beta A=6
\end{array}
$$

and

$$
A_{f}=\frac{A}{1+\beta A}=\frac{1285}{7}
$$

and

$$
V_{s}=\frac{V_{0}}{V_{f}}=\frac{36}{1285 / 7}=0.196 \mathrm{~V}
$$

Example 6-8 The output resistance of voltage-series feedback amplifier is $10 \Omega$. If the gain of the basic amplifier is 100 and the feedback fraction is 0.01 , what is the output resistance without feedback?

## Solution:

$$
R_{o f}=10 \Omega, A=100, \beta=0.01
$$

We know that:

$$
\begin{aligned}
R_{o f} & =\frac{R_{0}}{1+\beta A} \\
R_{0} & =R_{o f}(1+\beta A) \\
& =10(1+0.01 \times 100) \\
& =20 \Omega
\end{aligned}
$$

Example 6-9 The signal and output voltages of an amplifier are 1 mV and 1 V respectively. If the gain with negative feedback is 100 and the input resistance without the feedback (voltage-series) is $2 \mathrm{k} \Omega$, find the feedback fraction and input resistance with the feedback.

## Solution:

$$
V_{s}=1 \mathrm{mV}, \quad V_{0}=1 \mathrm{~V}, \quad A_{f}=100, \quad R_{i}=20 \mathrm{k} \Omega
$$

We know that,

$$
\begin{array}{cc}
A=\frac{V_{0}}{V_{s}}=\frac{1 \mathrm{~V}}{1 \mathrm{mV}}=1000 \\
A_{f}=\frac{A}{1+\beta A} \\
\Rightarrow \quad 1+\beta A=\frac{A}{A_{f}}=\frac{1000}{100}=10 \\
\therefore \quad \beta=0.009
\end{array}
$$

Input resistance with the feedback:

$$
\begin{aligned}
R_{i f} & =R_{i}(1+\beta A) \\
& =2 \mathrm{k} \Omega \times 10=20 \mathrm{k} \Omega
\end{aligned}
$$

Example 6-10 If an amplifier has a bandwidth of 200 kHz and voltage gain of 80 , what will be the new bandwidth and gain if $5 \%$ of negative feedback is introduced?

Solution:

$$
B W=200 \mathrm{kHz}, \quad A=80, \quad \beta=5 \%=0.05
$$

We know that:

$$
\begin{aligned}
A_{f} & =\frac{A}{1+\beta A} \\
& =\frac{80}{1+0.05 \times 80}=16
\end{aligned}
$$

With the feedback:

$$
A \times B W=A_{f} \times B W_{f}
$$

$$
\begin{aligned}
\Rightarrow \quad B W_{f} & =\frac{A \times B W}{A_{f}} \\
& =\frac{80 \times 200}{16}=1 \mathrm{Mz}
\end{aligned}
$$

Example 6-11 The open-loop gain of an amplifier is -100 and distortion voltage is of 0.2 Volt. Tolerance voltage is 0.04 Volt. Find out the transmission factor.

## Solution:

Output distortion voltage with feedback is:

$$
\begin{aligned}
& V_{D f}=\frac{V_{D}}{1+A \beta} \\
& 1+A \beta=\frac{V_{D}}{V_{D f}}=\frac{0.1}{0.04}=\frac{10}{4}=2.5
\end{aligned}
$$

or

$$
\begin{aligned}
A \beta & =2.5-1=1.5 \\
\beta & =\frac{1.5}{-100}=-0.015
\end{aligned}
$$

Example 6-12 An amplifier has an open-loop gain of 500 and a feedback ratio of 0.1. If open-loop gain changes by $20 \%$ due to the temperature, find the percentage change in the closed-loop gain.

Solution:

$$
A=500, \beta=0.1, \frac{d A}{A}=20
$$

Change in closed-loop gain:

$$
\begin{aligned}
\frac{d A_{f}}{A_{f}} & =\frac{d A}{A} \times \frac{1}{1+\beta A} \\
& =20 \times \frac{1}{1+500 \times 0.1} \\
& =0.3921=39.21 \%
\end{aligned}
$$

Example 6-13 Discuss how gain of an amplifier is stabilized with negative feedback. The open loop gain of an amplifier changes by $5 \%$ if 10 dB negative feedback is applied. Calculate the percentage change of the closed loop gain.

## Solution:

$$
\frac{d A}{A}=5 \%
$$

We know that feedback is negative.
Thus,
or,

$$
20 \log _{10} \frac{A_{f}}{A}=-10
$$

$$
2 \log _{10} \frac{A_{f}}{A}=-1
$$

or,
or,
or, $\log _{10}(1+\beta A)^{2}=1$
or,

$$
(1+\beta A)^{2}=10
$$

or,

$$
(1+\beta A)=\sqrt{10}
$$

We know:

$$
\begin{aligned}
& \frac{d A_{f}}{A_{f}}=\frac{1}{1+\beta A} \frac{d A}{A} \\
& \frac{d A_{f}}{A_{f}}=\frac{1}{\sqrt{10}} 5=1.6 \%
\end{aligned}
$$

Example 6-14 An amplifier consists of three identical stages connected in cascade. The output voltage is sampled and returned to the input in series opposing. If it is specified that the relative change $d A_{f} / A_{f}$ in the closed-loop voltage gain $A_{f}$ must not exceed $y / f$, show that the minimum value of the open-loop gain $A$ of the amplifier is given by:

$$
A=3 A_{f}\left|\frac{\psi_{1}}{\psi_{f}}\right|
$$

where, $\psi \equiv d A_{1} / A_{1}$ is the relative change in the voltage gain of each stage of the amplifier.

## Solution:

From:

$$
\left|\frac{d A_{f}}{A_{f}}\right|=\frac{1}{|1+\beta A|}\left|\frac{d A}{A}\right|
$$

we obtain $\left|\frac{d A_{f}}{A_{f}}\right| \equiv\left|\psi_{f}\right|=\frac{1}{|1+\beta A|}=\left|\frac{d A}{A}\right|$
where, $\quad A=A_{1}^{3}$
or,

$$
d A=3 A_{1}^{2} d A_{1}
$$

Then,

$$
\left|\frac{d A}{A}\right|=3 \frac{d A_{1}}{A_{1}}=3 \psi_{1}
$$

$\because$

$$
A_{f}=\frac{A}{1+\beta A}
$$

$$
\frac{A_{f}}{A}=\frac{1}{1+\beta A}
$$

$$
\left.\left|\psi_{f}\right|=\frac{A_{f}}{A} 3 \psi_{1} \right\rvert\,
$$

or,

$$
A=3 A_{f} \frac{\left|\psi_{1}\right|}{\left|\psi_{f}\right|}
$$

Example 6-15 Discuss how gain of an amplifier is stabilized with negative feedback. The open loop gain of an amplifier changes by $5 \%$ if 10 dB negative feedback is applied. Calculate the percentage change of the closed loop gain.

## Solution:

$$
\frac{d A}{A}=5 \%
$$

We know that feedback is negative.
Thus,

$$
20 \log _{10} \frac{A_{f}}{A}=-10
$$

or,

$$
2 \log _{10} \frac{A_{f}}{A}=-1
$$

or,
or,

$$
2 \log _{10}(1+\beta A)=-1
$$

$$
\log _{10}(1+\beta A)^{2}=1
$$

$$
(1+\beta A)^{2}=10
$$

or,

$$
(1+\beta A)=\sqrt{10}
$$

$$
\begin{aligned}
& \frac{d A_{f}}{A_{f}}=\frac{1}{1+\beta A} \frac{d A}{A} \\
& \frac{d A_{f}}{A_{f}}=\frac{1}{\sqrt{10}} 5=1.6 \%
\end{aligned}
$$

Example 6-16 If an amplifier has a bandwidth of 200 kHz and voltage gain of 80 , what will be the new bandwidth and gain if $5 \%$ of negative feedback is introduced?

## Solution:

$$
B W=200 \mathrm{kHz}, \quad A=80, \quad \beta=5 \%=0.05
$$

We know that:

$$
\begin{aligned}
A_{f}= & \frac{\mathrm{A}}{1+\beta A} \\
& =\frac{80}{1+0.05 \times 80}=16
\end{aligned}
$$

With the feedback:

$$
\begin{aligned}
& A \times B W=A_{f} \times B W_{f} \\
& B W_{f}=\frac{A \times B W}{A_{f}} \\
& =\frac{80 \times 200}{16}=1 \mathrm{Mz}
\end{aligned}
$$

Example 6-17 The output resistance of voltage-series feedback amplifier is $10 \Omega$. If the gain of the basic amplifier is 100 and the feedback fraction is 0.01 , what is the output resistance without the feedback?

## Solution:

$$
R_{o f}=10 \Omega, \quad A=100, \quad \beta=0.01
$$

We know that:

$$
\begin{aligned}
R_{o f} & =\frac{R_{0}}{1+\beta A} \\
R_{0} & =R_{o f}(1+\beta A) \\
& =10(1+0.01 \times 100) \\
& =20 \Omega
\end{aligned}
$$

Example 6-18 An amplifier with an open-loop voltage gain $A V=1000 \pm 100$ is available. It is necessary to have an amplifier whose voltage gain varies by no more than $\pm 0.1 \%$.
(a) Find the reverse transmission factor $\beta$ of the feedback network used.
(b) Find the gain with the feedback.

## Solution:

(a) From: $\left|\frac{d A_{f}}{A_{f}}\right|=\frac{1}{|1+\beta A|}\left|\frac{d A}{A}\right|$

$$
\frac{0.1}{100}=\frac{A}{1+\beta A} \frac{100}{1000}
$$

$$
1+A \beta=100
$$

or,

$$
\beta A=99
$$

$$
\therefore \quad \beta=\frac{99}{1000}=0.099
$$

(b)

$$
A_{f}=\frac{A}{1+\beta A}=\frac{1000}{1+99}=10
$$

Example 6-19 The transistors in the feedback amplifier shown in the diagram are identical. Make reasonable approximations whenever appropriate, and neglect the reactance of the capacitors. Calculate:

$$
R_{i f}=\frac{V_{s}}{I_{1}}, \quad A_{i f}=-\frac{I}{I_{1}}, \quad A_{v f}^{\prime}=\frac{V_{0}}{V_{1}}, \quad A_{v f}=\frac{V_{0}}{V_{s}} \quad \text { and } \quad R_{o f}{ }^{\prime}
$$



## Solution:

Step 1: Consider the type of feedback. We sample the output voltage and $V_{f}=V_{0} 0.1 / 10.1=b V_{0}$; hence, it is a voltage series feedback with $b=0.0099-0.01$

Step 2: We obtain the basic amplifier without the feedback to find the input circuit we short circuit the output and to find the output circuit we open the input loop. Thus, we have the amplifier, as shown in the following figure.



Step 3: Replacing the transistors with the appropriate hybrid equivalent small signal model we obtain the next stage of the amplifier, as shown in the following figure.

Let:

$$
A V_{1}=\frac{V_{0}}{V_{f}}=\frac{V_{0}}{V_{1}} \times \frac{V_{1}}{V_{f}}
$$

$$
\frac{V_{0}}{V_{f}}=-h_{f e} \frac{4.7 \| 10.1}{h_{i e}}=-50 \times \frac{3.2}{1.1}=-145.5
$$

$$
\frac{V_{1}}{V_{f}}=-h_{f e} \frac{R_{L 1}}{R_{f 1}}
$$

But,

$$
R_{f 1}=h_{i e}+\left(1+h_{f o}\right) R_{e}=1.1+51 \times 0.1=6.2 \mathrm{~K}
$$

and

$$
R_{L 1}=22\|20.2\| h_{i e}=990 \Omega
$$

Hence,

$$
\frac{V_{1}}{V_{f}}=-50 \times \frac{0.99}{6.2}=-8.0
$$

Now that

$$
\begin{aligned}
& A_{V I} n=(-8) \times(-145.5)=1100 \\
& \quad D=1+\beta A_{V I}=1+11.60-12.6 \\
& A_{V f}^{\prime}=\frac{A_{V I}}{D}=\frac{1160}{12.6}=92.1
\end{aligned}
$$

where,

$$
\beta=0.01, \quad R_{i f}^{\prime}=R_{f 1} D .
$$

$$
R_{11}=6.2 \mathrm{k} \text { hence, } R_{i f}=0.2 \times 12.0=78 \mathrm{k}
$$

Then,

$$
\frac{V_{i}}{V_{s}}=\frac{78 \| 20.2}{0.1+78 \| 20.2}=\frac{16.1}{16.2}=0.993
$$

$$
\therefore \quad A_{v f}=A_{v f}^{\prime}=0.993-91.5
$$

We have that,

$$
R_{i f} \times L_{1}=V_{s}
$$

$$
\therefore \quad R_{i f}=78 \| 20.2-02=16.2 \mathrm{k}
$$

$$
A_{v f}=-\frac{V_{0}}{V_{s}}=-\frac{I R_{L}}{I_{1} R_{i f}}=A_{i f}=91.5 \times \frac{10.2}{4.7}=314
$$

Finally,

$$
\begin{aligned}
& R_{0}^{\prime}=4.7 \| 10.1-3.2 \mathrm{k} \\
& R_{o f}^{\prime}=\frac{R_{Q}^{\prime}}{D}=\frac{3.2}{12.6}=253 \Omega
\end{aligned}
$$

Example 6-20 An amplifier has a voltage gain of 100 . The feedback fraction is 0.04 . Find the voltage gain with the feedback.

## Solution:

Using the formula:

$$
A_{v}=\frac{A_{v}}{1+\beta A_{v}}=\frac{100}{1+0.04 \times 100}=\frac{100}{5}=20
$$

Hence, the voltage gain of the feedback is 20
Example 6-21 The signal and output voltages of an amplifier are 1 mV and 1 V respectively. If the gain with negative feedback is 100 and the input resistance without the feedback (volt-age-series) is $2 \mathrm{k} \Omega$, find the feedback fraction and input resistance with the feedback.

## Solution:

$$
V_{s}=1 \mathrm{mV}, \quad V_{0}=1 \mathrm{~V}, \quad A_{f}=100, \quad R_{i}=20 \mathrm{k} \Omega
$$

We know that:

$$
A=\frac{V_{0}}{V_{s}}=\frac{1 \mathrm{~V}}{1 \mathrm{mV}}=1000
$$

$$
A_{f}=\frac{A}{1+\beta A}
$$

$$
\Rightarrow \quad 1+\beta A=\frac{A}{A_{f}}=\frac{1000}{100}=10
$$

$$
\therefore \quad \beta=0.009
$$

Input resistance with the feedback:

$$
\begin{aligned}
R_{i f} & =R_{i}(1+\beta A) \\
& =2 \mathrm{k} \Omega \times 10=20 \mathrm{k} \Omega
\end{aligned}
$$

Example 6-22 An amplifier has a voltage gain of 200. This gain is reduced to 50 when negative feedback is applied. Determine the reverse transmission factor and express the amount of feedback in dB .

## Solution:

We know that:

$$
A=200, A_{f}=50
$$

$$
A_{f}=\frac{A}{1+\beta A}
$$

6-36 | Basic Electronics

$$
\begin{array}{ll}
\Rightarrow & 50=\frac{200}{1+\beta \times 200} \\
\therefore & \beta=0.015
\end{array}
$$

Feedback in dB:

$$
\begin{aligned}
N & =20 \log _{10}\left|\frac{A_{f}}{A}\right|=20 \log _{10}\left(\frac{1}{1+\beta A}\right) \\
& =20 \log _{10}\left(\frac{1}{1+200 \times 0.015}\right)=20 \log _{10}\left(\frac{1}{4}\right) \\
& =-12.042 \mathrm{~dB}
\end{aligned}
$$

Example 6-23 An amplifier without the feedback gives a fundamental output of 36 V with 7\% second harmonic distortion when the input is 0.028 V .
(a) If $1.2 \%$ of the output is feedback into the input in a negative voltage-series feedback circuit, what is the output voltage?
(b) If the fundamental output is maintained at 36 V but the second harmonic distortion is reduced to $1 \%$, what is the input voltage?

## Solution:

(a) Voltage gain:

$$
D / D^{\prime}=7, V_{f}=1.2 \% V_{0}
$$

$$
|A|=\frac{V_{0}}{V_{i}}=\frac{36}{0.028}=1285
$$

Feedback ratio:

$$
\beta=\frac{V_{f}}{V_{0}}=\frac{1.2}{100}=0.012
$$

We know that:

$$
A_{f}=\frac{A}{1+\beta A}=\frac{1285}{1+0.012 \times 1285}=78.2
$$

Output voltage:

$$
V_{0}^{\prime}=A_{f} V_{s}=78.2 \times 0.028=2.19 \mathrm{~V}
$$

(b) If the output is maintained constant at 36 V then the distortion generated by the device is unchanged. The reduction of the total distortion is caused by the feedback.

We know that:

$$
D^{\prime}=\frac{D}{1+\beta A}
$$

$$
\Rightarrow \quad 1+\beta A=\frac{D}{D^{\prime}}=7
$$

$$
\Rightarrow \quad \beta A=6
$$

$$
A_{f}=\frac{A}{1+\beta A}=\frac{1285}{7}
$$

$$
V_{s}=\frac{V_{0}}{V_{f}}=\frac{36}{1285 / 7}=0.196 \mathrm{~V}
$$

Example 6-24 When a negative feedback is applied to an amplifier of gain 200, the overall gain becomes 50 .
(a) Calculate the value of the feedback factor.
(b) If feedback factor remains same, calculate the value of amplifier gain, so that the overall gain becomes 30 .

## Solution:

Amplifier gain $=200$
Overall gain (gain with the feedback) $=50$
Feedback factor can be calculated from the formula:
or,

$$
\begin{aligned}
A_{f}(1+\beta A) & =A \\
(1+\beta A) & =\frac{A}{\beta A} \\
\beta A & =\frac{A}{A_{f}}-1 \\
A & =\frac{1}{A}\left(\frac{A}{A_{f}}-1\right)
\end{aligned}
$$

Putting the values:

$$
\frac{1}{200}\left(\frac{200}{50}-1\right)=\frac{3}{200}
$$

(b) If $\beta$ remains same:

$$
\beta=\frac{3}{200} \quad \text { and } \quad A_{f}=50
$$

Then:

$$
A_{f}=\frac{A}{(1+\beta A)}
$$

$$
\begin{array}{ll} 
& A_{f}(1+\beta A)=A \\
\Rightarrow & A_{f}=A\left(1-\beta A_{f}\right) \\
\Rightarrow & A=\frac{A_{f}}{1-\beta A_{f}}=\frac{30}{1-\frac{3 \times 50}{200}}=120
\end{array}
$$

Example 6-25 An amplifier without the feedback gives a fundamentals output of 36 V with $7 \%$ secondharmonic distortion when the input is 0.028 V .
(a) If $1.5 \%$ of the output is feedback into the input in a negative voltage-series feedback circuit, what is the output voltage?
(b) For an output of 36 V with $1 \%$ second-harmonic distortion, what is the input voltage?

## Solution:

(a) $A=\frac{36}{0.028}=1285$

$$
\beta=0.012
$$

From:

$$
\begin{aligned}
A_{f} & =\frac{A}{1+\beta A} \\
& =\frac{1285}{1+(0.015)(1285)}=63.38
\end{aligned}
$$

$$
\therefore \quad V_{0}=A_{f} V_{s}=63.38 \times 0.028=1.77 \mathrm{~V}
$$

(b) If the output remains constant at 36 V , then the distortion produced within the active devices of the amplifier is unchanged. However since the distortion at the output is less than in part a by a factor of 7 , follows that the feedback now increased by 9 and hence, the voltage gain decreases by 9 . Thus the input signal required to produce the same output-as in part (a) without FB-must be $V_{s}=9(0.028 \mathrm{~V})=0.252 \mathrm{~V}$.

Example 6-26 An amplifier with an open-loop voltage gain of 2000 delivers 20 W of output power at $10 \%$ second-harmonic distortion within the input signal is 10 mV . A 40 dB negative voltage-series feedback is applied and the output power is to remain at 10 W . Determine: (a) the required input signal, (b) the percent harmonic distortion.

## Solution:

(a) $-40 \mathrm{~dB}=20 \log _{10} \frac{1}{|1+\beta A|}$

$$
=-20 \log _{10}|i+\beta A|
$$

$$
\therefore \quad|1+\beta A|=100
$$

But, $\quad\left|A_{f}\right|=\frac{|A|}{|1+\beta A|}=\frac{2000}{100}=20$
When the amplifier delivers 20 W , its output voltage is:

$$
V_{0}=A_{V s}=2000(10 \times 10-3)=20 \mathrm{~V}
$$

If the output power is to remain at 10 W , then the output voltage also must remain at 10 V .
Hence, the input signal required when $I_{B}$ is applied will be $V_{s}=V_{o} / A_{f}=20 \mathrm{v} / 20$.
(b) The distortion of the amplifier with FB will be reduced by FB factor:

$$
|1+\beta A|=100
$$

Hence,

$$
D_{4}=\frac{10 \%}{100}=0.1 \%
$$

Example 6-27 For the circuit, as shown in the figure below, find:
(a) $A_{I f}=I_{0} / I_{s}$,
(b) $R_{i f}$,
(c) $A_{V f}=V_{0} / V_{s}$,
(where $I_{s}=V_{s} / R_{s}$ ),
(d) $A_{V f}{ }^{\prime}=V_{0} / V_{s}$, and (e) $R_{o f}{ }^{\prime}$.


## Solution:

(a) Step 1: Type of feedback: the mixing is of shunt type and $I_{f}=V_{1}-V / 27 \mathrm{~K}$ (where, $V$ is the voltage drop across the 3 K resistor). Since $V \gg V_{1}$ :

$$
I_{1}=-\frac{V}{27 \mathrm{~K}}=\frac{3}{27}\left(I_{0}-I_{1}\right) \quad \text { or } \quad I_{f}=\frac{3}{30} I_{0}-0.1 I_{0}=8 I_{0}
$$

Hence, this is again a current-shunt feedback.
Step 2: To obtain the basic amplifier without feedback we open the output loop $I_{0}=0$, and we thus have at the input a resistor $27+3=30 \mathrm{~K}$ in parallel with $R_{s}$. Let $V_{1}=0$; and we have at the output loop a resistor $27 \| 3 \mathrm{~K}=2.7 \mathrm{~K}$. The resulting equivalent circuit is as shown in following figure.


Step 3: Since the circuit is a current-shunt feedback amplifier the current gain will be stabilized. We now find $A_{1}$ for the basic amplifier without the feedback.

$$
A_{1}=\frac{I_{0}}{I_{2}} \frac{I_{2}}{I_{1}} \frac{I_{1}}{I_{s}}, \quad \frac{I_{0}}{I_{s}}=-h_{f e}=-50, \quad \frac{I_{2}}{I_{1}}=-h_{f e} \frac{18}{18+R_{i f}}
$$

where,

$$
R_{i f}=h_{f e}+\left(1+h_{f e}\right) 3.7 \quad \text { or } \quad R_{i f}=2+51 \times 3.7=190 \mathrm{~K}
$$

or,

$$
\begin{aligned}
& \frac{I_{1}}{I_{s}}=-50 \times \frac{18}{208}=-4.32 \\
& \frac{I_{1}}{I_{s}}=\frac{1\|10\| 30}{2+(1\|10\| 30)}
\end{aligned}
$$

But, $\quad 1\|10\| 30=\frac{1}{1+0.1+0.39}=\frac{1}{1.133}=0.0884 \mathrm{~K}$
or, $\quad \frac{I_{1}}{I_{s}}=\frac{0.884}{2.884}=0.308$

Hence,

$$
A_{1}=\frac{A_{1}}{D} b i t=D=1+\beta A_{1}=7.66 \quad \text { or } \quad A_{i f}=\frac{66.6}{7.66}=8.69
$$

(b) $R_{1}=1\|10\| 30\left\|h_{f e}=0.884\right\| 2=\frac{1.768}{2.884}=0.615$

$$
R_{i f}=\frac{6.15}{7.66}=80.2 \mathrm{~W}
$$

(c) $A_{v f}=\frac{V_{0}}{V_{1}}=\frac{I_{0} R_{C}}{I_{s} R_{s}}=A_{i f}=\frac{10}{1}=86.9$
(d) $A_{v f}=\frac{V_{0}}{V_{1}}=\frac{V_{0}}{V_{s}} \frac{V_{s}}{V_{1}}$

Now with feedback,

$$
\begin{gathered}
I_{s} R_{i f}=V_{1} \\
I_{s}=\frac{V_{s}}{R_{s}} \\
\frac{V_{s}}{V_{1}}=\frac{R_{s}}{R_{11}}=\frac{1}{0.080}=12.5
\end{gathered}
$$

Therefore,

$$
A_{v f}=86.0 \times 12.5=1070
$$

(e) $R_{o f}{ }^{\prime}=R_{o f}\left(\frac{1+\beta A_{1}}{1+\beta A_{1}}\right)$

Since,

$$
\mathrm{A}_{1}-\lim R_{L} \rightarrow 0 \text { and } A_{1} \text { is independent of } R_{L}:
$$

$$
A_{1}-A_{1} \quad \text { and } \quad R_{o f}^{\prime}-R_{0}^{\prime}=10 \mathrm{~K}
$$

Example 6-28 The circuit shown in the diagram has $R_{c}=4 \mathrm{k} \Omega, R_{L}=4 \mathrm{k} \Omega, R_{B}=20 \mathrm{k} \Omega, R_{s}=1$ $\mathrm{k} \Omega$, and the transistor parameters are: $h_{i e}=1 \mathrm{k} \Omega, h_{f e}=50, h_{r e}=2.5 \times 10^{-4}$ and $h_{o e}=24 \mu \mathrm{~S}$. Find: (a) the current gain, (b) the voltage gain, (c) the transconductance, (d) the transresistance, (e) the input resistances by the source and (f) the output resistance seen by the load. Neglect all capacitive effects.


Solution:

$$
\begin{aligned}
& R_{c}=4 \mathrm{k} \Omega, R_{L}=4 \mathrm{k} \Omega \\
& R_{B}=20 \mathrm{k} \Omega, R_{s}=1 \mathrm{k} \Omega
\end{aligned}
$$

The ac equivalent of the circuit is shown in the
following figure.
(a) Current gain, $A_{I}=\frac{I_{L}}{I_{s}}=\frac{I_{i}}{I_{s}} \frac{I_{b}}{I_{i}} \frac{I_{L}}{I_{b}}$

$$
\frac{I_{i}}{I_{s}}=\frac{R_{s}}{R_{s}+R_{i}}
$$



Input resistance:

$$
\begin{aligned}
R_{i} & =R_{b}\left\|h_{i e}=20 \mathrm{k}\right\| 1.1 \mathrm{k} \\
& =\frac{20 \times 1.1}{20+1.1}=1.04 \mathrm{k} \Omega
\end{aligned}
$$

Then:

$$
\begin{aligned}
\frac{I_{i}}{I_{s}} & =\frac{\mathrm{T} 1 \mathrm{k}}{1 \mathrm{k}+1.04 \mathrm{k}}=\frac{1}{2.04} \text { and } \quad \frac{I_{b}}{I_{i}}=\frac{R_{B}}{R_{B}+h_{i e}} \\
& =\frac{20}{20+1.1}=0.95 \\
\frac{I_{L}}{I_{b}} & =-h_{f e} \frac{R_{c}}{R_{c}+R_{L}} \\
& =-50 \times \frac{4}{4+4}=-25
\end{aligned}
$$

$$
\begin{aligned}
A_{1} & =\frac{I_{L}}{I_{s}}=\frac{1}{2.04} \times 0.95 \times(-25) \\
& =-11.65
\end{aligned}
$$

(b) Voltage gain, $A_{V}=\frac{V_{0}}{V_{s}}=\frac{I_{L} R_{L}}{I_{s} R_{s}}$

$$
=(-11.65) \times \frac{4 \mathrm{k}}{1 \mathrm{k}}=-46.6
$$

(c) Transconductance, $G_{m}=\frac{I_{L}}{V_{s}}=\frac{V_{0}}{R_{L}} \frac{1}{V_{s}}=\frac{V_{0}}{V_{s}} \frac{1}{R_{L}}$

$$
=\frac{-46.6}{4 \mathrm{k}}=-11.65 \mathrm{~mA} / \mathrm{V}
$$

(d) Transresistance, $R_{m}=\frac{V_{0}}{I_{s}}=\frac{R_{s}}{V_{s}} V_{0}=\frac{V_{0}}{V_{s}} R_{s}$

$$
=1 \mathrm{k} \times(-46.6)=-46.6 \mathrm{k} \Omega
$$

(e) Input resistance, $R_{i}=1.04 \mathrm{k} \Omega$
(f) Output resistance, $R_{0}=R_{c}\left\|\frac{i}{h_{o e}}=4 \mathrm{k}\right\| 40 \mathrm{k}=3.64 \mathrm{k} \Omega$

## POINTS TO REMEMBER

1. Feedback is defined as the process by which a portion of the output is returned to the input to form part of the system excitation.
2. The four feedback topologies are:
(a) Shunt-shunt
(b) Shunt-series
(c) Series-shunt
(d) Series-series
3. The main advantage of negative feedback is stability. Its main application is in the design of a stable amplifier.
4. Positive feedback produces instability in the system. Its main application is in the design of an oscillator.
5. Conditions for Barkhausen criteria:
(a) Positive feedback
(b) Loop gain is unity, i.e., $\mathrm{A} \beta=1$; therefore, feedback gain is infinite $\left(\mathrm{A}_{\mathrm{f}}=\infty\right)$.
(c) Phase variation is zero or integral multiple of 360.
6. The frequency of a sinusoidal oscillator is determined by the condition that the loop gain phase shift is zero.

## IMPORTANT FORMULAE

1. Gain with feedback:

$$
A_{f}=\frac{A}{1+A \beta}
$$

2. dB of feedback:

$$
N=20 \log _{10}\left|\frac{A_{f}}{A}\right|=20 \log _{10}\left(\frac{1}{1+\beta A}\right)
$$

3. Sensitivity:

$$
S=\frac{\frac{d A_{f}}{A_{f}}}{\frac{d A}{A}}=\frac{1}{1+A \beta}
$$

4. Voltage-series feedback:

$$
\begin{aligned}
Z_{i f} & =\frac{V_{s}}{I_{i}}=Z_{i}\left(1+\beta A_{V}\right) \\
Z_{o f} & =\frac{V}{I}=\frac{Z_{o}}{1+\beta A_{v}}
\end{aligned}
$$

5. Current-series feedback:

$$
\begin{aligned}
& Z_{i f}=Z_{i}\left(1+\beta Y_{M}\right) \\
& Z_{o f}=Z_{o}\left(1+\beta Y_{m}\right)
\end{aligned}
$$

6. Current-shunt feedback:

$$
\begin{aligned}
Z_{i f} & =\frac{Z_{i}}{1+\beta A_{I}} \\
Z_{o f} & =\frac{V}{I}=Z_{o}(1+\beta A)
\end{aligned}
$$

7. Voltage-shunt feedback:

$$
\begin{aligned}
Z_{i f} & =\frac{Z_{i}}{1+\beta Z_{M}} \\
Z_{o f} & =\frac{Z_{o}}{1+\beta Z_{m}}
\end{aligned}
$$

8. Distortion with feedback:

$$
D^{\prime}=\frac{D}{1+A_{v} \beta}
$$

## OBJECTIVE QUESTIONS

1. Open-loop gain of an amplifier is given by:
(a) $A$
(b) $A \beta$
(c) $\beta$
(d) None of the above
2. Loop gain is given by:
(a) $A$
(b) $A \beta$
(c) $\beta$
(d) None of the above
3. In a feedback amplifier, sensitivity $D$ is equal to:
(a) $A \beta$
(b) $1-A \beta$
(c) $1+A \beta$
(d) $1 /(A \beta+1)$
4. In a negative feedback amplifier, voltage sampling:
(a) Tends to decrease the output resistance
(b) Tends to increase to output resistance
(c) Does not alter the output resistance
(d) Produces the same effect on output resistance as current sampling
5. In a negative feedback amplifier, current sampling:
(a) Tends to increase the output resistance
(b) Tends to decrease the output resistance
(c) Does not alter the output resistance
(d) Produces the same effect on input resistance as voltage sampling
6. In a negative feedback amplifier, series mixing:
(a) Tends to increase the input resistance
(b) Tends to decrease the input resistance
(c) Does not alter the input resistance
(d) Produces the same effect on input resistance as shunt mixing
7. In a negative feedback amplifier, shunt mixing:
(a) Tends to increase the input resistance
(b) Tends to decrease the input resistance
(c) Does not alter the input resistance
(d) Produces the same effect on input resistance as the series mixing
8. Negative feed back in an amplifier improves:
(a) The signal to noise ratio at the output
(b) Reduces distortion
(c) Both (a) and (b)
(d) None of the above
9. For a shunt-shunt negative feedback amplifier
(a) Input impedance decreases but output impedance increases
(b) Both input impedance and output impedance increases
(c) Both input impedance and output impedance decreases
(d) None of the above
10. An amplifier with the negative feedback:
(a) Controls the gain
(b) Reduces the noise
(c) Reduces phase distortion
(d) All of the above
11. An amplifier with resistive negative feedback has two left half plane poles in its open-loop transfer junction. The amplifier will be:
(a) Stable for all frequencies
(b) Unstable for all frequencies
(c) Stable for a particular frequencies
(d) Unstable for a particular frequencies
12. Barkhusen criteria is:
(a) Positive feedback, $A \beta=1, \theta=0$ or multiple 360
(b) Negative feedback, $A \beta=1, \theta=0$ or multiple 360
(c) Positive feedback, $A \beta=0, \theta=0$ or multiple 360
(d) Negative feedback, $A \beta=1, \theta=180$

## REVIEW QUESTIONS

1. Draw and explain the concept of feedback in detail with the help of a block diagram. Explain the operation of each block.
2. What do you mean by positive and negative feedback?
3. Calculate the expression for feedback gain for an amplifier?
4. Explain the following terms
(a) Feedback ratio
(b) Feedback factor
(c) Open-loop gain
(d) Closed-loop gain
5. Classify the different topologies of a feedback network. Explain each topology with the help of block diagrams and proper circuit diagrams.
6. Explain the advantages and disadvantages of negative feedback.
7. Explain the advantages and disadvantages of positive feedback.
8. "Gain bandwidth product is constant." Comment on this statement with respect to negative feedback.
9. What is Barkhausen criterion? Explain the use of it.
10. Negative feedback reduces the gain of an amplifier, but why is it used in an amplifier design?
11. What is Nyquist Criterion? Why this is so important in oscillator design?

## PRACTICE PROBLEMS

1. The open-loop gain of an amplifier changes by $20 \%$ due to changes in the parameters of the active amplifying devices. If gain changes by $5 \%$, what type of feedback has to be applied? Find the minimum value of the feedback ratio and open-loop gain for the feedback gain of -30 .
2. The open-loop gain of an amplifier is -1000 and gives an output distortion voltage of 0.15 Volt. For negative feedback the tolerable output distortion voltage is 0.05 Volt. Find out the reverse transmission factor.
3. An amplifier has a voltage gain of 100 . The feedback ratio is 0.15 . Find:
(a) The voltage gain with feedback band feedback in dB.
(b) The feedback factor.
(c) The output voltage, if input voltage is 1.15 Volt.
(d) The feedback voltage.
4. An amplifier has a bandwidth of 300 kHz and voltage gain of 100 , what will be the new bandwidth and gain if $10 \%$ of negative feedback is introduced?
5. The signal and output voltages of an amplifier are 5 mV and 1 V , respectively. If the
gain with negative feedback is 200 and the input resistance without feedback (voltageseries) is $2 \mathrm{k} \Omega$, find the feedback fraction and input resistance with the feedback.
6. An amplifier has a bandwidth of 30 kHz and voltage gain of 100 , what will be the new bandwidth and gain if $9 \%$ of negative feedback is introduced?
7. The signal and output voltages of an amplifier are 12 mV and 2 V , respectively. If the gain with negative feedback is 60 and the input resistance without feedback is $8 \mathrm{k} \Omega$, calculate the feedback fraction and input resistance with feedback.
8. An amplifier uses negative feedback having an open-loop gain of -30 and voltage amplification of -100 . Calculate the overall gain and reverse transfer ratio.
9. If open-loop gain of an amplifier changes by $20 \%$ calculate the percentage change of the closed-loop gain if a 10 dB negative feedback is applied.
10. The open-loop gain of an amplifier is 99 and distortion voltage is in the order of 0.35 volt. Tolerance voltage is 0.06 volt. Calculate the transmission factor.

## SUGGESTED READINGS

1. Singh, J. 1994. Semiconductor Devices: An Introduction. New York, NY: McGraw-Hill.
2. Streetman B.G., Banerjee S. 2000. Solid State Electronic Devices. 5th Ed. New Delhi: Pearson Education.
3. Millman, Jacob, Halkias Christos C. 1986. Integrated Electronics: Analog and Digital

Circuits and Systems. New Delhi: McGraw Hill Book Company.
4. Pierret, R. F and G.W. Neudeck. 1989. Modular Series on Solid State Devices. Boston, M.A.: Addison Wesley.
5. Singh, B. P. and Rekha Singh. 2006. Electronic Devices and Integrated Circuits. New Delhi: Pearson Education.

This page is intentionally left blank.

## 7

## Oscillators

## Outline

## 7-1 Introduction

7-2 Classifications of Oscillators
7-3 Circuit Analysis of a General Oscillator

7-5 Tuned Oscillator<br>7-6 Crystal Oscillator<br>7-7 Real-Life Applications

7-4 Conditions for Oscillation: Barkhausen Criteria

## Objectives

In this chapter we will explore the working principle of the oscillator. Generally speaking, the oscillator produces sinusoidal and other waveforms. Beginning with a detailed circuit analysis of the oscillator, we will proceed to discuss the conditions and frequency of oscillation. Following this, the different types of oscillators-Tuned oscillator, Hartley oscillator, Colpitts oscillator, Clapp oscillator, Phase-shift oscillator, Crystal oscillator and Wien-bridge oscillator-will be examined with detailed mathematical analysis and illustrations. The chapter ends with an overview of the applications of the oscillator.

## 7-1 INTRODUCTION

An oscillator is an electronic system. It comprises active and passive circuit elements and sinusoidal produces repetitive waveforms at the output without the application of a direct external input signal to the circuit. It converts the dc power from the source to ac power in the load. A rectifier circuit converts ac to dc power, but an oscillator converts dc noise signal/power to its ac equivalent. The general form of a harmonic oscillator is an electronic amplifier with the output attached to a narrow-band electronic filter, and the output of the filter attached to the input of the amplifier. When the power supply to the amplifier is just switched on, the amplifier's output consists only of noise. The noise travels around the loop, being filtered and re-amplified till it increasingly resembles the desired signal level. In this chapter, the oscillator analysis is done in two methods-first by a general analysis, considering all other circuits are the special form of a common generalized circuit and second, using the individual circuit KVL analysis. The difference between an amplifier and an oscillator is shown in Figure 7-1. Figure 7-1(a) shows how an amplifier produces output based on the given input. Figure 7-1(b) shows how an oscillator produces output without any direct input.


Figure 7-1 Schematic block diagrams showing the difference between an amplifier and an oscillator
Table 7-1 Different types of oscillators and their frequency ranges

| Type of Oscillator | Frequency Range Used |
| :--- | :--- |
| Audio-frequency oscillator | $20 \mathrm{~Hz}-20 \mathrm{kHz}$ |
| Radio-frequency oscillator | $20 \mathrm{kHz}-30 \mathrm{MHz}$ |
| Very-high-frequency oscillator | $30 \mathrm{MHz}-300 \mathrm{MHz}$ |
| Ultra-high-frequency oscillator | $300 \mathrm{MHz}-3 \mathrm{GHz}$ |
| Microwave oscillator | $3 \mathrm{GHz}-30 \mathrm{GHz}$ |
| Millimeter wave oscillator | $30 \mathrm{GHz}-300 \mathrm{GHz}$ |

## 7-2 CLASSIFICATIONS OF OSCILLATORS

Oscillators are classified based on the type of the output waveform. If the generated waveform is sinusoidal or close to sinusoidal (with a certain frequency) then the oscillator is said to be a sinusoidal oscillator. If the output waveform is non-sinusoidal, which refers to square/saw-tooth waveforms, the oscillator is said to be a relaxation oscillator. In this chapter the oscillator circuits are designed by transistors, but oscillators also can be designed using the FET and op-amp.

An oscillator has a positive feedback with the loop gain infinite. Feedback-type sinusoidal oscillators can be classified as LC (inductor-capacitor) and RC (resistor-capacitor) oscillators. The classification of various oscillators is shown in Table 7-1.

Generally no direct external signal is applied to an oscillator circuit. During the period when the power supply to the system is switched on, a noise voltage is generated which triggers the oscillations. A negative resistance must be provided in an oscillator by an external positive feedback to make the gain infinite.

## 7-3 CIRCUIT ANALYSIS OF A GENERAL OSCILLATOR

This section discusses the general oscillator circuit with a simple generalized analysis using the transistor, as shown in Figure 7-2. An impedance $z_{1}$ is connected between the base $B$ and the emitter $E$, an impedance $z_{2}$ is connected between the collector $C$ and emitter $E$. To apply a positive feedback $z_{3}$ is connected between the collector and the base


Figure 7-2 A generalized oscillator circuit analysis
terminal. All the other different oscillators can be analysed as a special case of the generalized analysis of oscillator.

The above generalized circuit of an oscillator is considered using a simple transistor-equivalent circuit model. The equivalent model of transistor, as calculated in Chapter 5, where the current voltage expressions are expressed as follows:

$$
\begin{equation*}
v_{1}=h_{i} i_{1}+h_{r} v_{2} \simeq h_{i} i_{1} \tag{7-1}
\end{equation*}
$$

As the numerical value of $h_{r} v_{2}$ is negligible:

$$
\begin{gather*}
v_{1}=h_{i} i_{1}  \tag{7-2}\\
i_{2}=h_{f} i_{1}+h_{0} v_{2} \simeq h_{f} i_{1} \tag{7-3}
\end{gather*}
$$

As the numerical value of $h_{0} v_{2}$ negligible the Equation (7-3) can be written as:

$$
\begin{equation*}
i_{2}=h_{f} i_{1} \tag{7-4}
\end{equation*}
$$

Applying KVL at loop (1) of Figure 7-2 by considering that current through the impedance $z_{1}$ is $\left(i_{1}-i_{3}\right)$, we get:

$$
\begin{align*}
& v_{1}+z_{1}\left(i_{1}-i_{3}\right)=0 \\
& \text { or, } \quad v_{1}=-z_{1}\left(i_{1}-i_{3}\right)=z_{1}\left(i_{3}-i_{1}\right)
\end{align*}
$$

Substituting the value of voltage $v_{1}$ from Equation (7-2) in Equation (7-5) we get:
or,

$$
\begin{align*}
& h_{i} i_{1}+z_{1} i_{1}-z_{1} i_{3}=0 \\
& \quad i_{1}\left(h_{1}+z_{1}\right)-z_{i} i_{3}=0 \tag{7-6}
\end{align*}
$$

Applying KVL at loop (3) by considering voltage across the impedance $z_{2}$ :

$$
\begin{equation*}
v_{2}+z_{2}\left(i_{3}+i_{2}\right)=0 \tag{7-7}
\end{equation*}
$$

Substituting the value of current $i_{2}$ we get:
or,

$$
\begin{align*}
& v_{2}=-z_{2}\left(h_{f} i_{1}+i_{3}\right) \\
& \quad z_{2} h_{f} i_{1}+z_{2} i_{3}+v_{2}=0 \tag{7-8}
\end{align*}
$$

Applying the KVL at loop (2) by considering voltage across $z_{3}$ we get,

$$
\begin{equation*}
i_{3} z_{3}+\left(i_{2}+i_{3}\right) z_{2}+\left(i_{3}-i_{1}\right) z_{1}=0 \tag{7-9}
\end{equation*}
$$

or,

$$
\begin{gather*}
i_{3} z_{3}-v_{2}+v_{1}=0  \tag{7-10}\\
i_{3} z_{3}=v_{2}-v_{1} \tag{7-11}
\end{gather*}
$$

Substituting the value of $v_{1}$ in Equation (7-11) we get:
or,

$$
\begin{gather*}
i_{3} z_{3}=v_{2}-h_{i} i_{1}  \tag{7-12}\\
i_{3} z_{3}-v_{2}+h_{i} i_{1}=0  \tag{7-13}\\
-\left(v_{2}-i_{3} z_{3}-h_{i} i_{1}\right)=0  \tag{7-14}\\
v_{2}-h_{i} i_{1}-z_{3} i_{3}=0 \tag{7-15}
\end{gather*}
$$

or,
or,
Equation (7-6), Equation (7-8) and Equation (7-15) can be rewritten as:

$$
\begin{aligned}
& i_{1}\left(h_{i}+z_{1}\right)+0 . v_{2}+\left(-z_{1}\right) i_{3}=0 \\
&-i_{1} z_{2} h_{f}+1 \cdot v_{2}+z_{2} i_{3}=0 \\
&-i_{1} h_{i}+1 . v_{2}+\left(-z_{3}\right) i_{3}=0
\end{aligned}
$$

Eliminating three variables $i_{1}, v_{2}, i_{3}$ using Camers rule, and from Equations (7-6), (7-8) and (7-15), we get the following matrix:

$$
\left|\begin{array}{ccr}
\left(h_{i}+z_{1}\right) & 0 & -z_{1} \\
z_{2} h_{f} & 1 & z_{2} \\
-h_{i} & 1 & -z_{3}
\end{array}\right|=0
$$

or,

$$
\begin{equation*}
\left(h_{i}+z_{1}\right)\left[-z_{3}-z_{2}\right]+0+\left(-z_{1}\right)\left[z_{2} h_{f}+h_{i}\right]=0 \tag{7-16}
\end{equation*}
$$

or,

$$
-z_{3} h_{i}-z_{2} h_{i}-z_{1} z_{3}-z_{1} z_{2}-z_{1} z_{2} h_{f}-z_{1} h_{i}=0
$$

or,

$$
-h_{i}\left[z_{3}+z_{2} z_{1}\right]-z_{1} z_{2}\left[1+h_{f}\right]-z_{1} z_{3}=0
$$

or,

$$
h_{i}[R+j x]+z_{1} z_{2}\left[1+h_{f}\right]+z_{1} z_{3}=0
$$

Let,

$$
\begin{array}{llll}
z_{1}=R_{1}+j x_{1} \simeq j x_{1} & \Theta & R_{1} \simeq x_{1} \\
z_{2}=R_{2}+j x_{2} \simeq j x_{2} & & R_{2} \simeq x_{2} \\
z_{3}=R_{3}+j x_{3} \simeq j x_{3} & \& & R_{3} \simeq x_{3}
\end{array}
$$

By adding, we get:

$$
\left(z_{1}+z_{2}+z_{3}\right)=(R+j x)
$$

where, $R=\left(R_{1}+R_{2}+R_{3}\right)$ is not negligible in comparison with $x=x_{1}+x_{2}+x_{3}$ as we shall see $x=0$, at frequency of oscillation.

$$
\begin{align*}
\therefore \quad \mathrm{z}_{1} z_{2} & \left(h_{f}+1\right)+\left(z_{1}+z_{2}+z_{3}\right) h_{i}+z_{1} z_{3}=0  \tag{7-17}\\
& -x_{1} x_{2}\left(h_{f}+1\right)+(R+j x) h_{i}-x_{1} x_{3}=0 \\
& -x_{1}\left[x_{2}\left(h_{f}+1\right)+x_{3}\right]+(R+j x) h_{i}=0 \tag{7-18}
\end{align*}
$$

Equating imaginary parts $\quad\left[\Theta j x_{1} j x_{2}=-x_{1} x_{2}\right]:$

$$
j x h_{\mathrm{i}}=0 \quad(+\mathrm{ve}) \text { inductive impedance }
$$

$$
\therefore \quad \begin{align*}
x & =0 \quad(-\mathrm{ve}) \text { capacitive impedance } \\
x_{1}+x_{2}+x_{3} & =0 \tag{7-19}
\end{align*}
$$

Equating real parts we get:

$$
\begin{array}{r}
-x_{1} x_{2}\left[h_{f}+1\right]+R h_{i}-x_{1} x_{3}=0 \\
x_{1} x_{2} h_{f}+x_{1}\left(x_{2}+x_{3}\right)-R \cdot h_{i}=0 \tag{7-21}
\end{array}
$$

From the Equation (7-19) we get: $\quad x_{2}+x_{3}=-x_{1}$
Substituting the value of Equation (7-22) in Equation (7-19) we get:

$$
\begin{array}{r}
x_{1} x_{2} h_{f}-x_{1}^{2}-R \cdot h_{i}=0 \\
h_{f}=\frac{x_{1}}{x_{2}}+\frac{R \cdot h_{i}}{x_{1} x_{2}} \tag{7-23}
\end{array}
$$

This is the general condition for oscillation for an oscillator.
Different types of oscillator circuits with different configurations can be analysed through this general method. This makes the analysis simpler.

## 7-3-1 Hartley Oscillator

Hartley oscillator contains two inductors and one capacitor, as shown in Figure 7-3 where, $x_{1}$ and $x_{2}$ are inductances, and $x_{3}$ is a capacitance, i.e., $x_{1}=\omega L_{1}, x_{2}=\omega L_{2}$, $x_{3}=-1 / \omega C$.

Substituting the values in Equation (7-23) we get the condition for oscillation, considering $R$ is small.

$$
\begin{align*}
\quad h_{f} & =\frac{\omega L_{1}}{\omega L_{2}}+\frac{R \cdot h_{i}}{\omega^{2} L_{1} L_{2}} \\
\therefore \quad h_{f} & =\frac{L_{1}}{L_{2}} \\
h_{f} & =\frac{L_{1}}{L_{2}}+\frac{R C h_{i}}{L_{11}} \tag{7-24}
\end{align*}
$$



Figure 7-3 Hartley Oscillator

Where, $\quad L_{11}=\frac{L_{1} L_{2}}{L_{1}}+L_{2}$

$$
\begin{array}{l|l}
L_{11}=\frac{\Theta x_{1}+x_{2}=-x_{3}}{L_{1}} & \omega L_{1}+\omega L_{2}=-\left(\frac{-1}{\omega C}\right) \\
L_{11}=L_{1} L_{2} / L_{1}+L_{2} & L_{1}+L_{2}=-\frac{1}{\omega^{2} C} \\
L_{11}\left(L_{1}+L_{2}\right)=L_{1} L_{2} &
\end{array}
$$

$$
\therefore \quad \frac{L_{1}}{L_{2}}+\frac{R h_{i}}{\omega^{2} L_{1} L_{2}}=\frac{L_{1}}{L_{2}}+\frac{R h_{i}}{\omega^{2} L_{1} L_{2}}=\frac{L_{1}}{L_{2}}+\frac{R h_{i} C}{L_{11}}
$$

Frequency of oscillation can be calculated as follows:

$$
\begin{align*}
\omega L_{1}+\omega L_{2} & =-\left(-\frac{1}{\omega C}\right) \\
\omega^{2}\left(L_{1}+L_{2}\right) & =\frac{1}{c} \\
\omega & =\frac{1}{\sqrt{C\left(L_{1}+L_{1}\right)}} \\
2 \pi f & =\frac{1}{\sqrt{C\left(L_{1}+L_{1}\right)}} \\
f & =\frac{1}{2 \pi} \sqrt{C\left(L_{1}+L_{1}\right)} \tag{7-25}
\end{align*}
$$

This is the required frequency of oscillation for Hartley oscillator.

## 7-3-2 Colpitts Oscillator

Colpitts oscillator contains two capacitors and one inductor, as shown in Figure 7-4. $X_{1}$ and $X_{2}$ are capacitances, $X_{3}$ is inductance, $Z_{1}$ and $Z_{2}$ are capacitors, $C_{1}$ and $C_{2}$ are capacitances, and $Z_{3}$ is an inductor of inductance $L$.

$$
\begin{aligned}
& X_{1}=-\frac{1}{\omega C_{1}} \\
& X_{2}=-\frac{1}{\omega C_{2}} \\
& X_{3}=\omega L
\end{aligned}
$$



Figure 7-4 Colpitts oscillator

$$
\begin{gathered}
X_{1}+X_{2}+X_{3}=0 \\
-\frac{1}{\omega C_{1}}-\frac{1}{\omega C_{2}}+\omega L=0 \\
\frac{1}{\omega}\left(\frac{1}{C_{1}}+\frac{1}{C_{2}}\right)=\omega L \\
\frac{1}{L}\left(\frac{1}{C_{1}}+\frac{1}{C_{2}}\right)=\omega^{2}, \quad \omega=\sqrt{\frac{1}{L}\left(\frac{1}{C_{1}}+\frac{1}{C_{2}}\right)}
\end{gathered}
$$

Frequency of oscillation:

$$
\begin{equation*}
2 \pi f=\frac{1}{\sqrt{L C}} \Rightarrow f=\frac{1}{2 \pi \sqrt{L C}} \tag{7-26}
\end{equation*}
$$

where, $\quad \frac{1}{C^{\prime}}=\frac{1}{C_{1}}+\frac{1}{C_{2}}$

$$
\begin{equation*}
h_{f}=\frac{X_{1}}{X_{2}}+\frac{R h_{i}}{X_{1} X_{2}} \tag{7-27}
\end{equation*}
$$

Therefore, condition for oscillation:

$$
\begin{align*}
h_{f} & =\frac{C_{2}}{C_{1}}+R h_{i} \omega^{2} C_{1} C_{2}  \tag{7-28}\\
& =\frac{C_{2}}{C_{1}}+R_{h i} \omega^{2} C_{1} C_{2}
\end{align*}
$$

$R=$ Resistance of the coil 2

$$
\begin{align*}
& \quad R=\frac{C_{2}}{C_{1}}+R h_{i} \frac{1}{L} \frac{C_{1}+C_{2}}{C_{1} C_{2}} C_{1} C_{2}\left[\because \omega^{2}=\frac{1}{L}\left(\frac{1}{C_{1}}+\frac{1}{C_{2}}\right)\right] \\
& R=\frac{C_{2}}{C_{1}}+R h_{i} \frac{1}{L}\left(C_{1}+C_{2}\right) R h_{i}  \tag{7-29}\\
& R=\frac{C_{2}}{C_{1}}\left[\text { neglecting } \frac{R h_{i}}{L}\left(C_{1}+C_{2}\right)\right]
\end{align*}
$$

The circuit diagram of Colpitts oscillator is shown in Figure 7-4.

## 7-3-3 Phase-Shift Oscillator

The circuit diagram of a phase-shift oscillator with three pairs of RC combination is shown in Figure 7-5(a).

The equivalent circuit representation of phase-shift oscillator is shown in Figure 7-5(b). By applying KVL in the circuit in Figure 7-5(b) we have the mesh ABCHIJ at loop (2).

$$
\begin{array}{r}
\left(i+h_{f} i_{1}\right) R+\left(i-i^{1}\right) R+\frac{i}{j w c}=0 \\
\left(2 R+\frac{1}{j w c}\right) i+R h_{f} i_{1}-R i^{1}=0 \\
\left(2 R+j x_{c}\right) i+R h_{f} i_{1}-R i^{1}=0 \tag{7-30}
\end{array}
$$

At mesh CDGH [at loop (3)]:


Figure 7-5(a) Phase-shift oscillator: equivalent circuit using the approximate equivalent circuit of the transistor


Figure 7-5(b) Equivalent circuit representation of a phase-shift oscillator

$$
\begin{gather*}
\left(i^{1}-i\right) R+\frac{1}{j \omega c} i^{1}+\left(i^{1}-i_{1}\right) R=0 \\
\left(2 R+j x_{c}\right) i^{1}-R i-R i_{1}=0 \tag{7-31}
\end{gather*}
$$

At mesh CDEFGH [at loop (4)]:

$$
\begin{array}{r}
\left(i_{1}-i^{1}\right) R+j x_{c} i_{1}+R i_{1}=0 \\
\left(2 R+j x_{c}\right) i_{1}-R i^{1}=0 \tag{7-32}
\end{array}
$$

Eliminating $i_{1}, i, i^{1}$, order wise Equations (7-30), (7-31) and (7-32) will be:

$$
\left|\begin{array}{ccc}
i_{1} & i & i^{1} \\
\left(2 R+j x_{c}\right) & 0 & -R \\
R h_{f} & \left(2 R+j x_{c}\right) & -R \\
-R & -R & \left(2 R+j x_{c}\right)
\end{array}\right|
$$

Dividing each element of the determinant by $R$ :

$$
\therefore \quad \frac{1}{\mathrm{R}}\left|\begin{array}{ccc}
R\left(2+j x_{c} / R\right) & 0 & -R \\
R_{h f} & R\left(2+j x_{c} / R\right) & -R \\
-R & -R & R\left(2+j x_{c} / R\right)
\end{array}\right|=0
$$

Let

$$
\frac{X_{C}}{R}=a
$$

$\therefore \quad\left|\begin{array}{ccc}(2+j a) & 0 & -1 \\ h_{f} & (2+j a) & -1 \\ -1 & -1 & (2+j a)\end{array}\right|=0$

$$
\begin{aligned}
(2+j a)\left[(2+j a)^{2}-1\right]+0+(-1)\left[-h_{f}+2+j a\right] & =0 \\
(2+j a)\left[4+4 j a-\mathrm{a}^{2}-1\right]+h_{f}-2-j a & =0 \\
8+8 j a-2 a^{2}-2+4 j a-4 a^{2}-j a^{3}-j a+h_{f}-2-j a & =0 \\
-j a^{3}+8+12 j a-6 a^{2}-4-2 j a+h_{f} & =0
\end{aligned}
$$

$\therefore$ Equating the imaginary parts:

$$
\begin{aligned}
& j\left(-a^{3}-2 a+12 a\right)=0 \\
& a\left(10-a^{2}\right)=0 \\
& a^{2}-10=0 \\
& \therefore \quad a=\sqrt{10} \\
& \frac{X C}{R}=\sqrt{10} \\
& \frac{X_{c}^{2}}{R^{2}}=10
\end{aligned}
$$

$$
\frac{1}{\omega^{2} C^{2} R^{2}}=10
$$

or, $\quad \omega^{2}=\frac{1}{10 C^{2} R^{2}}$
or, $\quad \omega=\frac{1}{\sqrt{10} C R}$
$\therefore$ Frequency of oscillation is: $f=\frac{1}{2 \pi \sqrt{10} C R}$
Equating the real parts we get:

$$
\begin{aligned}
8 & -6 a^{2}-4+h_{f e}=0 \\
h_{f e} & =4+6 a^{2}-8=4+6.10-8 \\
& =4+60-8 \\
& =56
\end{aligned}
$$

For sustained oscillations, $h_{f e}$ of 56 for $R=R_{L}$ The equivalent diagram of a phase-shift oscillator is shown in Figure 7-6.


Figure 7-6 Equivalent diagram of a phase-shift oscillator

## 7-3-4 Wien-Bridge Oscillator

Wien-bridge oscillator is the series and parallel combination of a resistance $R$ and a capacitor $C$. According to Barkhausen criteria, $A_{v} \beta=1$.
Since, $\quad A_{v} \beta=1$

$$
\begin{array}{r}
\beta=\frac{1}{A_{v}}=\frac{v_{i r}}{v_{o}}=\frac{v_{z i}}{\left(z_{1}+z_{2}\right) i} \\
A_{v}=\frac{1}{\beta}=\frac{z_{1}+z_{2}}{z_{2}}=1+\frac{z_{1}}{z_{2}} \\
z_{1}=R+j x_{1} \text { (series combination) } \\
\frac{1}{z_{2}}=\frac{1}{R_{2}}+\frac{1}{j x_{2}} \text { (parallel combination) } \\
A=1+\left(R_{1}+j x_{1}\right)\left(\frac{1}{R_{2}}+\frac{1}{j x_{2}}\right) \\
=1+\left(\frac{R_{1}}{R_{2}}+\frac{x_{1}}{x_{2}}\right)+j\left(\frac{x_{1}}{R_{2}}-\frac{R_{1}}{x_{2}}\right) \tag{7-35}
\end{array}
$$

The two-stage $R C$ coupled amplifier can be used by equating real and imaginary parts. Considering only the real parts, we get:

$$
\begin{equation*}
A=1+\frac{R_{1}}{R_{2}}+\frac{x_{1}}{x_{2}} \tag{7-36}
\end{equation*}
$$

Considering only the imaginary parts, we get:

$$
\begin{equation*}
\frac{x_{1}}{R_{2}}-\frac{R_{1}}{X_{2}}=0 \tag{7-37}
\end{equation*}
$$

$X_{1} X_{2}=R_{1} R_{2}$ (frequency of oscillation)

$$
\begin{align*}
R_{1} R_{2} & =\frac{1}{w^{2} c_{1} c^{2}} \\
w^{2} & =\frac{1}{C_{1} C_{2} R_{1} R_{2}} \tag{7-38}
\end{align*}
$$

If $R_{1}=R_{2}=R \quad \& \quad C_{1}=C_{2}=C$

$$
A=1+1+1=3
$$

and,

$$
\begin{aligned}
& w^{2}=\frac{1}{C^{2} R^{2}} \Rightarrow w=\frac{1}{C R} \\
& f=\frac{1}{2 \pi C R}
\end{aligned}
$$



Figure 7-7 Wien-bridge oscillator

At balance condition: $\quad \frac{R_{3}}{R_{4}}=\frac{Z_{1}}{Z_{2}}$ (for oscillation)
From the circuit diagram of the Wien-bridge oscillator, as given in Figure 7-7, we get:

$$
\begin{align*}
\frac{R_{3}}{R_{4}} & =\left(R_{1}+\frac{1}{j w c_{1}}\right)\left(\frac{1}{R_{2}}+j w c_{2}\right)  \tag{7-41}\\
& =\left(\frac{R_{1}}{R_{2}}+\frac{C_{2}}{C_{1}}\right)+j\left(\omega C_{2} R_{1}-\frac{1}{\omega C_{1} R_{2}}\right)
\end{align*}
$$

Equating imaginary parts we get:

$$
\begin{align*}
\omega c_{2} R_{1} & =\frac{1}{\omega C_{1} R_{2}} \\
\omega^{2} & =\frac{1}{C^{2} R^{2}} \tag{7-42}
\end{align*}
$$

$$
\begin{aligned}
& \because R_{1}=R_{2}=R \quad \text { and } \quad C_{1}=C_{2}=\mathrm{C} \\
& \therefore \quad \\
& \therefore \frac{R_{3}}{R_{4}}=\frac{R_{1}}{R_{2}}+\frac{C_{2}}{C_{1}} \\
& \\
& \\
& \frac{R_{3}}{R_{4}}=\frac{R}{R}+\frac{C}{C}=1+1=2
\end{aligned}
$$



Figure 7-8 Wien-bridge oscillator with an amplifier

The Wien-bridge oscillator with an amplifier is shown in Figure 7-8.

## Advantages of Wien-Bridge Oscillator

The Wien-bridge oscillator has the following advantages:

1. The frequency of oscillation can be easily varied just by changing $R C$ network
2. High gain due to two-stage amplifier
3. Stability is high

## Disadvantages of Wien-Bridge Oscillator

The main disadvantage of the Wien-bridge oscillator is that a high frequency of oscillation cannot be generated.

## 7-4 CONDITIONS FOR OSCILLATION: BARKHAUSEN CRITERION

Earlier we established that the overall gain of a feedback amplifier is $A_{f}=A /(1+A \beta)$, where $A$ is the gain of the internal amplifier, $\beta$ is the feedback ratio, and $-A \beta$ is the loop gain. For positive feedback, the feedback gain is expressed as:

$$
\begin{equation*}
A_{f}=\frac{A}{1-A \beta} \tag{7-44}
\end{equation*}
$$

For $A \beta=1$, Equation (7-44) yields $A_{f}=\infty$. The amplifier then produces an output voltage without any externally applied input voltage. Thus, the amplifier becomes an oscillator. When the signal equals $V_{o}^{\prime} \Rightarrow A \beta V_{o}=V_{o}$ or $A \beta=1$, the output voltage regenerates itself and the amplifier oscillates. This condition is called the Barkhausen criterion. This condition means that $|A \beta|=1$ and the phase angle of $A \beta$ is zero or an integral multiple of 360 . The basic conditions for oscillation in a feedback amplifier are: (1) the feedback must be regenerative, (2) the loop-gain must be unity, and (3) the phase difference must be zero or an integral multiple of 360 .

## 7-4-1 Nyquist Criterion for Oscillation

The loop gain factor $A \beta$ is a complex quantity and it is function of frequency. In case of positive feedback, the amplifier breaks into oscillations. The system is unstable due to circuit non-linearity. The condition of instability of an amplifier is expressed by the Nyquist criterion.

In Figure $7-9, X$ is a point on the locus of $A \beta$. If $X$ is inside the circle of unit radius $(1+j 0)$, we have $|1-A \beta|<1$ and positive feedback occurs. If $X$ is outside the circle, we have $|1-A \beta|>1$ and the feedback is negative. Nyquist criterion states that if this closed curve passes through or encloses the point $(1+j 0)$, the amplifier becomes unstable and oscillates. It is important to note that a positive feedback amplifier will not oscillate unless the Nyquist criterion is satisfied.

In the steady state condition the loop gain becomes unity and the oscillations are sustained, the frequency of oscillations is controlled by the frequency-determining network of the oscillator. The RC and LC combination circuits are used in oscillators to serve as the frequency-determining network.

Let us summarize the key necessities of a feedback oscillator.

1. Amplifier with positive feedback produces a negative resistance in the system.
2. A frequency-determining network creates oscillations at certain required frequencies.
3. System non-linearity introduced by the devices contain the amplitude of oscillation.


Figure 7-9 Regions of positive and negative feedback in the complex plane


Figure 7-10 (a) Circuit diagrams of a tuned oscillator (b) ac equivalent circuit of tuned circuit

## 7-5 TUNED OSCILLATOR

The circuit diagram of a tuned oscillator is shown in Figure 7-10(a). The emitter by pass capacitor $C_{E}$ shunts the ac so that $R_{E}$ is omitted from the ac equivalent circuit of Figure 7-10(b). The dc operating point of the transistor is determined by the resistances $R_{1}, R_{2}$ and $R_{E}$, and supply voltage. The transistor gives a phase-shift of $180^{\circ}$.

## 7-5-1 Circuit Analysis

The frequency of oscillation is approximately given by the natural resonant frequency of the $L C$ tank circuit. Thus:

$$
\begin{equation*}
f=\frac{1}{2 \pi \sqrt{L C}} \tag{7-45}
\end{equation*}
$$

The resistance $R$ of the transformer primary is small at resonance; the resistance is:

$$
\begin{equation*}
R_{T}=\frac{L}{C R} \tag{7-46}
\end{equation*}
$$

From the $h$-parameter ac equivalent circuit of Figure 7-10(b), we obtain:

$$
\begin{equation*}
V_{2}=-I_{2} R_{T}=-\frac{I_{2} L}{C R} \tag{7-47}
\end{equation*}
$$

Upon application of KCL at the point we have:

$$
\begin{equation*}
I_{2}=h_{o e} V_{2}+h_{f e} I_{1} \tag{7-48}
\end{equation*}
$$

Substituting for $V_{2}$ from Equation (7-47) into Equation (7-48), we have:

$$
\begin{gather*}
I_{2}=-\frac{I_{2} L}{C R} h_{o e}+h_{f e} I_{1} \\
\text { or, } \quad I_{2}\left(1+h_{o e} \frac{L}{C R}\right)=h_{f e} I_{1}
\end{gather*}
$$

If M is the mutual inductance, then the voltage in the transformer secondary is $j \omega M I_{p^{\prime}} I_{P}$ is the primary current. The secondary circuit impedance is $R_{B}+h_{i e}$. Applying Kirchhoff's voltage law in the secondary circuit, we obtain:
or,

$$
\begin{equation*}
I_{1}=\frac{j \omega M I_{p}-h_{r e} V_{2}}{R_{B}+h_{i e}} \tag{7-50}
\end{equation*}
$$

From Figure 7-10(b), we also obtain:

$$
\begin{equation*}
I_{p}=\frac{1 /(j \omega C)}{R+j \omega L+\frac{1}{j \omega C}} I_{2} \tag{7-51}
\end{equation*}
$$

Substituting $I_{p}$ and $V_{2}$ from Equations (7-51) and (7-47), in Equation (7-50) yields:

$$
\begin{equation*}
I_{1}=\frac{\left(\frac{\omega^{2} M L}{R}+\frac{h_{r e} L}{C R}\right) I_{2}}{R_{B}+h_{i e}} \tag{7-52}
\end{equation*}
$$

Putting this value of $I_{1}$ in Equation (7-52) gives:

$$
\begin{equation*}
1+h_{o e} \frac{L}{C R}=\frac{h_{f e}}{R_{B}+h_{i e}}\left(\omega^{2} M+\frac{h_{r e}}{C}\right) \frac{L}{R} \tag{7-53}
\end{equation*}
$$

Substituting $\omega=1 / \sqrt{L C}$ in Equation (7-53) we get:

$$
\begin{equation*}
M=\frac{R_{B}}{h_{f e}}\left(C R+h_{o e} L\right)+C R \frac{h_{i e}}{h_{f e}}+L \frac{\left(h_{i e} h_{o e}-h_{f e} h_{r e}\right)}{h_{f e}} \tag{7-54}
\end{equation*}
$$

The value of M is used to calculate the condition for sustained oscillation.

## 7-6 CRYSTAL OSCILLATOR

Crystal oscillator is most commonly used oscillator with high-frequency stability. Crystal oscillators are used for laboratory experiments, communication circuits and biomedical instruments. Crystal oscillators are usually, fixed frequency oscillators where stability and accuracy are the primary considerations. In order to design a stable and accurate LC oscillator for the upper HF and higher frequencies it is absolutely necessary to have a crystal control; hence, the reason for crystal oscillators. Crystal oscillators are oscillators where the primary frequency determining element is a quartz crystal. Because of the inherent characteristics of the quartz crystal the crystal oscillator may be held to extreme accuracy of frequency stability. Temperature compensation may be applied to crystal oscillators to improve thermal stability of the crystal oscillator. Crystal oscillators are usually, fixed frequency oscillators where stability and accuracy are the primary considerations. A typical crystal oscillator is shown in Figure 7-11(a). A series LCR circuit shunted by a capacitor $C^{\prime}$, as shown in Figure 7-11(a), represents the equivalent circuit of a piezoelectric crystal, shown in Figure 7-11(a). The crystal size and cut determine the values of $L, C, R$ and $C^{\prime}$. The resistance $R$ is the friction of


Figure 7-11 (a) Symbol of a vibrating piezoelectric crystal
(b) Its equivalent electrical circuit
the vibrating crystal, capacitance $C$ is the compliance, and inductance $L$ is the equivalent mass. The capacitance $C^{\prime}$ is the electrostatic capacitance between the mounted pair of electrodes with the crystal as the dielectric.

The circuit of Figure 7-11(b) has two resonant frequencies. At the series resonant frequency $f_{\mathrm{s}}$ the reactance of the series $L C$ arm is zero, that is:

$$
\begin{align*}
\omega_{s} L-\frac{1}{\omega_{s} C} & =0 \\
\text { or, } \quad \omega_{s} & =\frac{1}{\sqrt{L C}} \tag{7-55}
\end{align*}
$$

$\omega_{p}$ is the parallel resonant frequency of the circuit greater than $\omega_{s}$, where:

$$
\begin{align*}
& \left.\begin{array}{rl}
\left(\omega_{p} L-\frac{1}{\omega_{p} C}\right.
\end{array}\right) & =\frac{1}{\omega_{p} C^{\prime}} \\
\text { or, } & \omega_{p}^{2} & =\frac{1}{2}\left(\frac{1}{C}+\frac{1}{C^{\prime}}\right) \\
\text { or, } & \omega_{p} & =\sqrt{\frac{1}{2}\left(\frac{1}{C}+\frac{1}{C^{\prime}}\right)} \tag{7-56}
\end{align*}
$$

Therefore, $\omega_{p}$ and $\omega_{\mathrm{s}}$ are as shown in Figure 7-12. At the parallel, resonant frequency, the impedance offered by the crystal to the internal circuit is very high.

The resonant frequencies of a crystal vary inversely as the thickness of the cut.

$$
f=\frac{1}{t}
$$

Crystal oscillators are generally used in the frequency range from about 10 kHz to 10 MHz . For lower frequencies, the size of the quartz crystal is inconveniently large. At higher frequencies, the thickness of the crystal is so small that it becomes very much fragile. The actual circuit diagram of the crystal oscillator is shown in Figure 7-13.


Figure 7-13 Circuit of a crystal oscillator

## Solved Examples

Example 7-1 Find the operating frequency of the transistor of a Colpitts oscillator if $C_{1}=0.001 \mu \mathrm{~F}, C_{2}=0.01 \mu \mathrm{~F}$ and $L=15 \mu \mathrm{H}$.

## Solution:

For Colpitts oscillator:

$$
\begin{aligned}
f & =\frac{1}{2 \pi \sqrt{C_{T} L}} \\
\Theta C_{T} & =\frac{C_{1} \times C_{2}}{C_{1}+C_{2}} \\
& =\frac{0.01 \times 0.001 \times 10^{-6} \times 10^{-6}}{(0.01+0.001) \times 10^{-6}} \\
C_{T} & =909.09 \times 10^{-12} \mathrm{~F} \\
\therefore \quad & f=\frac{1}{2 \pi \sqrt{909.09 \times 10^{-12} \times 15 \times 10^{-6}}}=\frac{10^{9}}{2 \pi \sqrt{909.09}} \\
\therefore \quad & f=1.36 \mathrm{MHz}
\end{aligned}
$$

Example 7-2 A crystal has a thicknes reduced by 1\%. What happens to the oscillations?

## Solution:

Frequency, $f=\frac{K}{t}$

$$
\therefore \quad f \alpha \frac{1}{t}
$$

If the of the crystal is reduced by $1 \%$, the frequency of oscillations will increase by $1 \%$.

Example 7-3 The ac equivalent circuit of a crystal has these values: $L=1 \mathrm{H}, C=0.01 \mathrm{pF}$, $R=1000 \Omega$ and $C_{m}=20 \mathrm{pF}$. Calculate $f_{S}$ and $f_{P}$ of the crystal.

## Solution:

Given:

$$
L=1 \mathrm{H}, C=0.01 \mathrm{pF}, R=1000 \Omega, C_{m}=20 \mathrm{pF}
$$

For series resonance:

$$
\begin{array}{ll} 
& f_{S}=\frac{1}{2 \pi \sqrt{L C}}=\frac{1}{2 \pi \mathrm{R} 1 \times 0.01 \times 10^{-12}} \\
\therefore \quad f_{S}=1.59 \mathrm{mHz}
\end{array}
$$

For parallel resonance:

$$
\begin{aligned}
& f_{P}=\frac{1}{2 \pi \sqrt{L . C_{T}}} \\
& C_{T}=\frac{C \times C_{m}}{C+C_{m}}=\frac{0.01 \times 20 \times 10^{-24}}{(0.01+20) \times 10^{-12}} \\
& C_{T}=0.009995 \times 10^{-12} \mathrm{~F} \\
& f_{p}=\frac{1}{2 \pi \sqrt{0.009995 \times 10^{-12} \times 1}} \\
& \therefore \quad f_{p}=1.592 \mathrm{MHz}
\end{aligned}
$$

If this crystal is used in an oscillator, the frequency of oscillations will be between 1.59 and 1.592 MHz .

Example 7-4 Calculate the value of $\beta$ in order for oscillation to occur if $A=30$ and the amplification with feedback.

## Solution:

According to Barkhausen criteria:

$$
\begin{array}{ll} 
& A \beta=1 \\
\because & A=30 \\
\therefore & \beta=\frac{1}{A}=\frac{1}{30} \\
\therefore & \beta=0.033
\end{array}
$$

Amplification with feedback:

$$
\begin{array}{ll} 
& A^{\prime}=\frac{A}{1-A \beta}=\frac{30}{1-30 \times 0.0333} \\
\therefore & A^{\prime}=\infty
\end{array}
$$

The amplification with feedback becomes infinite and it should be controlled by non-linearity.

Example 7-5 A Clapp oscillator has the following circuit components $C_{1}=10000 \mathrm{pF}, C_{2}=1000 \mathrm{pF}$, $L_{3}=50 \mu \mathrm{H}$ and $C_{3}$ is $5-150 \mathrm{pF}$, variable capacity. Find the tuning frequency range and minimum gain for oscillation.

## Solution:

Frequency of oscillation is by:

$$
\begin{gathered}
f_{o}=\frac{1}{2 \pi \sqrt{L_{3} C_{e q}}} \\
C_{e q}=\frac{C_{1} \times C_{2} \times C_{3}}{C_{1} C_{2}+C_{2} C_{3}+C_{1} C_{3}}
\end{gathered}
$$



For $C_{3}=5 \mathrm{pF}$

$$
\begin{aligned}
& C_{e q 1} & =\frac{10000 \times 1000 \times 5}{10000 \times 1000+1000 \times 5+5 \times 10000} \\
& \therefore \quad \mathrm{C}_{e q 1} & =4.97 \mathrm{pF} \\
& f_{o 1} & =\frac{1}{2 \pi \sqrt{50 \times 10^{-6} \times 4.97 \times 10^{-12}}} \\
\therefore & f_{o 1} & =10.096 \mathrm{MHz}
\end{aligned}
$$

For $C_{3}=150 \mathrm{pF}$

$$
\begin{array}{ll} 
& C_{e q 2}=\frac{10000 \times 1000 \times 150}{10000 \times 1000+150 \times 1000+10000 \times 150} \\
\therefore \quad & C_{e q 2}=128.75 \mathrm{pF} \\
& f_{o 2}=\frac{1}{2 \pi \sqrt{50 \times 10^{-6} \times 128.75 \times 10^{-12}}} \\
\therefore \quad & f_{o 2}=1.98 \mathrm{MHz}
\end{array}
$$

$\therefore$ The tuning range of capacitor is from 1.98 to 10.096 MHz .
For minimum range for oscillation:

$$
\begin{array}{cc} 
& A \beta=1 \\
& A_{\text {loop }} \geq 1 \\
\therefore \quad & A_{\text {loop }}=A_{v o} \times \frac{C_{2}}{C_{1}}=\frac{10000}{1000} \\
\therefore \quad A_{v o}=10
\end{array}
$$

Example 7-6 A Hartley oscillator uses a FEET with $g_{m}$ of 3 ms and $r_{d}=20 \mathrm{k} \Omega$. The total coil inductance $C_{e}$ is $20 \mu \mathrm{H}$ with a turns ratio of input side to output side of $1: 10$. It is turned with a 20 pF capacitor. Find the frequency of oscillation and the amplifier gain margin in dB .

## Solution:

For Hartley oscillator:

$$
f_{o}=\frac{1}{2 p \sqrt{L_{T} \cdot L_{3}}}=\frac{1}{2 \pi \sqrt{20 \times 10^{-6} \times 20 \times 10^{-12}}}
$$

$\therefore$ Frequency of oscillation:

$$
f_{o}=7.95 \mathrm{MHz}
$$

$$
\mu=g_{m} r_{d}=3 \times 10^{-3} \times 20 \times 10^{3}=60
$$

For oscillation:

$$
\begin{gathered}
A_{\text {loop }}=\mu \times \frac{\mathrm{N}_{1}}{\mathrm{~N}_{2}}=60 \times \frac{1}{10}=6 \\
20 \log 6=15.56 \mathrm{~dB}
\end{gathered}
$$

$\therefore$ Excess gain

Example 7-7 Prove that in a crystal the ratio of frequencies in series and parallel resonance is given by:

$$
1+\frac{1}{2} \times \frac{C}{C^{\prime}}
$$

## Solution:

The equivalent circuit is as shown in the given diagram.
For series resonance:

$$
w_{1}^{2}=\frac{1}{L C}
$$

For parallel resonance:

$$
\begin{array}{ll}
w_{2}^{2} & =\frac{1}{C_{e q} \times L} \\
C_{e q} & =\frac{C \times C^{\prime}}{C+C^{\prime}} \\
\therefore \quad & \frac{\omega_{2}^{2}}{\omega_{1}^{2}}=\frac{1}{C_{e q} L} \times \frac{L C}{1} \\
\therefore \quad & \frac{\omega_{2}^{2}}{\omega_{1}^{2}}=\frac{C+C^{\prime}}{L \times C \times C^{\prime}} \times \frac{L C}{1}=1+\frac{C}{C^{\prime}} \\
\therefore \quad & \frac{\omega_{2}}{\omega_{1}}=\sqrt{1+\frac{C}{C^{\prime}}}=\left(1+\frac{C}{C^{\prime}}\right)^{1 / 2}
\end{array}
$$



On expanding and neglecting higher powers:

$$
\therefore \quad \frac{\omega_{2}}{\omega_{1}}=1+\frac{1}{2} \times \frac{C}{C^{\prime}}(\text { Proved })
$$

Example 7-8 Find the value of $R^{\prime}$ in the circuit of the figure for generally sinusoidal oscillations. Find the frequency of oscillations.


## Solution:

At node $a$ :

$$
\begin{align*}
& \frac{V_{a}}{R}+\frac{V_{a}-V_{c}}{R^{\prime}}=0 \\
& V_{c}=V_{a}\left(1+\frac{R^{\prime}}{R}\right) \tag{1}
\end{align*}
$$

At node $b$ :

$$
\begin{gather*}
V_{a}=V_{b} \\
V_{c}=V_{b}\left(1+\frac{R^{\prime}}{R}\right)  \tag{2}\\
0-\left(V_{b}\right) D C+\frac{V_{b}-V_{d}}{R}=0 \\
V_{b}(1+S C R)=V_{d} \tag{3}
\end{gather*}
$$

At node $d$ :

$$
\begin{gather*}
\left(V_{d}-V_{c}\right) S C+\frac{V_{d}}{R}+\frac{\left(V_{d}-V_{b}\right)}{R}=0 \\
V_{d}(2+S C R)=V_{c}(\mathrm{SCR})+V_{b} \tag{4}
\end{gather*}
$$

From Equations (2), (3) and (4):

$$
\begin{gathered}
V_{b}(1-S C R)(2+S C R)=V_{b}\left(1+\frac{R^{\prime}}{R}\right)(S C R)-V_{b} \\
2-3 S C R+S^{2} C^{2} R^{2}-\left(1+\frac{R^{\prime}}{R}\right)(S C R)-1=0 \\
1+S^{2} C^{2} R^{2}+\left(2-\frac{R^{\prime}}{R}\right)(S C R)=0
\end{gathered}
$$

For oscillation:

$$
R^{\prime}=2 R, \omega=\frac{1}{C R}
$$

Example 7-9 In a Wien-bridge oscillator, the capacitors are of the variable type. The maximum and minimum values of capacitance are 900 pF and 90 pF respectively. The value of $R=100 \mathrm{k} \Omega$.
(a) Determine the range of the operating frequency of the oscillator.
(b) Determine the value of $R_{3}$ if $R_{4}=10 \mathrm{k} \Omega$, so that oscillation can be maintained.

## Solution:

(a) The frequency of oscillation is given by:

$$
f_{o}=\frac{1}{2 \pi R C}
$$

The capacitor $C$ is variable, $C_{\text {maximum }}=900 \mathrm{pF}$ and $C_{\text {minimum }}=90 \mathrm{pF}$. When the $C$ is the minimum, we get the maximum frequency, and:


$$
\begin{aligned}
f_{o \text { maximum }} & =\frac{1}{2 \pi R C_{\text {minimum }}} \\
& =\frac{1}{2 \pi 100 \mathrm{k} \times 90 \mathrm{pF}}=17.68 \mathrm{KHz}
\end{aligned}
$$

When the $C$ is the maximum, we get the minimum frequency as:

$$
\begin{aligned}
f_{o \text { minimum }} & =\frac{1}{2 \pi R C_{\text {maximum }}} \\
& =\frac{1}{2 \pi 100 \mathrm{k} \times 900 \mathrm{pF}}=1.768 \mathrm{KHz}
\end{aligned}
$$

Therefore, the range of oscillation frequency is from 1.768 to 17.68 KHz .
(b) Using,

$$
\begin{aligned}
& \frac{R_{3}}{R_{3}+R_{4}} \leq \frac{1}{3} \\
& R_{3}=2 R_{4} \\
& R_{3}=2 \times 10 \mathrm{k} \Omega=20 \mathrm{k} \Omega
\end{aligned}
$$

Example 7-10 Find the minimum voltage gain and the frequency of oscillation for a Colpitts oscillator with $C_{1}=0.004 \mu \mathrm{~F}, C_{2}=0.003 \mu \mathrm{~F}$ and $L=4.0 \mathrm{mH}$.

## Solution:

$$
\begin{gathered}
A_{v} \geq \frac{C_{2}}{C_{1}} \\
A_{v} \geq \frac{0.03 \times 10^{-6}}{0.04 \times 10^{-6}} \geq 7.5
\end{gathered}
$$

so,

$$
\begin{aligned}
2 \pi f_{o} & =\sqrt{\frac{C_{1}+C_{2}}{L C_{1} C_{2}}} \\
f_{o} & =\frac{1}{2 \pi} \sqrt{\frac{0.004 \times 10^{-6}+0.003 \times 10^{-6}}{\left(4 \times 10^{-3}\right)\left(0.004 \times 10^{-6}\right)\left(0.003 \times 10^{-6}\right)}} \\
& =\frac{1}{2 \pi} \sqrt{7.08 \times 10^{10}}=42.4 \times 10^{3} \mathrm{~Hz}=42.4 \mathrm{KHz}
\end{aligned}
$$

Example 7-11 A transistor LC oscillator circuit is as shown in the following diagram. Assume that the transistor has very high impedance. Derive an equation governing the circuit operation and find the frequency of oscillation. Also state the gain condition required for oscillations to start.

## Solution:

$$
\begin{gathered}
Z_{1}=\frac{1}{j \omega C_{1}}=\frac{-j}{\omega C_{1}} \\
Z_{2}=\frac{1}{j \omega C_{2}}=\frac{-j}{\omega C_{2}} \\
Z_{3}=j \omega L_{1} \\
\frac{-1+h_{f e}}{\omega^{2} C_{1} C_{2}}+j \omega\left[L_{1}-\frac{1}{\omega^{2}}\left(\frac{1}{C_{1}}+\frac{1}{C_{2}}\right)\right] h_{f e}+\frac{L_{1}}{C_{2}}=0 \\
\omega^{2} L_{1}=\frac{1}{C_{1}}=\frac{1}{C_{2}}=\frac{C_{1}+C_{2}}{C_{1} C_{2}} \\
X_{C}^{2}=\frac{C_{1}+C_{2}}{L_{1} C_{1} C_{2}}
\end{gathered}
$$

$$
\begin{gathered}
1+h_{f e}-\frac{1}{\omega_{0}^{2} C_{1} C_{2}+\frac{L_{1}}{C_{2}}}=0 \\
\left(1+h_{f e}\right)=\omega^{2} C_{1} L_{1}=\frac{C_{1}+C}{C_{1} C_{2}} C_{1} \\
h_{f e}=\frac{C_{1}}{C_{2}} \text { (condition of oscillation) }
\end{gathered}
$$

Example 7-12 A Hartley oscillator, as shown in the following diagram, has the circuit parameters: $L_{1}=500 \mu \mathrm{H}, L_{2}=5000 \mu \mathrm{H}, \mathrm{M}=300 \mu \mathrm{H}$ and $C=150 \mathrm{pF}$.
(a) Determine the frequency of oscillation.
(b) If the transistor has the following parameters, determine whether the circuit will oscillate or not.
Given: $R_{L}=10 \mathrm{k} \Omega, g_{m}=8 \mathrm{~mA} / \mathrm{V}, r_{o}=50 \mathrm{k} \Omega$.

## Solution:

(a) Frequency of oscillation:

$$
\begin{aligned}
f_{o} & =\frac{1}{2 \pi \sqrt{L_{T} C}} \\
L_{T} & =L_{1}+L_{2}+2 M \\
& =500 \mu \mathrm{H}+5000 \mu \mathrm{H}+2 \times 300 \mu \mathrm{H}=6.1 \mathrm{mH}
\end{aligned}
$$

and,

$$
\begin{aligned}
& C=150 \mathrm{pF} \\
& \qquad f_{o}=\frac{1}{2 \pi \sqrt{6.1 \mathrm{mH} \times 150 \mathrm{pF}}}=166.4 \mathrm{KHz}
\end{aligned}
$$

The voltage gain using the approximate formula is:

$$
A_{v}=-g_{m} R_{L}^{\prime}
$$

(b) The effective

$$
\begin{aligned}
R_{L}^{\prime} & =\mathrm{R}_{\mathrm{L}}\left\|r_{o}=10 \mathrm{k} \Omega\right\| 50 \mathrm{k} \Omega=8.33 \mathrm{k} \Omega \\
A_{v} & =-8 \mathrm{~mA} / \mathrm{V} \times 8.33 \mathrm{k} \Omega=-66.64 \\
\left|A_{v}\right| & =66.64
\end{aligned}
$$

From the equation:

$$
\frac{N_{2}}{N_{1}}=\frac{L_{2}+M}{\mathrm{~L}_{1}+M}=\frac{500 \mu \mathrm{H}+300 \mu \mathrm{H}}{500 \mu \mathrm{H}+300 \mu \mathrm{H}}=6.625
$$

Therefore, the condition for maintaining sustained oscillation is given by:

$$
\begin{gathered}
A_{v} \frac{N_{2}}{N_{1}} \geq 1 \\
\left|A_{v}\right| \frac{N_{2}}{N_{1}}=66.64 \times 6.625=441.5, \text { which is much larger than } 1 .
\end{gathered}
$$

Hence, the circuit will oscillate.
Example 7-13 A piezo-oscillator has the following circuit and the device parameters: $C_{g s}=5 \mathrm{pF}$ $C_{d s}=1 \mathrm{pF}, \mathrm{gm}=10 \mathrm{~mA} / \mathrm{V}, r_{d}=50 \mathrm{k}$ and REGISTER $=10 \mathrm{M}$. The crystal parameters are $L=0.5 \mathrm{H}$, $C_{2}=0.05 \mathrm{pF}, R_{s e}=1 \mathrm{~K}$ and $C_{1}=1 \mathrm{pF}$. Find:
(a) The equivalent series-resonant capacitance $C_{r}$
(b) The frequency of oscillations $f$
(c) The series and the parallel resonant frequencies $f_{S}$ and $f_{P}$, and $Q$ of the crystal
(d) The loop gain AB at zero bias
(e) The bias time constant


## Solution:

(a) From the figure, we obtain the total capacitance $C_{T}$ in series with $L$ as:

$$
\begin{aligned}
C_{T} & =C_{2}\left[C_{1} \|\left(C_{d s} \text { in series with } C_{g s}\right)\right] \\
& =\frac{1}{\frac{1}{0.05}+\frac{1}{1+\left(\frac{1 \times 5}{1+5}\right)}}=0.049 \mathrm{pF}
\end{aligned}
$$

(b) The series resonant frequency of the Clapp oscillator like the piezo-oscillator is:

$$
f_{o}=\frac{\sqrt{2}}{2 \pi \sqrt{L C_{T}}}=\frac{\sqrt{2}}{2 \pi \sqrt{0.5 \times 0.049 \times 10^{-12}}}=1.017 \mathrm{MHz}
$$

(c) Parallel resonant frequency:

$$
\begin{gathered}
\omega_{p}=\frac{1}{\left(\frac{L C_{1} C_{2}}{C_{1}+C_{2}}\right)^{1 / 2}} \\
f_{p}=\frac{1}{2 \pi\left(\frac{0.5 \times 10^{-12} \times 0.05 \times 10^{-12}}{1 \times 10^{-12}+0.05 \times 10^{-12}}\right)^{1 / 2}}=1.3 \mathrm{MHz}
\end{gathered}
$$

Series resonant frequency:

$$
\begin{gathered}
\omega_{s}=\frac{1}{\left(L C_{2}\right)^{1 / 2}} \\
f_{s}=\frac{1}{2 \pi\left(0.5 \times 0.05 \times 10^{-12}\right)^{1 / 2}}=1.0065 \mathrm{MHz}
\end{gathered}
$$

Quality factor $Q$ of the crystal:

$$
\begin{gathered}
Q=\frac{\left(L / C_{2}\right)^{1 / 2}}{R_{s e}} \\
Q=\frac{1}{10^{3}}\left(\frac{0.5}{0.05 \times 10^{-12}}\right)^{1 / 2}=316
\end{gathered}
$$

(d) The loop-gain:

$$
A \beta=g_{m} r_{d} \frac{C_{d s}}{C_{g s}}=10 \times 10^{-3} \times 50 \times 10^{3} \times \frac{1 \mathrm{pF}}{5 \mathrm{pF}}=100
$$

(e) $T_{\text {bias }}=R_{G} C_{G}=R_{G}\left(C_{g s} \| C_{d s}\right)=10 \times 10^{6}(5-1) \times 10^{12}=60 \mu \mathrm{~s}$

$$
\frac{1}{\omega_{O}}=\frac{1}{2 \pi \times 1.017 \times 10^{6}}=0.45 \mu \mathrm{~s}
$$

Thus, $\quad T_{\text {bias }} \gg \frac{1}{\omega_{O}}$ (as required for proper operation)

Example 7-14 A Colpitts oscillator, as shown in the following diagram, has a coil with inductance of $C_{1}=100 \mathrm{pF}$ and $C_{2}=1000 \mathrm{pF}$. Find:
(a) Frequency of oscillation
(b) The minimum gain required of the amplifier to maintain oscillation

## Solution:

The frequency of oscillation is:

$$
\begin{aligned}
f_{o}=\frac{1}{2 \pi \sqrt{L_{1} C_{e q}}} \\
\begin{aligned}
L_{1}=100 \mu \mathrm{H} & =100 \times 10^{-6} \\
C_{e q} & =\frac{C_{1} \times C_{2}}{C_{1}+C_{2}}=\frac{200 \times 10^{-12} \times 1000 \times 10^{-12}}{200 \times 10^{-12}+1000 \times 10^{-12}} \\
& =166.67 \times 10^{-12} \mathrm{~F} \\
f_{o} & =\frac{1}{2 \pi \sqrt{100 \times 10^{-6} \times 166.67 \times 10^{-12}}} \\
f_{o} & =123.3 \mathrm{KHz}
\end{aligned}
\end{aligned}
$$

The minimum gain required is:

$$
\left|A_{v}\right| \geq \frac{C_{2}}{C_{1}}=\frac{1000 \mathrm{pF}}{200 \mathrm{pF}}=5
$$

Example 7-15 In the Hartley oscillator, $L_{2}=0.4 \mathrm{mH}$ and $C=0.04 \mathrm{mF}$. If the frequency of the oscillation is 120 kHz , find the value of $L_{1}$. Neglect the mutual inductance.

## Solution:

Frequency of Hartley oscillator is:

$$
\begin{gathered}
f=\frac{1}{2 \pi \sqrt{\left(L_{1}+L_{2}\right) C}} \\
L_{1}=\frac{1}{4 \pi^{2} f^{2} C}-L_{2} \\
L_{1}=\frac{1}{4 \pi^{2}\left(120 \times 10^{3}\right)^{2} \times 0.004 \times 10^{-6}}-0.4 \times 10^{-3} \\
L_{1}=0.04 \mathrm{mH}
\end{gathered}
$$

Example 7-16 A crystal has $L=0.33 \mathrm{H}, C=0.065 \mathrm{pF}$ and $C_{1}=1.0 \mathrm{pF}$ and $R=5.5 \mathrm{~K}$.
(a) Calculate the series resonant frequency.
(b) Calculate the series resonant frequency.
(c) By what percent does the parallel resonant frequency exceed the resonant frequency?
(d) Find $Q$ of the crystal.

Solution:
(a) $f_{s}=\frac{1}{2 \pi}\left(\frac{1}{L C}\right)^{\frac{1}{2}}=\frac{1}{2 \pi}\left(\frac{10^{12}}{0.33 \times 0.065}\right)^{\frac{1}{2}}=1.09 \mathrm{MHz}$
(b) $\frac{f_{p}}{f_{s}}=\left(1+\frac{C}{C_{1}}\right)^{\frac{1}{2}}=\left(1+\frac{0.065}{1.0}\right)^{\frac{1}{2}} \approx 1.033 \mathrm{MHz}$
(c) $f_{p}$ exceeds $f_{s}$ by $3.3 \%$
(d) $Q=\frac{\omega_{s} L}{R}=\frac{1}{R} \sqrt{\frac{L}{C}}=\frac{1}{5.5 \times 10^{3}}\left(\frac{0.33}{0.065 \times 10^{-12}}\right)^{\frac{1}{2}}=410$

## 7-7 REAL-LIFE APPLICATIONS

Oscillators are a common element of almost all electronic circuits. They are used in various applications, and their use makes it possible for circuits and subsystems to perform numerons useful functions. In oscillator circuits, oscillation usually builds up from zero when power is first applied under linear circuit operation. The oscillator's amplitude is kept from building up by limiting the amplifier saturation and various non-linear effects. Oscillator design and simulation is a complicated process. It is also extremely important and crucial to design a good and stable oscillator. Oscillators are commonly used in communication circuits. All the communication circuits for different modulation techniques-AM, FM, PM-the use of an oscillator is must. Add-all digital modulators use oscillators.

Oscillators frequently consist of one or two transistors, an inductor $(L)$, and a capacitor $(C)$ in an LC tank circuit, followed by a buffering amplifier. An oscillator circuit may be implemented with a tuned amplifier having positive feedback from the amplifier's output terminal to its input terminal, in which design takes advantage of the instability possible in circuits having such a feedback loop. Oscillators are used as stable frequency sources in a variety of electronic applications. Oscillator circuits are used in computer peripherals, counters, timers, calculators, phase-locked loops, digital multi-metres, oscilloscopes, and numerous other applications. An oscillator circuit may act as an active device, such as a transistor, to produce power gain-routing a sufficient amount of the active device's output signal to an input of the active device, to sustain oscillations. An oscillator circuit may be used to provide a clock signal, or to produce an accurate waveform. In communication systems, oscillators are employed to provide a stable frequency reference signal for translating information signals to a desired frequency band.

## 7-7-1 Voltage-Controlled Oscillator

A common oscillator implementation is the voltage-controlled oscillator (VCO) circuit, where an input tuning voltage is applied to an oscillator circuit and the tuning voltage adjusted to set the frequency at which the circuit oscillates. The VCO is the most widely used oscillator circuit and it produces an oscillatory output voltage. It provides a periodic signal, where the frequency of the periodic
signal is related to the level of an input voltage control signal supplied to the VCO. A VCO is simply an oscillator having a frequency output that is proportional to an applied voltage.

VCOs are the basic building blocks of many electronic systems especially phase-locked loops and may be found in computer disk drives, wireless electronic equipment such as cellular telephones, and other systems in which oscillation frequency is controlled by an applied tuning voltage. The centre frequency of a VCO is the frequency of the periodic output signal formed by the VCO when the input control voltage is set to a nominal level. The VCO has a characteristic gain, which often is expressed as a ratio of the VCO output frequency to the VCO input voltage. VCO typically utilizes a variable control voltage input to produce a frequency output. A VCO is capable of varying an oscillating frequency in response to a change in control voltages. The VCO in an integrated circuit comprises of a monolithic amplifier section with a resonant circuit external to the amplifier or a fully integrated solid state device, such as a ring oscillator, that does not include a resonator with reactive components. VCOs often have a tuning stub that is used to fine-tune the frequency of operation of the VCO. A stub is employed to establish the frequency of operation of the VCO.

In some VCOs, a varactor diode is employed since the space-charge capacitance of the varactor changes as a function of control voltage, thus changing the capacitance of the tank circuit. Ring-type oscillator is one type of VCO.

VCOs are used in many applications to produce an oscillating signal having a frequency defined by an input voltage. A VCO is a critical component in almost every digital communications systems. VCOs are often used to generate local oscillator $(L O)$ signals, which are used by transmitter and receiver subsystems for frequency up-conversion and down-conversion, respectively. In cellular telephone applications, VCOs are used to establish a channel frequency within one or two bands according to the GSM digital telephone standard. In order to provide local oscillator signals, as well as transmit carriers, tunable VCOs are implemented in a frequency synthesizer application. The VCO is an important building block in phase-locked loops, clock recovery circuits, and frequency synthesizers. High-frequency and radio-frequency (RF) VCOs can be implemented monolithically as LC oscillators, as relaxation oscillators and ring oscillators. Some applications require the VCO to rapidly change the carrier frequency. These types of oscillators are referred to as agile VCOs. VCOs are utilized within many synthesizer and tuner circuits, such as those found in TVs and in wireless communication devices.

## 7-7-2 Cascode Crystal Oscillator

The cascode crystal oscillator is composed of a Colpitts crystal oscillator and a base-common buffer amplifier in mobile circuits. In the cascode crystal oscillator, a temparature-independent voltage source biases the buffer amplifier and the bypass capaciter gets eliminated. GSM phones, set-top boxes and digital audio broadcasting equipments use oscillators. and digital audio broadcasting equipment use oscillators. VCOs are used in wireless modems, coaxial cables, voltage regulators, wireless speakers, RF and microwave attenuators, cordless phones, integrated electronic circuits, frequency converters, computer motherboards, thin-film capacitors, wireless routers, cell phone batteries, printed circuit boards (PCB), RF power amplifiers, two-way radios, membrane switches, wireless access points, microprocessors, radio-frequency modulators, wireless keyboards, electronic doors, network analyzers, microcontroller, bandpass filters, crystal oscillators, GPS car navigation systems, cable modems, spectrum analyzers, flexible printed circuits (FPC), TV antennae, field-effect transistors, sound cards, power dividers/combiners, variable resistors, GPS antennae, car remote control, network
processors, RFID reader, DIP switches, satellite phones, BNC connectors, graphics processors, video cards, MEMs, PIN diodes, SAW filters, digital potentiometers, SMA connectors, PCMCIA PC cards, pulse generators, vacuum circuit breakers, digital-to-analog converters, memory cards, compact flash, memory stick, SD cards, PCB connectors, Real time clocks (RTC), wireless telemetry systems, field programmable gate array (FPGA), low-noise amplifiers (LNA), Magnetic resonance imaging (MRI) systems, embedded computer systems, electrical fuses, phase-locked loop (PLL), remote keyless entry systems, Schottky diode, tire pressure monitoring systems (TPMS), programmable logic controller (PLC), system on chip (SOC), RF directional couplers, wireless headphones, earphones, variable capacitors (varactor), overload relay, phase shifter, application specific integrated circuits (ASIC), EMI shielding solutions, air circuit breakers, electronic circuit design, RF transmitter modules, dielectric resonators, precision resistors, PCB assembly, fabrication, microstrip patch antennae, miniature circuit breakers, digital delay generators, ground fault circuit interrupters (GFCI), etc.

## POINTS TO REMEMBER

1. Oscillator converts de to ac.
2. Oscillator has no input signal.
3. Oscillator behaviour is opposite to that of a rectifier.
4. The conditions and frequencies of oscillation are classified as:

| Types of Oscillation | Condition of Oscillator | Frequency of Oscillation |
| :--- | :--- | :--- |
| Hartley Oscillator | $h_{f}=\frac{\omega L_{1}}{\omega L_{2}}+\frac{R h_{i}}{\omega^{2} L_{1} L_{2}}$ | $f=\frac{\omega}{2 \pi}=\frac{1}{2 \pi} \frac{1}{\left[\left(h_{o e} L_{1} L_{2} I h_{i e}\right)+C\left(L_{1}+L_{2}\right)\right]^{1 / 2}}$ |
|  | Simply,  <br> $f=\frac{1}{2 \pi \sqrt{C\left(L_{1}+L_{2}\right)}}=\frac{1}{2 \pi \sqrt{L C^{\prime}}}$  <br> Colpitts Oscillator $h_{f}=\frac{C_{2}}{C_{1}}+R h_{i} \cdot \omega^{2} C_{1} C_{2}$ | $f=\frac{\omega}{2 \pi}=\frac{1}{2 \pi}\left(\frac{h_{o e}}{h_{i e} C_{1} C_{2}}+\frac{1}{L C_{1}}+\frac{1}{L C_{2}}\right)^{1 / 2}$ |
| Phase-Shift <br> Oscillator | The transistor should have <br> an $h_{f e}$ of 56 when $R L=R$. | $f=\frac{1}{2 \pi \sqrt{10} C R}$ |
| Wein-Bridge <br> Oscillator | $\frac{R_{1}}{R_{2}}=2$ | $f=\frac{\omega}{2 \pi}=\frac{1}{2 \pi R C}$ |
| Crystal Oscillator | - | $f_{p}=\frac{\omega_{P}}{2 \pi}=\frac{1}{2 \pi} \sqrt{\frac{C+C^{\prime}}{L C C^{\prime}}}$ |

## IMPORTANT FORMULAE

1. General condition for oscillation for an oscillator:

$$
h_{f}=\frac{x_{1}}{x_{2}}+\frac{R_{h i}}{x_{1} x_{2}}
$$

2. Frequency of oscillation for a Hartley oscillator:

$$
f=\frac{1}{2 \pi} \sqrt{C\left(L_{1}+L_{2}\right)}
$$

3. Condition for oscillation for a Colpitts oscillator:

$$
h_{f}=\frac{\mathrm{C}_{2}}{\mathrm{C}_{1}}+R h_{i} \omega^{2} C_{1} C_{2}
$$

4. Frequency of oscillation for a phase-shift oscillator:

$$
f=\frac{1}{2 \pi \sqrt{10} C R}
$$

5. Frequency of oscillation for a Wien-bridge oscillator:

$$
f=\frac{1}{2 \pi C R}
$$

6. If the feedback signal aids the externally applied input signal, the overall gain is given by:

$$
A f=\frac{A}{1-A \beta}
$$

7. Value of $M$ required for sustained oscillations is given by:

$$
M=\frac{R_{B}}{h_{f e}}\left(C R+h_{o e} L\right)+C R \frac{h_{i e}}{h_{f e}}+L \frac{\Delta_{h e}}{h_{f e}}
$$

8. Oscillation frequency of a Clapp oscillator is given by:

$$
f_{o}=\frac{1}{2 \pi} \sqrt{\frac{1}{L}\left(\frac{1}{C_{o}}+\frac{1}{C_{1}}+\frac{1}{C_{2}}\right)}
$$

9. Condition for sustained oscillation for a phase-shift oscillator is given by:

$$
h_{f e}=23+29 \frac{R}{R_{L}}+4 \frac{R_{L}}{R}
$$

## OBJECTIVE QUESTIONS

1. A distorted sinusoid has the amplitudes $A_{1}$, $A_{2}, A_{3}$-of the fundamental, second harmonic and third harmonic-respectively. The total harmonic distortion is:
(a) $\left(A_{2}+A_{3}+\cdots\right) / A_{1}$
(b) $\sqrt{A_{2}^{2}+A_{3}^{2}+\cdots / A_{1}}$
(c) $\sqrt{\left(A_{2}^{2}+A_{3}^{2}+\ldots\right) /\left(\sqrt{A_{1}^{2}+A_{2}^{2}+A_{2}^{3}+\ldots}\right)}$
(d) $1-\left(\sqrt{A_{2}^{2}+A_{3}^{2}+\cdots / A_{1}}\right)$
2. An amplifier is assumed to have a single-pole high-frequency transfer function. The rise time of its output response to a step function input is 35 nsec . The upper 3 dB frequency (in MHz ) for the amplifier to a sinusoidal input is approximately at:
(a) 4.55
(b) 10
(c) 20
(d) 28.6
3. Frequency of oscillation of a Wein-bridge oscillator is given by:
(a) $1 / 6 \pi R C$
(b) $1 / 2 \pi R C$
(c) $2 \pi R C$
(d) $1 / \pi R C$
4. Which of the following is not true?
(a) An oscillator is a circuit that converts dc to ac.
(b) An oscillator is an amplifier that supplies it own input signal.
(c) All oscillators generate sine wave.
(d) In-phase feedback is called positive feedback.
5. What do phase-shift oscillators, twin-T oscillator and Wein-bridge oscillators have in common?
(a) They use $R C$ frequency control
(b) They have a sinusoidal output
(c) They use amplifier gain to overcome feedback loss
(d) All of the above
6. The stability of frequency of oscillation is high if:
(a) $\frac{d \phi}{d t}=0$
(b) $\frac{d \phi}{d t}=\infty$
(c) $\frac{d \phi}{d}=0$
(d) $\frac{d \phi}{d w}=\infty$
7. Match List I with List II and select the correct answer using the codes as provided.

## List I

(Oscillator)
(a) Wein-bridge
(b) Colpitts
(c) Hartley
(d) Clapp

## List II

(Characteristics/Features)

1. RF oscillator; two inductances and one capacitance in the reactance network
2. LC oscillator for RF; three capacitances and one inductance in the reactance network.
3. RC oscillator for audio-frequency applications.
4. RF oscillator; two capacitances and one inductance in the reactance network.
(c) a b c d
$\begin{array}{llll}3 & 4 & 1 & 2\end{array}$
(d) a b c d
$\begin{array}{llll}3 & 1 & 4 & 2\end{array}$
5. The primary advantage of a crystal oscillator is that:
(a) It can oscillate at any frequency
(b) It gives a high output voltage
(c) Its frequency of oscillation remains almost constant
(d) It operates on a very low dc supply voltage
6. A Hartley oscillator circuit uses:
(a) A tapped inductor
(b) A tapped capacitor
(c) Both the above
(d) A tapped inductor for inductive feedback
7. A Colpitts oscillator uses:
(a) A tapped inductor
(b) A tapped capacitor
(c) Both (a) and (b)
(d) None of the above
8. An oscillator circuit using a quartz crystal has:
(a) High-frequency stability
(b) Low-frequency stability
(c) Medium-frequency stability
(d) None of these
9. An oscillator is basically an amplifier with:
(a) Zero gain
(b) Very large gain
(c) Infinite gain
(d) Very low gain
10. In a feedback oscillator, constant amplitude oscillation are obtained when loop loop gain $-A \beta$ equals:
(a) 0
(b) -1
(c) 1
(d) $\infty$
11. Crystal oscillator uses:
(a) Silicon crystal
(b) Germanium crystal
(c) Crystal diode
(d) Piezo-electric quartz crystal
12. Effective $Q$ of the equivalent electrical circuit of a quartz crystal is of theorder of:
(a) 200
(b) 2000
(c) 20,000
(d) $10^{5}$
13. Barkhausen criterion for sustained oscillation gives:
(a) $-A \beta=1$
(b) $A \beta=0$
(c) $A=\beta$
(d) $A=1 / \beta$
14. Quartz crystal oscillators are popularly used because of:
(a) High $Q$ and high-frequency stability
(b) Low $Q$ and high-frequency stability
(c) Low $Q$ and large output power
(d) High $Q$ and large output power
15. The crystal oscillator frequency is highly stable due to:
(a) Crystal structure
(b) High $Q$ of the crystal
(c) Vibration of the crystal
(d) Rigidity of the crystal
16. The most likely application of a crystal oscillator is:
(a) As an RF test oscillator
(b) As an electronic organ for home use
(c) As a hi-fi test audio-frequency sweep generator
(d) In commercial radio transmitter
17. In RC phase phase-shift oscillator using FET and 3-section RC phase phase-shift network, the condition for sustained oscillation is:
(a) $\beta>6$
(b) $\beta>29$
(c) $\beta>4 n+23+29 / n, n=R_{d} / R$
(d) $\beta>23+29 / n$
18. FET RC phase-shift oscillator has angular frequency of oscillation $\omega$ equal to:
(a) $1 / 3 R C$
(b) $1 / 6 R C$
(c) $1 / \sqrt{6} R C$
(d) $1 / \sqrt{3} R C$
where, $R$ and $C$ refer to each section of three section $R C$ phase phase-shift network.
19. In an FET Hartley oscillator, the frequency of oscillation $\omega$ :
(a) $\approx \omega_{0}$
(b) $\ll \omega_{0}$
(c) $\gg \omega_{0}$
(d) $\omega_{0}\left(L_{1} / L_{2}\right)$
where, $\omega_{0}$ is the frequency of resonance.
20. In tuned collector oscillator, frequency $f[=\omega /(2 \pi)]$ of oscillation is:
(a) $=\omega_{0}$
(b) $<\omega_{0}$
(c) $>\omega_{0}$
(d) $\omega / h_{f e}$ where, $\omega_{0}$ is frequency of resonance.
21. The feedback factor $\beta$ at frequency of oscillation of Wein-bridge oscillator is:
(a) $1 / 3$
(b) 3
(c) $1 / 29$
(d) $-1 / 29$
22. The minimum number of $R C$ sections required in phase phase-shift oscillator is:
(a) Two
(b) Three
(c) Four
(d) None
23. The current amplification factor in radian square of Colpitts oscillator is:
(a) $C_{1} / C_{2}$
(b) $C_{1} C_{2}$
(c) $C_{1}+C_{2}$
(d) $C_{1}-C_{2}$
24. Electronic oscillator is better than a mechanical one because:
(a) It has better frequency stability
(b) It has higher efficiency
(c) It can produce $20-200 \mathrm{~Hz}$
(d) None
25. Wein-bridge oscillator is most often used whenever:
(a) Wide range of high purity sine waves is to be generated
(b) High feedback ratio is needed
(c) Square output waves are required
(d) Extremely high resonant frequencies are required
26. If Barkhausen criterion is not fulfilled by an oscillator circuit, it will:
(a) Stop oscillating
(b) Produce damped waves continuously
(c) Become an amplifier
(d) Produce high-frequency whistles
27. To generate a 1 MHz signal, the most suitable circuit is:
(a) Phase-shift oscillator
(b) Wein-Bridge oscillator
(c) Colpitts oscillator
(d) None of the above
28. In oscillator circuit, the energy feedback to its input terminal from the output is:
(a) $180^{\circ}$ out of phase with input signal
(b) In phase with the input signal
(c) $90^{\circ}$ out- of- phase with the input signal
(d) None
29. For sustaining oscillations in an oscillator:
(a) Feedback factor should be unity
(b) Phase shift should be $0^{\circ}$
(c) Feedback should be negative
(d) Both (a) and (b)

## REVIEW QUESTIONS

1. What is an oscillator?
2. Classify the different types of oscillators.
3. Define Barkhausen criteria?
4. What are the basic differences between a rectifier and an oscillator?
5. What are the applications of oscillators?
6. What is the source of input of an oscillator circuit?
7. Explain the working principle of a Hartley oscillator and find its condition and frequency of oscillation.
8. Explain the working principle of a Colpitts oscillator and find its condition and frequency of oscillation.
9. Explain the working principle of phase-shift oscillator and find its condition and frequency of oscillation.
10. Explain the working principle of tuned oscillator, and find its condition and frequency of oscillation.
11. Explain the working principle of crystal oscillator, and find its condition and, frequency of oscillation.

## PRACTICE PROBLEMS

1. Find the operating frequency of a transistor in Colpitts oscillator if $C_{1}=0.002 \mu \mathrm{~F}$, $C_{2}=0.011 \mu \mathrm{~F}$ and $L=10.5 \mu \mathrm{H}$.
2. Find the operating frequency of a transistor Colpitts oscillator if $C_{1}=0.022 \mathrm{~F}$, $C_{2}=0.051 \mathrm{~F}$ and $L=20.5 \mathrm{H}$.
3. A crystal's thickness is reduced by $3 \%$. What happens to its oscillations?
4. The ac equivalent circuit of a crystal has these values: $L=1.5 \mathrm{H}, C=0.01 \mathrm{pF}$,
$R=2000 \Omega$ and $C_{m}=200 \mathrm{pF}$. Calculate $f_{S}$ and $f_{P}$ of the crystal.
5. The ac equivalent circuit of a crystal has these values: $L=1 \mathrm{H}, C=0.01 \mathrm{pF}$, $R=1000 \Omega$ and $C_{m}=20 \mathrm{pF}$. Calculate $f_{S}$ and $f_{P}$ of the crystal.
6. Calculate the value of $\beta$ in order for oscillation to occur if $A=10$ and the amplification is with feedback.
7. A Clapp oscillator has the following circuit components $C_{1}=10000 \mathrm{pF}, C_{2}=1000 \mathrm{pF}$, $L_{3}=50 \mu \mathrm{H}$ and $C_{3}$ is $5-150 \mathrm{pF}$ variable capacity. Find the tuning frequency range and minimum gain for oscillation.
8. A Hartley oscillator uses a FET with $g_{m}$ of 3 ms and $r_{d}=21.00 \mathrm{k} \Omega$. The total coil inductance $C_{e}$ is $200 \mu \mathrm{H}$ with a turns ratio of 1:10 (input side to output side). It is turned with a 20 pF capacitor. Find the frequency of oscillation and the amplifier gain margin in dB .
9. Prove that in a crystal the ratio of frequencies in series and parallel resonance is given by:

$$
1+\frac{1}{2} \times \frac{C}{C^{\prime}}
$$

10. In a Wien-bridge oscillator, the capacitors are of a variable type. The maximum and minimum values of capacitance are 1000 pF and 90 pF respectively. The value of $R=100 \mathrm{k} \Omega$.
(a) Determine the range of the operating frequency of the oscillator.
(b) Determine the value of $R_{3}$ if $R_{4}=10 \mathrm{k} \Omega$, so that oscillation can be maintained.
11. Find the minimum voltage gain and the frequency of oscillation for a Colpitts oscillator with, $C_{1}=0.004 \mu \mathrm{~F}, C_{2}=0.03 \mu F$ and $L=4.0 \mathrm{mH}$.
12. A Hartley oscillator has the following circuit parameters:

$$
\begin{aligned}
& L_{1}=500 \mu \mathrm{H}, L_{2}=5000 \mu \mathrm{M} \\
& M=300 \mu \mathrm{H} \text { and } C=150 \mathrm{pF}
\end{aligned}
$$

(a) Determine the frequency of oscillation.
(b) If the transistor has the following parameters: $R_{L}=10 \mathrm{k} \Omega, g_{m}=8 \mathrm{~mA} / \mathrm{V}$ and $r_{o}=50 \mathrm{k} \Omega$, determine whether the circuit will oscillate or not
13. A Colpitts oscillator has a coil with inductance of $C_{1}=100 \mathrm{pF}$ and $C_{2}=1000$ pF . Find (a) frequency of oscillation; (b) the minimum gain required of the amplifier to maintain oscillation.
14. A crystal has $L=0.33 \mathrm{H}, C=0.065 \mathrm{pF}$ and $C_{1}=1.0 \mathrm{pF}$ and $R=5.5 \mathrm{~K}$
(a) Find the series resonant frequency.
(b) By what percent does the parallel resonant frequency exceed the resonant frequency?
(c) Find $Q$ of the crystal.
15. In the Hartley oscillator, $L_{2}=0.4 \mathrm{mH}$ and $C=0.04 \mathrm{mF}$. If the frequency of the oscillation is 120 KHz . Find the value of $L_{1}$. Neglect the mutual inductance.

## SUGGESTED READINGS

1. Millman, Jacob and Christos C. Halkias. 1986. Integrated Electronics: Analog and Digital Circuits and Systems. New Delhi: McGraw Hill Book Company.
2. Pierret, R. F and G.W. Neudeck. 1989. Modular Series on Solid State Devices. Boston and M.A.: Addison Wesley.
3. Singh, B.P. and Rekha Singh. 2006. Electronic Devices and Integrated Circuits. New Delhi: Pearson Education.
4. Chattopadhyay, D. and P.C. Rakshit. 2008. Electronics Fundamentals and Applications. New Delhi: New Age International Publishers.

## Electronic Instruments

## Outline

8-1 Introduction
8-2 Components of the Cathode-Ray Oscilloscope
8-3 Time-Base Generators
8-4 Sweep Frequency Generator
8-5 Measurements Using the
Cathode-Ray Oscilloscope

8-6 Types of Cathode-Ray Oscilloscope<br>8-7 Cathode-Ray Tube<br>8-8 Sine Wave Generator<br>8-9 Square Wave Generator<br>8-10 AF Signal Generator<br>8-11 Function Generator

## Objectives

This chapter discusses the key instruments of electronic measurement with special emphasis on the most versatile instrument of electronic measurement-the cathode-ray oscilloscope (CRO). The objective of this book will remain unrealized without a discussion on the CRO. The chapter begins with the details of construction of the CRO, and proceeds to examine the active and passive mode input-output waveforms for filter circuits and lead-lag network delay. This will be followed by a detailed study of the dual beam CRO and its uses in op-amp circuit integrator, differentiator, inverting and non-inverting circuits, comparative waveform study, and accurate measurement with impeccable visual display. In addition to the CRO, the chapter also examines the sweep frequency generator, the function generator, the sine wave generator, the square wave generator and the AF signal generator.

## 8-1 INTRODUCTION

The cathode-ray oscilloscope (CRO) is a multipurpose display instrument used for the observation, measurement, and analysis of waveforms by plotting amplitude along $y$-axis and time along $x$-axis. CRO is generally an $x-y$ plotter; on a single screen it can display different signals applied to different channels. It can measure amplitude, frequencies and phase shift of various signals. Many physical quantities like temperature, pressure and strain can be converted into electrical signals by the use of transducers, and the signals can be displayed on the CRO. A moving luminous spot over the screen displays the signal. CROs are used to study waveforms, and other time-varying phenomena over different frequency ranges. The central unit of the oscilloscope is the cathode-ray tube (CRT), and the remaining part of the CRO consists of the circuitry required to operate the cathode-ray tube.

## 8-2 COMPONENTS OF THE CATHODE-RAY OSCILLOSCOPE

The heart of the oscilloscope, the cathode-ray tube (CRT), which generates the electron beam using the electron gun, accelerates the beam to a high velocity, deflects the beam according to the input signal and the electron beam ultimately becomes visible on the phosphor screen. The block diagram of the oscilloscope is shown in Figure 8-1. The power supply block provides the necessary voltages for the CRT to generate and accelerate


Figure 8-1 Block diagram of a cathode-ray oscilloscope the electron beam and also to supply the required operating voltages for the other circuits of the oscillo scope. Comparatively high voltages, in the order of a few thousand volts, are required by CRTs for acceleration. However, a low voltage is also required for the heater of the electron gun.

The oscilloscope has a time-base generator, which generates the accurate voltage to be supplied to the cathode-ray tube for deflecting the spot at a constant time-dependent rate. The signal to be observed is fed into a vertical amplifier, which increases the potential of the input signal to a certain level in order to provide a usable deflection of the electron beam. To summarize, the CRO consists of the following:
(i) CRT
(ii) Vertical amplifier
(iii) Delay line
(iv) Horizontal amplifier
(v) Time-base generator
(vi) Triggering circuit
(vii) Power supply

## 8-3 TIME-BASE GENERATORS

The CRO is used to display a waveform that varies as a function of time. If the wave form is to be accurately reproduced, the beam should have a constant horizontal velocity. As the beam velocity is a function of the deflecting voltage, the deflecting voltage must increase linearly with time. A voltage with such characteristics is called a ramp voltage. If the voltage decreases rapidly to zero-with the waveform repeatedly produced, as shown in Figure 8-2-we observe a pattern which is generally called a saw-tooth waveform. The time taken to return to its initial value is known as flyback or return time.

During the sweep time $T_{s}$, the beam moves from left to right across the CRT screen. Hence the beam is deflected to the right by the increasing amplitude of the ramp voltage. As the positive voltage attracts the negative electrons, during the retrace time or fly back time $T_{r}$, the beam returns quickly to the left side of the screen. The control grid is generally "gated-off", which blanks out the beam during retrace time and prevents an undesirable retrace pattern from appearing on the screen.


Figure 8-2 Typical saw-tooth waveform applied to the horizontal deflection plates

Since signals of different frequencies can be observed using the oscilloscope, the sweep rate must be regulating. We can change the sweep rate in steps by switching different capacitors in the circuit. The front panel control for this adjustment is marked, time/div or sec/div. The sweep rate can be adjusted by the variable resistor $R$, as shown in Figure8-3(a).

The circuit shown in Figure 8-3(a) is a simple sweep circuit, in which the capacitor $C$ charges through the resistor $R$. The capacitor discharges periodically through the transistor $T_{1}$, which causes the waveform shown in Figure 8-3(b) to appear across the capacitor. The signal voltage, $V_{i}$ which must be applied to the base of the transistor to turn it ON for short time intervals is also shown in Figure 8-3(b). When the transistor is completely turned ON, it presents a low-resistance discharge path, through which the capacitor discharges quickly.

If the transistor is not turned ON, the capacitor will charge exponentially to the supply voltage $V_{c c}$ according to the equation:

$$
\begin{equation*}
V_{o}=V_{c c}\left(1-\exp ^{\frac{t}{-c c}}\right) \tag{8-1}
\end{equation*}
$$

where, $V_{o}$ is the instantaneous voltage across the capacitor at time $t, V_{c c}$ is the supply voltage, $t$ is the time of interest, $R$ is the value of series resistor, and $C$ is the value of capacitor.


Figure 8-3 (a) Simple saw-tooth generator (b) Associated waveforms (c) Time-base generator using UJT

The continuous sweep CRO uses the UJT as a time-base generator. The UJT is used to produce the sweep. When power is first applied to the UJT, it is in the OFF state and $C_{T}$ changes exponentially through $R_{T}$. The UJT emitter voltage $V_{E}$ rises towards $V_{B B}$ and $V_{E}$ reaches the plate voltage $V_{P}$. The emitter-to-base diode becomes forward biased and the UJT triggers ON. This provides a low resistance discharge path and the capacitor discharges rapidly. When the emitter voltage $V_{E}$ reaches the minimum value rapidly, the UJT goes OFF. The capacitor recharges and the cycles repeat.

To improve the sweep linearity, two separate voltage supplies are used; a low voltage supply for the UJT and a high voltage supply for the $R_{T} C_{T}$ circuit. This circuit is as shown in Figure 8-3(c). $R_{T}$ is used for continuous control of frequency within a range and $C_{T}$ is varied or changed in steps. They are sometimes known as timing resistor and timing capacitor.

## 8-3-1 Oscilloscope Amplifiers

The purpose of an oscilloscope is to produce a faithful representation of the signals applied to its input terminals. Considerable attention has to be paid to the design of these amplifiers for this purpose. The oscillographic amplifiers can be classified into two major categories.
(i) AC-coupled amplifiers
(ii) DC-coupled amplifiers

The low-cost oscilloscopes generally use ac-coupled amplifiers. The ac amplifiers, used in oscilloscopes, are required for laboratory purposes. The dc-coupled amplifiers are quite expensive. They offer the advantage of responding to dc voltages, so it is possible to measure dc voltages as pure signals and ac signals superimposed upon the dc signals. DC-coupled amplifiers have another advantage. They eliminate the problems of low-frequency phase shift and waveform distortion while observing low-frequency pulse train.

The amplifiers can be classified according to bandwidth use also:
(i) Narrow-bandwidth amplifiers
(ii) Broad-bandwidth amplifiers

If the frequency band does not extend up to the television colour sub-carrier frequency of 4.33 MHz , the amplifier can be classified as a narrow-bandwidth amplifier. If the frequency response curve of the amplifier is flat, beyond 4.33 MHz , the amplifier is classified as a broad-bandwidth amplifier. Laboratory oscilloscopes respond to frequencies in excess of 5 MHz .

## 8-3-2 Vertical Amplifiers

Vertical amplifiers determines the sensitivity and bandwidth of an oscilloscope. Sensitivity, which is expressed in terms of $\mathrm{V} / \mathrm{cm}$ of vertical deflection at the mid-band frequency.

Generally, amplifiers have a certain gain bandwidth product, which is the product of the voltage gain of the amplifier and its bandwidth. Voltage gain may be sacrificed in favour of greater bandwidth or vice versa.

The gain of the vertical amplifier determines the smallest signal that the oscilloscope can satisfactorily measure by reproducing it on the CRT screen. The sensitivity of an oscilloscope is directly proportional to the gain of the vertical amplifier. So, as the gain increases the sensitivity also increases. This facilitates the study the smaller amplitude signals.

The vertical sensitivity measures how much the electron beam will be deflected for a specified input signal. The CRT screen is covered with a plastic grid pattern called a graticule. The spacing between the grids lines is typically 10 mm . Vertical sensitivity is generally expressed in volts per division. On the front panel of the oscilloscope a rotary switch is used for gain control. The gain could be designated V/Div. The rotary attenuator switch is electrically connected to the input attenuator network. The setting of the rotary switch indicates the amplitude of the signal required to deflect the beam vertically by one division. The vertical sensitivity of an oscilloscope measures the smallest deflection factor that can be selected with the rotary switch.

The bandwidth of an oscilloscope detects the range of frequencies that can be accurately reproduced on the CRT screen. The greater the bandwidth, the wider is the range of observed frequencies. The broadband gain should be constant near the higher range of frequencies which can be observed using an oscilloscope.

The bandwidth of an oscilloscope is the range of frequencies over which the gain of the vertical amplifier stays within 3 db of the mid-band frequency gain, as shown in Figure 8-4. Rise time is defined as the time required for the edge to rise from $10-90 \%$ of its maximum amplitude. When an oscilloscope is used to observe a pulse or a square wave, the rise time of the instrument must be faster than the rise time of the pulse or square wave. An approximate relation is given as follows:


Figure 8-4 Frequency response graphs

$$
t_{r} \times B W=0.35
$$

where, $t_{r}$ is the rise time in seconds and $B W$ is the band width in Hertz.

## 8-4 SWEEP FREQUENCY GENERATOR

A sweep frequency generator is a signal generator which can automatically vary its frequency smoothly and continuously over an entire frequency range. Figure 8-5 shows the basic block diagram of a sweep frequency generator. The sweep frequency generator has the ramp generator and the voltage-tuned oscillator as its basic components.

The output of the ramp generator is a linear ramp voltage which serves as the input to the voltage-tuned oscillator. The basic circuit of a voltage-tuned oscillator is similar to that of a frequency modulator circuit.


Figure 8-5 Block diagram of a sweep frequency generator


Figure 8-6 Oscillator tank circuit

The resonant frequency of the tank circuit is given by:

$$
\begin{equation*}
f=\frac{1}{2 \pi \sqrt{L C}} \tag{8-2}
\end{equation*}
$$

With the increase of the voltage level of the ramp output, the reverse-bias on the diode of the oscillator circuit increases. This, is in turn, reduces the capacitance $C_{d}$ and the resonance frequency of the tank circuit increases. As the ramp voltage returns to its zero level, the diode capacitance and the output frequency of the oscillator decrease to return to their starting levels. The frequency range over which the oscillator frequency is swept is predetermined by choosing appropriate values of $L$ and $C$. Figure 8-6 shows an oscillator tank circuit.

## 8-4-1 Applications of the Sweep Frequency Generator

1. Sweep frequency generators are used to display the response curve of the various stages of frequency of television or radio receivers.
2. Sweep frequency generators can be used to determine the characteristics of a device over a wide continuous range of frequencies.

## 8-5 MEASUREMENTS USING THE CATHODE-RAY OSCILLOSCOPE

The CRO is used to measure frequency, time, phase and different parameters of signals. In the following sections we discuss the methods of measuring frequency using Lissajous figures and timebase; measurement of phase using the double-beam CRO and Lissajous figures.

## 8-5-1 Measurement of Frequency

## Time-base measurement

Time-base measurement helps to determine the frequency of a time-varying signal displayed on the CRT screen. If a time interval $t$ has $x$ complete cycles, then the time period of the signal is:
or,

$$
\begin{gathered}
T=\frac{t}{x} \\
f=\frac{1}{T}=\frac{x}{t}
\end{gathered}
$$

Hence, the frequency is determined.

## Measurement using Lissajous figures

The application of sinusoidal waves at the same time to the deflection plates produces various patterns. These patterns are generated on the basis of the relative amplitudes, frequencies and phases of the different waveforms and are known as Lissajous figures.

Figure 8-7 shows the Lissajous figure as a form of ellipse.
Frequency can be determined from:

$$
\frac{f_{v}}{f_{h}}=\frac{\text { Number of horizontal tangencies }}{\text { Number of vertical tangencies }}
$$

where, $f_{v}$ and $f_{h}$ are the frequencies of the vertical and the horizontal signals, respectively. Examples 8-1 and 8-4 show the practical ways of calculating frequency using Lissajous patterns.


Figure 8-7 Lissajous figure as a form of ellipse

## 8-5-2 Measurement of Phase

The phase difference of two different waveforms displayed on the CRT screen can be found from the time axis. Two sinusoidal signals of time period $T$ are in the same phase at time $t_{1}$ and $t_{2}$ respectively, and the phase difference between them is expressed as:

$$
\begin{equation*}
\varphi=\frac{2 \pi}{T}\left(t_{1}-t_{2}\right) \tag{8-3}
\end{equation*}
$$

Figure 8-8 shows the phase difference of two different waveforms.


Figure 8-8 Measurement of phase difference

## 8-5-3 Measurement of Phase Using Lissajous Figures

Lissajous figures are used to measure the phase difference between two sinusoidal voltages of the same amplitude and frequency. The signals are applied simultaneously to the horizontal and vertical deflection plates. The values of the deflection voltages are given by:

$$
\begin{align*}
& v_{y}=\mathrm{A} \sin (\omega t+\varphi)  \tag{8-4}\\
& v_{x}=\mathrm{A} \sin \omega t \tag{8-5}
\end{align*}
$$

and Equation (8-4) can be expanded as:

$$
\begin{equation*}
v_{y}=A \sin \omega t \cos \varphi+A \cos \omega t \sin \varphi \tag{8-6}
\end{equation*}
$$

Equation (8-5) yields:

$$
\begin{equation*}
A \cos \omega t=\sqrt{A^{2}-v_{x}^{2}} \tag{8-7}
\end{equation*}
$$

Substituting the sine and cosine terms from Equations (8-4) and (8-5) in Equation (8-6), we get:

$$
\begin{aligned}
& v_{y}=A \sin \omega t \cos \varphi+\sqrt{A^{2}-v_{x}^{2}} \sin \varphi \\
& v_{y}=v_{x} \cos \varphi+\sqrt{A^{2}-v_{x}^{2}} \sin \varphi \\
& v_{y}-v_{x} \cos \varphi=\sqrt{A^{2}-v_{x}^{2}} \sin \varphi \\
& \left(v_{y}-v_{x} \cos \varphi\right)^{2}=\left(A^{2}-v_{x}^{2}\right) \sin ^{2} \varphi
\end{aligned}
$$

$$
\begin{align*}
& v_{y}^{2}-2 v_{x} \cos \varphi v_{y}+v_{x}^{2} \cos ^{2} \varphi=A^{2} \sin ^{2} \varphi-v_{x}^{2} \sin ^{2} \varphi \\
& v_{y}^{2}-2 v_{x} \cos \varphi v_{y}+v_{x}^{2} \cos ^{2} \varphi v_{x}^{2} \sin ^{2} \varphi=A^{2} \sin ^{2} \varphi \\
& v_{y}^{2}-2 v_{x} \cos \varphi v_{y}+v_{x}^{2}\left(\cos ^{2} \varphi+\sin ^{2} \varphi\right)=A^{2} \sin ^{2} \varphi \\
& v_{y}^{2}-2 v_{x} \cos \varphi v_{y}+v_{x}^{2}=A^{2} \sin ^{2} \varphi \\
& v_{x}^{2}+v_{y}^{2}-2 v_{x} v_{y} \cos \varphi=A^{2} \sin ^{2} \varphi \tag{8.8}
\end{align*}
$$

The Lissajous figure is thus an ellipse represented by Equation (8-8). The ellipse is depicted in Figure 8-7.
Case I: When $\varphi=0^{\circ}, \cos \varphi=1$,

$$
\sin \varphi=0
$$

Then, Equation (8-8) reduces to:

$$
\begin{aligned}
v_{x}^{2}+v_{y}^{2}-2 v_{x} v_{y} & =0 \\
\left(v_{x}-v_{y}\right)^{2} & =0 \\
v_{x} & =v_{y}
\end{aligned}
$$

$$
\varphi=0^{\circ}
$$



Figure 8-9(a) Lissajous figure at $\varphi=0^{\circ}$ is a straight line with slope $m=1$

Equation (8-9) represents a straight line with slope $45^{\circ}$, i.e., $m=1$. The straight line diagram is shown in Figure 8-9(a).
Case II: When $0<\varphi<90, \varphi=45^{\circ}$,

$$
\cos \varphi=\frac{1}{\sqrt{2}}, \quad \sin \varphi=\frac{1}{\sqrt{2}}
$$

Then Equation (8-8) reduces to:

$$
\begin{equation*}
v_{x}^{2}+v_{y}^{2}-\sqrt{2} v_{x} v_{y}=\frac{A^{2}}{2} \tag{8-10}
\end{equation*}
$$

Equation (8-8) represents an ellipse, as shown in Figure 8-9(b).

Case III: When $\varphi=90^{\circ}, \cos \varphi=0$,

$$
\sin \varphi=1
$$

Then Equation (8-8) reduces to:

$$
\begin{equation*}
v_{x}^{2}+v_{y}^{2}=A^{2} \tag{8-11}
\end{equation*}
$$

$$
0^{\circ}<\varphi<90^{\circ}
$$



Figure 8-9(b) Lissajous figure at $0^{\circ}<\varphi<90$ takes the shape of an ellipse


Figure 8-10 Lissajous figure at $\varphi=90^{\circ}$ : it forms a circle

$$
\begin{equation*}
v_{x}^{2}+v_{y}^{2}+\sqrt{2} v_{x} y_{y}=\frac{A^{2}}{2} \tag{8-12}
\end{equation*}
$$

Equation (8-12) represents an ellipse shown in Figure 8-11.

> Case V: $\varphi=180^{\circ}, \cos \varphi=-1$ $\sin \varphi=0$

Then Equation (8-8) reduces to:

$$
\begin{align*}
v_{x}^{2}+v_{y}^{2}+2 v_{x} v_{y} & =0 \\
\left(v_{x}+v_{y}\right)^{2} & =0 \\
v_{x} & =-v_{y} \tag{8-13}
\end{align*}
$$

Equation (8-13) represents a straight line with slope $m=-1$; a slope of $45^{\circ}$ in the negative direction of the $x$-axis, as shown in Figure 8-12.

The maximum $y$-displacement, $A$, and the vertical displacement, $V_{y}$, at time $t=0$ can be measured from the vertical scale of the CRO. Putting $t=0$ in Equation (8-26), we get:

$$
\begin{align*}
v_{y 0} & =A \sin \varphi  \tag{8-14}\\
\sin \varphi & =\frac{v_{y 0}}{A}
\end{align*}
$$

Thus, the phase angle can be found from Equation (8-15) using any form of the Lissajous figure.

## Solved Examples

Example 8-1 AcertainLissajouspattern is produced by applying sinusoidal voltages to the vertical and horizontal input terminals of a CRO. The pattern makes five tangencies with the vertical three with the horizontal. Calculate the frequency of the signal applied to the vertical amplifier if the frequency of the input voltage is 3 kHz .

## Solution:

A feature that is common to all Lissajous figures is that the horizontal and the vertical lines are tangent to the pattern at a number of points. The number depends on the frequency applied to the vertical and to the horizontal deflecting plates and is given by:

$$
\frac{\text { Number of points at which figure is tangent to vertical line }}{\text { Number of points at which figure is tangent to horizontal line }}=\frac{\omega_{x}}{\omega_{y}}
$$

According to the data given in the problem, we have:

$$
\frac{5}{3}=\frac{3}{\omega_{y}} \mathrm{kHz}
$$

Hence the frequency of the signal applied to the vertical amplifier is:

$$
\omega_{y}=\frac{9}{5}=1.8 \mathrm{kHz}
$$

Example 8-2 A CRT is designed to have a deflection sensitivity of $0.5 \mathrm{~mm} / \mathrm{V}$. The deflecting plates are 3 cm long and 6 mm apart. $T$ distance of the screen from the centre of the plates is 20 cm . Calculate the required voltage to be applied to the final anode?

## Solution:

Deflection sensitivity:

$$
\begin{aligned}
S & =\frac{l L}{2 d V_{a}} \\
V_{a} & =\frac{l L}{2 d S}
\end{aligned}
$$

where, $l=3 \mathrm{~cm}, L=20 \mathrm{~cm}, \mathrm{~d}=0.6 \mathrm{~cm}, S=0.05 \mathrm{~cm} / \mathrm{V}$.
Therefore, the anode voltage $V_{a}=1000 \mathrm{~V}$
Example 8-3 Two ac signals of same frequency but having a phase difference are displayed simultaneously on a dual-trace CRO. If the horizontal separation between two neighbouring peaks of the displayed waveform corresponds to 2 divisions and the distance between two consecutive peaks of a signal wave corresponds to 14 divisions of the horizontal scale, calculate the phase difference between the two signals.

## Solution:

The phase difference

$$
\phi=\frac{2 \pi}{D} \times d
$$

Here, $d=2$ divs and, $D=14$ divs

Therefore,

$$
\phi=\frac{2 \pi}{D} \times 2=\frac{\pi}{3}=60^{\circ}
$$

Example 8-4 A certain Lissajous pattern is produced by applying sinusoidal voltages to the vertical and horizontal input terminals of a CRO. The pattern makes five tangencies with the vertical and three with the horizontal. Calculate the frequency of the signal applied to the vertical amplifier if the frequency of the input voltage is 14 kHz .

## Solution:

A feature that is common to all Lissajous figures is that the horizontal line and the vertical line are tangent to the pattern at a number of points. The number depends on the frequency applied to the vertical and to the horizontal deflecting plates and is given by:

$$
\frac{\text { Number of points at which figure is tangent to vertical line }}{\text { Number of points at which figure is tangent to horizontal line }}=\frac{\omega_{x}}{\omega_{y}}
$$

According to the data given in the problem, we have:

$$
\frac{5}{3}=\frac{12}{\omega_{y}} \mathrm{kHz}
$$

Hence the frequency of the signal applied to the vertical amplifier is:

$$
\omega_{y}=\frac{36}{5}=7.2 \mathrm{kHz}
$$

## 8-6 TYPES OF CATHODE-RAY OSCILLOSCOPE

The categorization of CROs is done on the basis of whether they are digital or analog. Digital CROs can be further classified as storage oscilloscopes. Different types of CRO models are explained in brief in the following sections.

## 8-6-1 Analog CRO

In an analog CRO, the amplitude, phase and frequency are measured from the displayed waveform, through direct manual reading.

## 8-6-2 Digital CRO

A digital CRO offers digital read-out of signal information, i.e., the time, voltage or frequency along with signal display. It consists of an electronic counter along with the main body of the CRO.

## 8-6-3 Storage CRO

A storage CRO retains the display up to a substantial amount of time after the first trace has appeared on the screen. The storage CRO is also useful for the display of waveforms of low-frequency signals. The displayed waveform can also be stored or saved in the memory section of the CRO.

## 8-6-4 Dual-Beam CRO

In the dual-beam CRO two electron beams fall on a single CRT. The dual-gun CRT generates two different beams. These two beams produce two spots of light on the CRT screen which make the simultaneous observation of two different signal waveforms possible. The comparison of input and its corresponding output becomes easier using the dual-beam CRO.

## 8-7 CATHODE-RAY TUBE

The electron gun or electron emitter, the deflecting system and the fluorescent screen are the three major components of a general purpose CRT. A detailed diagram of the cathode-ray oscilloscope is given in Figure 8-13.

## 8-7-1 Electron Gun

In the electron gun of the CRT, electrons are emitted, converted into a sharp beam and focused upon the fluorescent screen. The electron beam consists of an indirectly heated cathode, a control grid, an accelerating electrode and a focusing anode. The electrodes are connected to the base pins. The


Figure 8-13 Components of a cathode-ray oscilloscope


Figure 8-14(a) Deflecting system using parallel vertical plates


Figure 8-14(b) Deflecting system using parallel horizontal plate
cathode emitting the electrons is surrounded by a control grid with a fine hole at its centre. The accelerated electron beam passes through the fine hole. The negative voltage at the control grid controls the flow of electrons in the electron beam, and consequently, the brightness of the spot on the CRO screen is controlled.

## 8-7-2 Deflection Systems

Electrostatic deflection of an electron beam is used in a general purpose oscilloscope. The deflecting system consists of a pair of horizontal and vertical deflecting plates. Let us consider two parallel vertical deflecting plates $P_{1}$ and $P_{2}$. The beam is focused at point $O$ on the screen in the absence of a deflecting plate voltage. If a positive voltage is applied to plate $P_{1}$ with respect to plate $P_{2}$, the negatively charged electrons are attracted towards the positive plate $P_{1}$, and these electrons will come to focus at point $Y_{1}$ on the fluorescent screen. The deflection is proportional to the deflecting voltage between the plates. If the polarity of the deflecting voltage is reversed, the spot appears at the point $Y_{2}$, as shown in Figure 8-14(a). To deflect the beam horizontally, an alternating voltage is applied to the horizontal deflecting plates and the spot on the screen horizontally, as shown in Figure 8-14(b). The electrons will focus at point $X_{2}$.

By changing the polarity of voltage, the beam will focus at point $X_{1}$. Thus, the horizontal movement is controlled along $X_{1} O X_{2}$ line.

## Spot beam deflection sensitivity

The deflection sensitivity of a CRT is defined as the distance of the spot-beam deflection on the screen per unit voltage. If $l_{\text {total }}$ is the total amount of deflection of the spot beam on the screen for the deflecting voltage $V_{d}$, as shown in Figure8-15, the sensitivity can be expressed as:


Figure 8-15 Schematic diagram of electrostatic deflection systems

$$
\begin{equation*}
S=\frac{I_{\text {total }}}{V_{d}} \tag{8-16}
\end{equation*}
$$

The unit of deflection sensitivity is milimeter/Voltage.
If $V_{d}=1$, then $S=l_{\text {total }}$, i.e., the magnitude of the defection sensitivity is equal to the spot deflection distance for the applied unit deflection voltage.

## Electrostatic deflection

$s=$ separation between deflecting plates
$P=$ distance between the plate and screen $S$
$l=$ length of each deflecting plate
$V_{d}=$ deflecting voltage applied across the plates
$m=$ mass of the electron
$e=$ charge of the electron
$v=$ velocity of the entering electron
$V_{a}=$ accelerating anode voltage
Thus:

$$
\begin{align*}
\frac{1}{2} m v^{2} & =e V_{a}  \tag{8-17}\\
v^{2} & =\frac{2 e V_{a}}{m} \tag{8-18}
\end{align*}
$$

Force exerted on the electron towards the positive deflecting plate is:

$$
F s=e V_{d}
$$

$$
\begin{gather*}
F=\frac{e V_{d}}{s}  \tag{8-19}\\
m f=\frac{e V_{d}}{s} \\
1 f=\frac{e V_{d}}{m s} \tag{8-20}
\end{gather*}
$$

Hence, acceleration is:
Time taken by the electron to move through the deflecting plates is:

$$
t=\frac{l}{v}
$$

Therefore, the upward velocity acquired by the emerging electron is:

$$
\begin{gather*}
v_{y}=f t \\
v_{y}=\frac{f l}{v} \\
v_{y}=\frac{f l}{v}=\frac{e V_{d}}{\operatorname{sm}} \frac{l}{v} \tag{8-21}
\end{gather*}
$$

The vertical displacement of the electron in this case is derived directly from the well-known formula of mechanics:

$$
D=u t+\frac{1}{2} f t^{2}
$$

where, $D$ is the distance traversed by an electron, $u$ is the initial velocity, $f$ is the acceleration of an electron, and $t$ is the time taken.

As the electron is starting from rest, the initial velocity is zero, i.e., $u=0$ and the distance travelled by the electron $D=l_{2}$.

Substituting this value of $D$ in the expression for $D$, from the formula of mechanics, we get:

$$
\begin{equation*}
l_{2}=\frac{1}{2} f t^{2} \tag{8-22}
\end{equation*}
$$

Substituting the value of $t$ in Equation (14-7) we get:

$$
\begin{align*}
l_{2} & =\frac{1}{2} f\left(\frac{l_{1}}{v}\right)^{2}=\frac{e V_{d}}{2 s m}\left(\frac{l}{v}\right)^{2}  \tag{8-23}\\
\tan \theta & =\frac{v_{y}}{v}=\frac{l_{1}}{P}  \tag{8-24}\\
l_{\text {total }} & =l_{1}+l_{2}=\frac{e V_{d} l}{s m v^{2}}\left(\frac{l}{2}+P\right)  \tag{8-25}\\
L & =\left(\frac{l}{2}+P\right) \tag{8-26}
\end{align*}
$$

Substituting $v^{2}$ from Equation (8-18) and $L$ from Equation (8-26) in Equation (8-25) we have:

$$
\begin{equation*}
l_{\text {total }}=\frac{l L V_{d}}{2 s V_{a}} \tag{8-27}
\end{equation*}
$$



Figure 8-16(a) A typical display waveform on the screen
The deflection sensitivity of the CRT is, by definition:

$$
\begin{equation*}
S=\frac{l_{\text {total }}}{V_{d}}=\frac{l L}{2 s V_{a}} \mathrm{~m} / \mathrm{V} \tag{8-28}
\end{equation*}
$$

The deflection factor of the CRT is: $\quad G=\frac{1}{S}=\frac{2 s V_{a}}{l L} \mathrm{~V} / \mathrm{m}$
The deflection sensitivity can be increased by reducing the anode voltage; as a result the brightness of the spot gets reduced. This problem is solved by post-acceleration. The beam is accelerated after it has been deflected by an enhancer anode.

## 8-7-3 Fluorescent Screen

Phosphor is used as screen material on the inner surface of a CRT. Phosphor absorbs the energy of the incident electrons. The spot of light is produced on the screen where the electron beam hits. The bombarding electrons striking the screen, release secondary emission electrons. These electrons are collected or trapped by an aqueous solution of graphite called "Aquadag" which is connected to the second anode. Collection of the secondary electrons is necessary to keep the screen in a state of electrical equilibrium.

The type of phosphor used, determines the colour of the light spot. The brightest available phosphor isotope, P31, produces yellow-green light with relative luminance of $99.99 \%$. The persistence of glow of the phosphor after the electrons have ceased bombarding plays an important role in the selection of the phosphor. The continuous excited spots on the screen form an unbroken line. High persistence results in an undesirable overlapping of a new trace with an old or previous trace.

Usually the CRT is kept at relatively lower brightness. A bright spot on the screen for a long time will cause a burnout. After hitting the screen, the electrons should return to the anode for closing the circuit. The negative charge accumulated near the screen will repel the electron beam, and there will be no display on the screen. Figure 8-16(a) illustrates a typical CRT display waveform on a fluorescent screen.


Figure 8-16(b) Triangular waveform input applied to the vertical deflecting plates of CRO
Figure 8-16(a) shows a sine wave applied to vertical deflecting plates and a repetitive ramp or saw-tooth applied to the horizontal plates. The ramp waveform at the horizontal plates causes the electron beam to be deflected horizontally across the screen. If the waveforms are perfectly synchronized then the exact sine wave applied to the vertical display appears on the CRO display screen. Similarly the display of the triangular waveform is as shown in Figure 8-16(b).

## Solved Examples

Example 8-5 The electron beam in a CRT enters a magnetic deflection system after being accelerated through a potential difference of 1 kV . The deflection system employs a magnetic field of 160 gauss acting over an axial length of 1 cm . Find the deflection of the spot on the fluorescent screen placed at a distance of 20 cm from the centre of the deflection system. Calculate the deflection sensitivity.

## Solution:

Given: $B=160$ gauss $=1.6 \times 10^{-2}$ tesla, $\quad V=103$ volt, $\quad l=1 \mathrm{~cm}=0.01 \mathrm{~m}$

$$
L+\frac{1}{2}=20 \mathrm{~cm}=0.2 \mathrm{~m}
$$

$\therefore \quad$ The deflection of the spot is:

$$
\begin{aligned}
d & =B \sqrt{\frac{e}{2 V m}} l\left(L+\frac{l}{2}\right) \\
& =0.299 \mathrm{~m}=29.9 \mathrm{~cm}
\end{aligned}
$$

The magnetic deflection sensitivity is:

$$
S=\frac{d}{B}=\frac{299}{150}=1.99 \mathrm{~mm} / \text { gauss }
$$

Example 8-6 The Lissajous figure is produced upon application of sinusoidal voltages to the two deflecting plates. The pattern gives four tangencies with the vertical and three tangencies with
the horizontal. If the frequency of the horizontal signal is 1 kHz , what will be the frequency of the vertical signal?

## Solution:

Let $f_{v}$ and $f_{h}$ be the frequencies of the vertical and horizontal signals respectively.
Then,

$$
\frac{f_{v}}{f_{h}}=\frac{3}{4}
$$

Given: $\quad f_{h}=4 \mathrm{kHz}=4000 \mathrm{~Hz}$

$$
\therefore \quad f_{v}=3000 \mathrm{~Hz}=3 \mathrm{kHz}
$$

Example 8.7 The transit time of an electron through the deflection plates of a CRT should be kept below 0.2 per cycle. If the electrons enter the deflection system with a KE of 1 keV and the axial length of each deflection plate is 1.5 cm , calculate the highest frequency of the deflecting voltage.

## Solution:

Axial velocity of the electron:

$$
v=\sqrt{\frac{2 e V_{a}}{m}}=1.87 \times 10^{7} \mathrm{~m} / \mathrm{s}
$$

Transit time of the electron through the deflecting plates:

$$
\tau=\frac{l}{v}=\frac{1.5 \times 10^{-2}}{1.87 \times 10^{7}}=0.802 \times 10^{-9} \mathrm{~s}
$$

$T$ is the time period of the sinusoidal deflecting voltage:

Hence,

$$
\begin{aligned}
\tau_{\max } & =(0.2 / 360) \times T \\
\frac{0.2}{360} T & =0.802 \times 10^{-9} \\
& T=\frac{2.887}{2} \times 10^{-6} \mathrm{~s}=1.4435 \times 10^{-6} \mathrm{~s}
\end{aligned}
$$

Therefore, the highest frequency of the deflecting voltage is:

$$
f=\frac{1}{T}=6.92 \times 10^{5} \mathrm{~Hz}=692 \mathrm{kHz}
$$

Example 8-8 A trigger pulse is applied to the sweep generator every 10 ms . Compute the amplitude of the voltage $V_{o}$ across the capacitor when the trigger pulse is applied. The value of the capacitor is $0.2 \mu \mathrm{~F}$ and resistance is $500 \mathrm{k} \Omega$. Supply voltage is 50 volt.

## Solution:

Using standard formula:

$$
\begin{aligned}
V_{o} & =V_{c c}\left[1-\exp \left(-\frac{t}{R C}\right)\right] \\
V_{c c} & =50 \mathrm{~V} \\
T & =10 \mathrm{msec}=10 \times 10^{-3} \mathrm{sec} \\
R & =500 \times 10^{3} \Omega
\end{aligned}
$$

$$
C=0.2 \times 10^{-6} \mathrm{Farad}
$$

Putting the values we get:

$$
V_{o}=4.76 \mathrm{Volt}
$$

Since $V_{o}$ is less than $10 \%$ of $V_{c c}$, the charge curve should still be quite at this point when $V_{o}$ is 4.76 V .
Example 8-9 The time-base of a CRO is set at $0.1 \mathrm{~ms} / \mathrm{cm}$. A sinusoidal signal applied to the vertical deflection plate gives 5 cycles over a sweep width of 20 cm . Calculate the frequency of the signal.

## Solution:

One cycle of signal occupies:

$$
\frac{20}{5} \mathrm{~cm}=4 \mathrm{~cm}
$$

The time interval corresponding to 4 cm is $0.1 \times 4=0.4 \mathrm{~ms}$.
Hence, the frequency is: $f=\frac{1}{0.4 \mathrm{~ms}}=\frac{10 \times 10^{3}}{4}=2500 \mathrm{~Hz}=2.5 \mathrm{kHz}$
Example 8-10 Two sinusoidal voltages of the same amplitude and frequency are applied simultaneously to the vertical and horizontal deflection systems of a CRO. An ellipse is traced on the fluorescent screen. The slope of the major axis is negative. The trace has a maximum vertical value of 3 divisions and it crosses the vertical axis at 1.1 divisions above the origin. What is the phase difference between the voltages?

## Solution:

If $\theta$ is the phase difference between the two voltages, we have:

$$
\begin{gathered}
\sin \theta=\frac{v_{y 0}}{A}=\frac{1.1}{3}=0.366 \\
\theta=159^{\circ}
\end{gathered}
$$

As the major axis of the ellipse has negative slope, $\theta$ must lie between $90^{\circ}$ and $180^{\circ}$.
Example 8-11 The electron beam in a CRT is accelerated through a potential difference of 4000 V . The beam then travels through a pair of deflecting plates of axial length 2 cm , the separation between the plates being 5 mm . The potential difference applied between the plates is 20 V . The distance of the CRT screen from the centre of the deflecting plates is 25 cm . Determine:
(a) The transit time of the beam through the deflecting plates
(b) The transverse acceleration imparted to the electrons
(c) The deflection of the spot on the CRT screen. Also calculate deflection sensitivity

## Solution:

The axial velocity of the electron is:
(a) Transit time:

$$
v=\sqrt{\frac{2 e V_{a}}{m}}=3.74
$$

$$
t=\frac{l}{v}=0.5035 \times 10^{-9} \mathrm{~s}
$$

(b) Transverse acceleration:

$$
\begin{aligned}
\frac{e V_{d}}{s m} & =0.702 \times 10^{15} \mathrm{~m} / \mathrm{s}^{2} \\
d & =\frac{l L}{2 s} \frac{V_{d}}{V_{a}}=.25 \mathrm{~cm} \\
S & =\frac{d}{V_{d}}=0.5 \mathrm{~mm} / \mathrm{V}
\end{aligned}
$$

(c) Spot deflection:

## 8-8 SINE WAVE GENERATOR

Generally a sine wave is not produced from the function generator as a primary waveform. This is because at low frequencies amplitude and frequency distortions are introduced. A sine wave is produced by converting a triangular wave, applying proper circuits. The triangular wave is produced by employing an integrator and a Schmitt trigger circuit. This triangular wave is then converted to a sine wave using the diode loading circuit, as shown in Figure 8-17.

Resistors $R_{1}$ and $R_{2}$ behave as the voltage divider. When $V R_{2}$ exceeds $+V_{1}$, the diode $D_{1}$ becomes forward-biased. There is more attenuation of the output voltage levels above $+V_{1}$ than levels below $+V_{1}$. With the presence of the diode $D_{1}$ and resistor $R_{3}$ in the circuit, the output voltage rises less steeply. The output voltage falls below $+V_{1}$ and the diode stops conducting, as it is in reverse-bias. The circuit behaves as a simple voltage-divider circuit. This is also true for the negative half-cycle of the input $V_{i}$. If $R_{3}$ is carefully chosen to be the same as $R_{4}$, the negative and the positive cycles of the output voltage will be the same. The output is an approximate sine wave.

The approximation may be further improved by employing a six-level diode loading circuit, as shown in Figure 8-18(a). All the diodes are connected to different bias voltage levels by appropriate values of resistors. As there are six diodes, there will three positive- and three negative-bias voltage levels. Therefore, at each half-cycle of the output voltage, the slope changes six times and the output wave shape is a better approximation of the sine wave.

The triangular to sine wave converter is an amplifier whose gain varies inversely with the amplitude of the output voltage.
$R_{1}$ and $R_{3}$ set the slope of $V_{0}$ at low amplitudes near the zero crossing. As $V_{0}$ increases, the voltage across $R_{3}$ increases to begin forward biasing $D_{1}$ and $D_{3}$ for positive outputs or $D_{2}$ and $D_{4}$ for negative output. When these diodes conduct, they shunt feedback resistance $R_{3}$ lowering the gain. This tends to shape the triangular output into the sine wave. In order to get the rounded tops for sine waves,


Figure 8-17 Two-level diode loading circuit


Figure 8-18(a) Diagram for the six-level diode loading circuit


Figure 8-18(b) Triangular to sine wave generator using op-amp
output $R_{2}$ and diodes $D_{1}$ and $D_{2}$ are adjusted to make the amplifier gain approach zero at the peak. The circuit is shown in Figure 8-18(b).

The circuit is adjusted by comparing a 1 kHz sine wave and the output of the triangular/sine wave converter on a dual-track CRO. $R_{1}, R_{2}, R_{3}$ and the peak amplitude of $E_{i}$ are adjusted in sequence for the best sinusoidal shape.

## 8-9 SQUARE WAVE GENERATOR

A square wave can be most easily obtained from an operational amplifier astable multi-vibrator. An astable multi-vibrator has no stable state-the output oscillates continuously between high and low states.


Figure 8-19 Sine wave generator
In Figure 8-19, the block comprising the op-amp, resistors $R_{2}$ and $R_{3}$ constitutes a Schmitt trigger circuit. The capacitor $C_{1}$ gets charged through the resistor $R_{1}$. When the voltage of the capacitor reaches the upper trigger point of the Schmitt trigger circuit, the output of the op-amp switches to output low. This is because the Schmitt trigger is a non-inverting type. Now, when the op-amp output is low, the capacitor $C_{1}$ starts getting discharged. As the capacitor discharges and the capacitor voltage reaches the lower trigger point of the Schmitt trigger, the output of the op-amp switches back to the output high state. The capacitor charges through the resistor again and the next cycle begins. The process is repetitive and produces a square wave at the output. The frequency of the output square wave depends on the time taken by the capacitor to get charged and discharged when the capacitor voltage varies from UTP (upper trigger point) and LTP (lower trigger point).


Figure 8-20 Wien-bridge feedback network with an amplifier

The frequency of the output square wave is given by:

$$
\begin{equation*}
f=\frac{1}{T}=\frac{1}{2 t} \tag{8-30}
\end{equation*}
$$

where, $t$ is the time taken by the capacitor to get charged or discharged. The UTP and LTP values for the Schmitt trigger can be fixed by choosing appropriate values of $R_{2}$ and $R_{3}$.

$$
\begin{equation*}
|\mathrm{UTP}|=|\mathrm{LTP}|=V_{0} \frac{R_{3}}{R_{2}+R_{3}} \tag{8-31}
\end{equation*}
$$

## 8-10 AF SIGNAL GENERATOR

An AF signal generator generally uses an oscillator which is regulated by a controlled phase shift through a resistor and capacitor network. The Wien-bridge oscillator produces sine waves using an RC network as a feedback.

The amplifier is connected as an oscillator in order to determine at what frequency the Wienbridge provides the required criterion for oscillation. With respect to ground, the voltage at $A$ is given by:
and

$$
\begin{align*}
V_{a} & =\frac{Z_{1}}{Z_{1}+Z_{2}} V_{i}  \tag{8-32}\\
V_{b} & =\frac{R_{1}}{R_{1}+R_{2}} V_{i} \tag{8-33}
\end{align*}
$$

Since $V_{a}$ and $V_{b}$ are the same, from Equations (8-32) and (8-33) we can write:

$$
\begin{equation*}
\frac{R_{1}}{R_{1}+R_{2}}=\frac{Z_{1}}{Z_{1}+Z_{2}} \tag{8-34}
\end{equation*}
$$

At a frequency $f_{0}=1 / 2 \pi R C$, the phase angle between $V_{a}$ and the output is zero. The Wien-bridge oscillator is tuned with a variable capacitance and the oscillator is band-switched using the resistance. The Wien-bridge oscillator is usually the heart of a general purpose AF signal generator. Harmonic distortion is then less than a few tenths of a percent.

## 8-11 FUNCTION GENERATOR

A function generator provides a variety of output waveforms. It can produce sine, square, ramp, pulse and triangular waveforms. The output amplitudes and frequencies are variable and a dc-offset adjustment is possible. The output frequency of a frequency generator may vary from a small fraction of a hertz to several hundred kilohertz. Output amplitude is usually $0-20 \mathrm{~V} p$-to- $p$ and $0-2 \mathrm{~V}$ $p$-to- $p$, while the output impedance is typically a few ohms. The accuracy of frequency selection of any function generator is around $\pm 2 \%$ of full scale of a given range, and distortion is less than $1 \%$. Figure 8-21 gives the basic block diagram of a function generator. The basic components of a function generator are:


Figure 8-21 Block diagram of a function generator
(i) Integrator
(ii) Schmitt trigger circuit
(iii) Sine wave converter
(iv) Attenuator

The output from the Schmitt trigger circuit is a square wave. The integrator produces a triangular waveform. The sine wave converter is used to convert a square or a triangular waveform into a sine wave. This instrument generates square or triangular waves as a primary waveform, which can then be applied to appropriate circuitry to produce the remaining waveform. Figure 8-22 gives the circuit diagram of a function generator.

The frequency of the function generator is controlled by the capacitor in the $L C$ or $R C$ circuit. The frequency is controlled by varying the magnitude of current which drives the integrator. The instrument produces sine, triangular and square waves with a frequency range of 0.01 Hz to 100 kHz .

The frequency controlled voltage regulates two current sources. The upper current source supplies constant current to the integrator whose output voltage increases linearly with time. The output of the integrator is a triangular waveform whose frequency is determined by the magnitude of the current supplied by the constant current source.

Attenuators are designed to change the magnitude of the input signal seen at the input stage, while presenting constant impedance on all ranges at the attenuator input. The attenuator is required to attenuate all frequencies equally.


Figure 8-22 Circuit diagram of a function generator

## POINTS TO REMEMBER

1. CRO is used to study waveforms.
2. CRT is the main component of a CRO.
3. Prosperous P31 is used for the fluorescent screen of a CRO.
4. A CRO has the following components:
(a) Electron gun
(b) Deflecting system
(c) Florescent screen
5. Lissajous figures are used to measure frequency and phase of the waves under study.
6. A time-base generator produces saw-tooth voltage.
7. An oscilloscope amplifier is used to provide a faithful representation of input signal applied to its input terminals.
8. Function generators can produce sine, square, ramp, pulse and triangular waveforms.
9. A sine wave is produced by converting a triangular wave, applying proper circuits.
10. Wien-bridge oscillator is usually the heart of a general purpose AF signal generator.

## IMPORTANT FORMULAE

1.The deflection sensitivity of the CRT is:

$$
S=\frac{l_{\text {total }}}{V_{d}}=\frac{l L}{2 s V_{a}} \mathrm{~m} / \mathrm{V}
$$

2. The deflection factor of the CRT is:

$$
G=\frac{1}{S}=\frac{2 s V_{a}}{l L} \mathrm{~V} / \mathrm{m}
$$

3. Phase angle is given by:

$$
\varphi=\frac{2 \pi}{T}\left(t_{1}-t_{2}\right)
$$

4. Lissajous equation is given by:

$$
v_{x}^{2}+v_{y}^{2}-2 v_{x} v_{y} \cos \varphi=A^{2} \sin ^{2} \varphi
$$

## OBJECTIVE QUESTIONS

1.Input impedance of CRO is:
(a) $1 \mathrm{M} \Omega$
(b) $1 \mathrm{k} \Omega$
(c) $100 \Omega$
(d) $1 \Omega$
2. CRO displays:
(a) AC signals
(b) DC signals
(c) Both ac and dc signals
(d) None of the above
3. CRO uses:
(a) Electrostatic deflection
(b) Magnetic deflection
(c) Electro-magnetic deflection
(d) None of the above
4. CRO fluroscent screen uses the phosphorous isotope:
(a) P31
(b) P32
(c) P30
(d) None of the above
5. Lissajous figure is used in CRO for:
(a) Phase measurement
(b) Frequency measurement
(c) Amplitude measurement
(d) None of the above
6. Lissajous figure at a 45 degree angle means:
(a) Straight line
(b) Circle
(c) Oval
(d) None of the above
7. The difference between the spectrum analyser (SA) and CRO is:
(a) CRO and SA both measure time domain signal
(b) CRO and SA both measure frequency domain signal
(c) CRO measures time domain signal and SA measures frequency domain
(d) CRO measures frequency domain signal and SA measures time domain
8. Digital storage oscilloscope is more preferable because of:
(a) Digital display
(b) Storage
(c) Both (a) and (b)
(d) None of the above
9. Saw-tooth voltage of a CRO means:
(a) Sweep time + fly back time
(b) Fly back time + sweep time
(c) Only fly back time
(d) Only sweep time
10. Defection sensitivity of CRO depends on:
(a) Deflection voltage, separation between the plates and plate length
(b) Only deflection voltage
(c) Only separation between plates
(d) Electron density

## REVIEW QUESTIONS

1.Draw the block diagram of a CRO and explain the function of each block.
2. What is CRT? How it is used?
3. Calculate the deflection sensitivity of a CRO? Why is electrostatic deflection used in a CRO?
4. How are different signal parameters measured by a CRO?
5. Explain the significance of Lissajous figures in CRO measurement.
6. How can you measure the frequency of a signal voltage using a CRO?
7. How can the phase difference between two ac voltages be measured by a CRO?
8. How can a waveform be displayed in a CRO?
9. State the applications of CRO.
10. Explain the following terms:
(a) Sweep voltage
(b) Synchronization
(c) Time-base
11. Distinguish between a CRT and a CRO.
14. Why is Aquadag coating neccessary for a CRO?
13. Derive the expression for deflection sensitivity.
14. Draw a sketch to illustrate the electrostatic deflection.
15. Define deflection factor and deflection sensitivity.
16. Discuss the factors that affect brightness of the display.
17. Briefly discuss the screen of a CRO.
18. Explain the sweep circuit of a CRO.
19. Describe the procedure of making amplitude and time measurement on an oscilloscope.
20. How are Lissajous figures obtained?
21. Derive the expression for obtaining Lissajous figures.
22. Describe the generation of a saw-tooth waveform.
23. What must be done to obtain a steady oscillogram?
24. How can a CRO measure the phase difference between two ac voltages?
25. What is post-acceleration and why is it used in a CRO?

## PRACTICE PROBLEMS

1. In a CRT, an electron beam is magnetically deflected after being accelerated through a potential difference of 1000 V . The deflecting magnetic field acts over an axial length of 1.8 cm . If a deflection sensitivity of $2.2 \mathrm{~mm} /$ gauss is to be attained, calculate the distance of the CRT screen from the centre of the deflection system?
2. ALissajous pattern is obtained on a CRO screen when the sinusoidal voltages are applied to the two sets of deflecting plates. The figure makes three tangencies with the horizontal and five tangencies with the vertical. If the frequency of the horizontal signal is 2.7 kHz , find the frequency of the vertical signal.
3. The accelerating voltage of a CRT is 1 kV . A sinusoidal voltage is applied to a set of deflecting plates of axial length 2.1 cm . Calculate the frequency of the deflecting voltage if the electrons remain between the plates for one half-cycles.
4. A deflection amplifier has the following components:

$$
\begin{aligned}
& R_{1}=R_{7}=10 \mathrm{k} \Omega \\
& R_{2}=R_{8}=5.7 \mathrm{k} \Omega \\
& R_{3}=R_{6}=15 \mathrm{k} \Omega \\
& R_{5}=2.3 \mathrm{k} \Omega \\
& R_{9}=R_{11}=15.2 \mathrm{k} \Omega \\
& R_{10}=2.2 \mathrm{k} \Omega
\end{aligned}
$$

If the supply voltage is $\pm 15 \mathrm{~V}$, determine the dc voltage levels throughout the circuit when the input level is zero and the moving contact of $R_{10}$ is at its centre position.
5. A 1 kHz triangular wave with peak amplitude of 11 V is applied to the vertical deflecting plates of a CRT. A 1 kHz saw-tooth wave with peak amplitude of 22 V is applied to the horizontal deflecting plates. The CRT has a
vertical deflection sensitivity of $0.4 \mathrm{~cm} / \mathrm{V}$ and a horizontal deflection sensitivity of $0.25 \mathrm{~cm} / \mathrm{V}$. Assuming that the two inputs are synchronized, determine the waveform displayed on the screen.
6. Repeat Problem 5 with the triangular-wave frequency changed to 2.2 kHz
7. If the vertical amplifier of the oscilloscope has the bandwidth of 17 MHz , what is the fastest rise time that an input may have to be displayed without distortion?
8. A certain Lissajous pattern is produced by applying sinusoidal voltages to the vertical and horizontal inputs of a CRO. The pattern makes five tangencies with the vertical and three with the horizontal. If the frequency of the horizontal input is 3 kHz , determine the frequency of the signal applied to the vertical input.
10. In a CRT the length of the deflecting plates is 1.6 cm , the spacing of the plates is 5 mm and the distance of the screen from the centre of the plates is 20 cm . If the final anode voltage is 1400 V , what would be the deflection sensitivity?
11. The deflection system in a CRT employs a magnetic field of $10^{-4} \mathrm{~T}$ acting over an axial length of 4 cm and is placed 24 cm from the screen. If the accelerating voltage is 600 V , find the deflection of the spot on the fluorescent screen.
12. If the time/div control of a waveform is set to 10 ms and the volts/div control is at 5.5 V , determine the peak amplitude and frequency of each waveform.
13. Two waveforms (A and B), each occupying five horizontal divisions for one cycle, are displayed on an oscilloscope. Wave B commences 1.6 divisions after commencement of wave A. Calculate the phase difference between the two.
14. If the volts/div of waveforms is set to 0.1 V and the time/div control is at $22 \mu \mathrm{~s}$, determine the pulse amplitude, the pulse frequency, the delay time, the rise time and the fall time.
15. A signal with an amplitude of $V_{s}=450 \mathrm{mV}$ and a source resistance of 1 kilo ohms is connected to an oscilloscope with $R_{i}=1 \mathrm{M} \Omega$ in parallel with $C_{i}=45 \mathrm{pF}$. The coaxial cable of the $1: 1$ probe used has a capacitance of $C_{c c}=-88 \mathrm{pF}$. Calculate the signal voltage level $V$ at the oscilloscope terminals when the signal frequency is 150 Hz . Also calculate the signal frequency at which $V_{t}$ is 3 dB below $V_{v}$.
16. In a CRT the distance between the deflecting plates is 1.0 cm , the length of the deflecting plate is 4.0 cm and the distance of the screen from the centre of the deflecting plate is 30 cm . If the accelerating voltage supply is 350 V , calculate the deflecting sensitivity of the tube.
17. An electrostatically deflected CRT has deflecting plate which is 3 cm long and 0.5 cm apart and the distance from the centre to the screen is 22 cm . The electron beam is accelerated by 2000 V and is projected centrally between the plates. Calculate the deflecting voltage required to cause the beam to strike the screen. Also, find the corresponding deflection.
18. In a neon tube time-base generator $R=100$ k and $C=0.01 \mu \mathrm{~F}$. The extinguishing and
striking potentials are 90 V and 140 V respectively. If the supply voltage is 180 V , determine the frequency of the time base.
19. Consider a circuit with $R_{1}=100 \mathrm{k} \Omega$, $R_{2}=50 \mathrm{k} \Omega$ and $V_{s}=150 \mathrm{~V}$. The voltage across $R_{2}$ is measured by the $0-50 \mathrm{~V}$ scale of a voltmeter of sensitivity $10 \mathrm{k} \Omega / \mathrm{V}$. Find the percentage error in measurement due to loading effect of the voltmeter.
20. Consider two $1 \mathrm{M} \Omega$ resistors connected in series and supplied by a source of 150 V . A multi-meter having a sensitivity $20 \mathrm{k} \Omega / \mathrm{V}$ is used to measure voltages across one of the resistors. The scale range used is 50 V . What will be the reading on the screen?
21. For the waveforms illustrated in the following diagram, the time/div control is at 50 ms , and the volts/div control is set to 22 mV . Determine the peak amplitude and frequency of each waveform, and calculate the phase difference.
22. Use the diagram provided for Problem 21, to calculate the number of horizontal divisions between the beginning of each waveform cycle for a phase difference of $35^{\circ}$.


## SUGGESTED READINGS

Kalsi, K. L. 2000. Electronic Measurement. New Delhi: Tata McGraw Hill.

Harris, F.K. 2000. Electrical Measurements. New York: John Wiley and Sons.
Golding E.W. and F.C.Wides. 1999. Electrical Measuring Instruments. A. H. Wheeler and Co.
Bell, David A. 1994. Electronic Instrumentation and Measurements. New Jersey: Prentice Hall.

Helfrick, Albert D. and William D. Cooper. 2000. Modern Electronic Instrumentation and Measurement Techniques. New Delhi: PHI.

Chattopadhyay, D. and P.C.Rakshit. 2006. Electronics Fundamentals and Applications. New Delhi: New Age International Publishers.

This page is intentionally left blank.

# Digital Electronic Principles 

## Outline

9-1 Introduction
9-2 Number System
9-3 Conversion of Number System
9-4 Boolean Algebra
9-5 Logic Gates

## 9-6 De Morgan's Theorem

9-7 Simplification of Boolean Expression
9-8 Logic Gate Circuits
9-9 Basic Concepts of Memory
9-10 Real-Life Applications

## Objectives

This chapter covers the fundamentals of digital electronics with a comprehensive overview of number systems, binary codes, logic gates and the applications of digital circuits. Beginning with an introduction to the history of digital systems, the chapter proceeds to discuss the number system and the conversion from binary to decimal. This is followed by a detailed analysis of Boolean algebra and its laws, supplemented with relevant examples. De Morgan's theorem and logic gate circuits are also examined with emphasis on practical applications. The chapter ends with a brief analysis of the real-life applications of digital circuits.

## 9-1 INTRODUCTION

The journey of digital electronics started in the year 1946 with the digital computer using vacuum tube technology. The term "digit" is derived from the counting operation of the computer. The twentyfirst century is the digital world. The devices common people use daily are mostly "digital" in their functions. Modern computer systems consist of digital components, starting from microprocessors to all other peripheral components. A binary digital circuit operates in two modes/states: ON state [1 (one)] and OFF state [0 (zero)]. These states are called binary states. These binary digits are called bits. In the binary digital world the logic lies between these two states; there is no intermediate state. This makes the digital states discrete in nature, whereas the analog states are continuous.

The evolution of digital electronics is a process of simultaneous development and simplification. The English scientist, George Boole, is known to be the inventor of Boolean algebra. Boolean algebra is the foundation of all contemporary computer arithmetic. In hindsight, Boole is regarded as one of the founders of computer science. Boolean algebra, developed by Boole in 1830, is a logical calculus of truth values.

The mathematician, Lewis Carroll, had formulated truth tables as early as 1894. Augustus De Morgan, the Indian-born British scientist, formulated the famous De Morgan's theorem, which was a simplification of the Boolean expressions. In 1952, the Karnaugh map was invented by Edward W. Veitch. The Karnaugh map is used to reduce the need for calculations. It was further developed in 1953 by Maurice Karnaugh, a telecommunications engineer at Bell Labs, to help simplify digital electronic circuits.

Digital logic can be of two different types-positive logic system and negative logic system. Generally, the digital circuits are connected with a dc supply battery (typically 5 V ) and a ground terminal of 0 V . If the 5 V refers to logic 1 or ON state and the ground 0 V refers to logic 0 or OFF state, the logic is referred to as positive logic. On the contrary, if 5 V referrers to logic 0 and ground 0 V referrers to logic 1 , then this logic is called negative logic.

## 9-2 NUMBER SYSTEM

The number system digits occupy certain relative positions having their relative positional significance. The left-most digit is called the most significant digit (MSD) and the right-most digit is called the lowest significant digit (LSD). Number systems are classified on the basis of radix/base, as shown in Table 9-1.

## 9-3 CONVERSION OF NUMBER SYSTEM

Conversion from one number system to another is an important aspect in digital electronics especially with respect to conversion from binary to decimal, decimal to binary, decimal to octal, decimal to hexadecimal, etc. Representation of a number in a system with base (radix) $N$ may only consist of digits that are less than $N$.

The base or radix of these number systems depends on the number of digit present in each number system. The binary system contains 0 and 1 , so its base is 2 . The decimal base is 10 and the hexadecimal base is 16 . The binary number system, having only two states, is the simplest way of calculating.

More accurately, if:

$$
M=a_{k} N^{k}+a_{k-1} N^{k-1}+\cdots+a_{1} N^{1}+a_{0}
$$

With $0 \leqslant a_{i}<N$ we have a representation of $M$ in base $N$ system, thus:

$$
M=\left(a_{k} a_{k-1} \ldots a_{0}\right)_{N}
$$

Table 9-1 Classification of number systems

| Binary | 0,1 |
| :--- | :--- |
| Ternary | $0,1,2$ |
| Quaternary | $0,1,2,3$ |
| Octal | $0,1,2,3,4,5,6,7$ |
| Decimal | $0,1,2,3,4,5,6,7,8,9$ |
| Hexadecimal | $0,1,2,3,4,5,6,7,8,9, A, B, C, D, E, F$ |

## 9-3-1 Binary to Decimal

Conversion from binary to decimal using decimal arithmetic is accomplished by simply summing the powers of 2 corresponding to the powers of 1 in the binary number.

## Conversion

$$
\begin{aligned}
1111= & 1 \times 10^{3}+1 \times 10^{2}+1 \times 10^{1}+1 \times 10^{0} \\
= & 1 \times 2^{3}+1 \times 2^{2}+1 \times 2^{1}+1 \times 2^{0} \\
& =8+4+2+1=15
\end{aligned}
$$

Similarly,

$$
\begin{aligned}
1110=1 & \times 10^{3}+1 \times 10^{2}+1 \times 10^{1}+0 \times 10^{0} \\
= & 1 \times 2^{3}+1 \times 2^{2}+1 \times 2^{1}+0 \times 2^{0} \\
= & 8+4+2+0=13
\end{aligned}
$$

For example, the binary number:

$$
10111=b_{4} b_{3} b_{2} b_{1} b_{0}
$$

This is converted to decimal by adding:

$$
\begin{aligned}
\mathrm{b}_{4} \times 2^{4}+ & b_{3} \times 2^{3}+b_{2} \times 2^{2}+b_{1} \times 2^{1}+b_{0} \times 2^{0} \\
& =b_{4} \times 16+b_{3} \times 8+b_{2} \times 4+b_{1} \times 2+b_{0} \times 1 \\
& =1 \times 16+0 \times 8+1 \times 4+1 \times 2+1 \times 1 \\
& =16+4+2+1 \\
& =(23) \text { decimal } \\
& =(23)_{10}
\end{aligned}
$$

## 9-3-2 Decimal to Binary

Conversion from decimal to binary using decimal arithmetic is accomplished by repeated division of the decimal number by two. After each division the remainder is the next bit of the binary number starting from the least significant.

For example, the decimal number (26):

$$
\begin{aligned}
26 / 2 & =13 \mathrm{R}=0=\mathrm{b}_{0} \\
13 / 2 & =6 \mathrm{R}=1=\mathrm{b}_{1} \\
6 / 2 & =3 \mathrm{R}=0=\mathrm{b}_{2} \\
3 / 2 & =1 \mathrm{R}=1=\mathrm{b}_{3} \\
1 / 2 & =0 \mathrm{R}=1=\mathrm{b}_{4} \\
0 / 2 & =0
\end{aligned}
$$

So (26) decimal $=(11010)$ binary .

$$
(26)_{10}=(11010)_{2}
$$

The decimal number (15):

So,

$$
\begin{gathered}
15 / 2=7 \mathrm{R}=1=\mathrm{b}_{0} \\
7 / 2=3 \mathrm{R}=1=\mathrm{b}_{1} \\
3 / 2=1 \mathrm{R}=1=\mathrm{b}_{2} \\
1 / 2^{1 / 2}=1 \mathrm{R}=1=\mathrm{b}_{3} \\
0 / 2=0 \\
(15)_{10}=(1111)_{2}
\end{gathered}
$$

## 9-3-3 Numer System Conversions

Conversions between binary and other number systems requires simple arithmetic computation. For example, the decimal number (19):

$$
19=1 \times 10+9 \times 1
$$

This is written as a binary number with:

$$
\begin{aligned}
10011=1 & \times 2^{4}+0 \times 2^{3}+0 \times 2^{2}+1 \times 2^{1}+1 \times 2^{0} \\
& =1 \times 16+0 \times 8+0 \times 4+1 \times 2+1 \times 1
\end{aligned}
$$

If this number is interpreted in groups of three bits, then each group of three can be interpreted as an octal digit, i.e., multiplying a power of 8 .

$$
\begin{aligned}
(10011)_{\text {binary }} & =1 \times 16+0 \times 8+0 \times 4+1 \times 2+1 \times 1 \\
& =(1 \times 16+0 \times 8)+(0 \times 4+1 \times 2+1 \times 1) \\
& =2 \times 8+3 \times 1 \\
& =(23)_{\text {octal }}
\end{aligned}
$$

Similarly, when groups of 4 bits are used, each group can be interpreted as a hexadecimal digit, i.e., multiplying a power of 16 .

$$
\begin{aligned}
(10011)_{\text {binary }} & =1 \times 16+0 \times 8+0 \times 4+1 \times 2+1 \times 1 \\
& =(1 \times 16)+(0 \times 8+0 \times 4+1 \times 2+1 \times 1) \\
& =1 \times 16+3 \times 1 \\
& =(13)_{\text {hexadecimal }}
\end{aligned}
$$

The octal numeral system is the base-8 number system, and uses the digits 0 to 7 . Numerals can be made from binary numerals by grouping consecutive digits into groups of three. For example, the binary representation for decimal 74 is 1001010 , which groups into 001001010 so the octal representation is 112. In decimal systems each decimal place is a base of 10 .

$$
\therefore \quad 74=7 \times 10^{1}+4 \times 10^{0}
$$

In octal numerals each place is a power with base 8 .

$$
\therefore \quad 112=1 \times 8^{2}+1 \times 8^{1}+2 \times 8^{0}
$$

By performing the calculation decimal system we see how 112 in octal is equivalent to $64+8+2=74$ in decimal.

Table 9-2 Conversion of decimal to hexadecimal to octal to binary

| $D E C$ | $H E X$ | $O C T$ | BIN |
| :---: | :---: | :---: | :---: |
| 0 | 0 | 000 | 00000000 |
| 1 | 1 | 001 | 00000001 |
| 2 | 2 | 002 | 00000010 |
| 3 | 3 | 003 | 00000011 |
| 4 | 4 | 004 | 00000100 |
| 5 | 5 | 005 | 00000101 |
| 6 | 6 | 006 | 00000110 |
| 7 | 7 | 007 | 00000111 |
| 8 | 8 | 010 | 00001000 |
| 9 | 9 | 011 | 00001001 |
| 10 | A | 012 | 00001010 |
| 12 | B | 013 | 00001011 |
| 13 | C | 014 | 00001100 |
| 14 | D | 015 | 00001101 |
| 15 | E | 016 | 00001110 |

The conversion from decimal to hexadecimal to octal to binary is shown in Table 9-2.

## 9-4 BOOLEAN ALGEBRA

The working principle of the digital circuit is guided by Boolean algebra. Boolean algebra functions through addition, subtraction and its five basic laws.

## 9-4-1 Addition

Boolean addition uses the addition process with binary numbers- 0 's and 1's. Various combinations of binary addition are shown in Table 9-3. The general form of addition of two binary numbers, say $A$ and $B$ produce a sum $(S)$ and a carry $\left(C_{y}\right)$ as shown here.

$$
\begin{array}{r}
A \\
+\quad B \\
\hline C_{y} S
\end{array}
$$

(Carry) (Sum)
Table 9-3 Binary addition

| 0 | 0 | 1 | 1 |
| :---: | :---: | :---: | :---: |
| +0 | +1 | +0 | +1 |
| 00 | 01 | 01 | 10 |

9-6 | Basic Electronics

Examples of binary addition:
(i) $A(10001)+B(11101)=C(101110)$

|  | 1 |  |  |  | 1 |  | $\rightarrow$ | Carry |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| + |  | 1 | 0 | 0 | 0 | 1 | $A$ |  |
| + |  | 1 | 1 | 1 | 0 | 1 | $B$ |  |
|  | 1 | 0 | 1 | 1 | 1 | 0 | $C$ |  |

(ii) $A(101101)+B(11001)=C(1000110)$

|  | 1 | 1 | 1 |  |  | 1 |  | $\rightarrow$ | Carry |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| + |  | 1 | 0 | 1 | 1 | 0 | 1 | $A$ |  |
| + |  |  | 1 | 1 | 0 | 0 | 1 | $B$ |  |
|  | 1 | 0 | 0 | 0 | 1 | 1 | 0 | $C$ |  |

(iii) $A(1011001)+B(111010)=C(10010011)$

|  | 1 | 1 | 1 | 1 |  |  |  |  | $\rightarrow$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  |  |  |  |  |  |  |
|  |  | 1 | 0 | 1 | 1 | 0 | 0 | 1 | $A$ |
| + |  |  | 1 | 1 | 1 | 0 | 1 | 0 | $B$ |
|  | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | $C$ |

(iv) $A(1110)+B(1111)=C(11101)$

|  | 1 | 1 | 1 |  | $\rightarrow$ | Carry |
| :---: | :--- | :--- | :--- | :--- | :--- | :--- | :--- |
| + |  | 1 | 1 | 1 | 0 | $A$ |
|  |  | 1 | 1 | 1 | 1 | $B$ |
|  | 1 | 1 | 1 | 0 | 1 | $C$ |

(v) $A(10111)+B(110101)=C(1001100)$

|  | 1 | 1 |  | 1 | 1 | 1 |  | $\rightarrow$ | Carry |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | 1 | 0 | 1 | 1 | 1 | $A$ |  |
| + |  | 1 | 1 | 0 | 1 | 0 | 1 | $B$ |  |
|  | 1 | 0 | 0 | 1 | 1 | 0 | 0 | $C$ |  |

(vi) $A(11011)+B(1001010)=C(1100101)$

|  |  | 1 | 1 |  | 1 |  |  | $\rightarrow$ Carry |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | 1 | 1 | 0 | 1 | 1 | $A$ |
| + | 1 | 0 | 0 | 1 | 0 | 1 | 0 | $B$ |
|  | 1 | 1 | 0 | 0 | 1 | 0 | 1 | $C$ |

Table 9-4 Binary subtraction

| 0 | 1 | 0 | 1 |
| ---: | ---: | ---: | ---: |
| -0 | -0 | -1 | -1 |
| 00 | 01 | 10 | 00 |

## 9-4-2 Subtraction

Boolean subtraction binary numbers- 0 's and 1's, is shown in Table 9-4. The general form of subtraction of two binary numbers $A$ and $B$ produce a difference $(D)$ and a borrow, as shown here.

$$
\begin{gathered}
A \\
-\quad B \\
\hline B_{r} D \\
(\text { Borrow) }(\text { Difference })
\end{gathered}
$$

Examples of binary subtraction:
(i) $A(1011011)-B(10010)=C(1001001)$

|  | 1 | 0 | 1 | 1 | 0 | 1 | 1 | $A$ |
| :---: | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- |
| - |  |  | 1 | 0 | 0 | 1 | 0 | $B$ |
|  | 1 | 0 | 0 | 1 | 0 | 0 | 1 | $C$ |

(ii) $A(1010110)-B(101010)=C(101100)$

|  |  |  |  |  |  |  |  |
| ---: | ---: | ---: | ---: | ---: | ---: | ---: | ---: |
|  | $\times 1$ | 10 | $\times 1$ | 10 | 1 | 1 | 0 |

(iii) $A(1000101)-B(101100)=C(11001)$

| 0 | 1 | 1 |  |  |  | $\rightarrow$ | Borrow |
| ---: | ---: | ---: | ---: | ---: | ---: | ---: | ---: |
| - | $\times 1$ | $\times 10$ | $\times 10$ | 10 | 1 | 0 | 1 |
| $A$ |  |  |  |  |  |  |  |
|  | 1 | 0 | 1 | 1 | 0 | 0 | $B$ |
|  | 1 | 1 | 0 | 0 | 1 | $C$ |  |

(iv) $A(100010110)-B(1111010)=C(10011100)$

(v) $A(101101)-B(100111)=C(110)$

|  |  |  |  |  |  |  |  |
| ---: | ---: | ---: | ---: | ---: | ---: | ---: | ---: |
|  |  |  | 0 | 10 |  |  | $\rightarrow$ |
| Borrow |  |  |  |  |  |  |  |
| - | 0 | $\times 1$ | $\times 1$ | $(1) 0$ | 1 | $A$ |  |
|  | 0 | 0 | 1 | 1 | 1 | $B$ |  |

(vi) $A(1110110)-B(1010111)=C(11111)$

|  |  | 0 | 10 | 1 | 10 | 10 |  | $\rightarrow$ |
| ---: | ---: | ---: | ---: | ---: | ---: | ---: | ---: | ---: |
|  | 1 | $\times 1$ | $\times 1$ | $\times 10$ | $\times 1$ | $\times 1$ | 10 | $A$ |
| - | 1 | 0 | 1 | 0 | 1 | 1 | 1 | $B$ |

## 9-4-3 Basic Boolean Laws

Every law has two expressions-(a) and (b). This is known as duality. These are obtained by changing every AND (.) to OR ( + ); every OR (+) to AND (.); and all 1's to 0's and vice-versa. It has become conventional to drop (.)-the AND symbol, i.e., $A . B$ is written as $A B$. Some of the very important laws are as follows:

- Commutative Law
(a) $A+B=B+A$
(b) $A B=B A$
- Associate Law
(a) $(A+B)+C=A+(B+C)$
(b) $(A B) C=A(B C)$
- Distributive Law
(a) $A(B+C)=A B+A C$
(b) $A+(B C)=(A+B)(A+C)$
- Identity Law
(a) $A+A=A$
(b) $A A=A$
- Redundance Law
(a) $A+A B=A$
(b) $A(A+B)=A$
- Inverse Law
(a) $A+\bar{A}=1$
(b) $A \cdot \bar{A}=0$


## 9-5 LOGIC GATES

The basic elements of digital circuits are logic gates. Logic circuits are generally designed with BJT, FET and CMOS circuits having many inputs and a single output. The output will be either logic high (1) or logic low (0) depending on the combination of input logic high and low. Logic gates have the ability of making logic decisions by producing a particular output under certain input. The functional behaviour of a logic gate is realized by the three processes, as explained in the following sections.

Table 9-5 Truth table of AND logic

| Input | Output |  |
| :---: | :---: | :---: |
| $A$ | $B$ | $Y$ |
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

The output $Y$ of the AND gate is high or 1 when both the inputs $A$ and $B$ are high. If any of the two inputs is low, the output becomes low. Logic equation for AND gate is $Y=A B$

1. Truth Table: Truth table is a prescribed specification table that explains the input-output relation for all possible combination of inputs.
2. Logic Equation: In logic equations, the output is expressed in terms of input according to the truth table. Logic equations are generally unique as truth tables vary from logic to logic.
3. Timing Diagram: Timing diagram of a logic gate indicates the variation of the output waveform with respect to the input waveform. It is a pictorial representation of the time-varying input and output of the logic gate.

## 9-5-1 AND Gate

The AND gate has two or more inputs. Its output is logic high (1) only when both the inputs are at logic high (1). The truth table of an AND gate is shown in Table 9-5 and logic symbol is shown in Figure 9-1.


Figure 9-1 Logic symbol for AND gate


Figure 9-2 Logic symbol of OR Gate

## 9-5-2 OR Gate

The OR gate is a two or more input logic gate. Its output is logic high (1) if any of the inputs are high (1). The truth table of an OR gate is shown in Table 9-6 and logic symbol is shown in Figure 9-2.

Table 9-6 Truth table of OR logic

| Input |  | Output |
| :---: | :---: | :---: |
| $A$ | $B$ | $Y$ |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

The output of the OR gate $Y$ is high when any of the inputs $A$ and $B$ is high or when both the inputs are high.
Logic equation for OR gate is $Y=A+B$

Table 9-7 Truth table of NOT logic

| Input | Output |
| :---: | :---: |
| 0 | 1 |
| 1 | 0 |

The output $Y$ of the NOT gate is the complement of the input $A$
Logic equation for NOT gate is $Y=\bar{A}$

## 9-5-3 NOT Gate

The NOT gate is a single input and single output gate, which performs a basic logical inversion/complementation operation. The truth table of a NOT gate is shown in Table 9-7 and the logic symbol is shown in Figure 9-3.

## 9-5-4 NAND Gate

The NAND gate is a two or more input logic gate. Its output is logic low (0) only when both the inputs are at logic (1). The truth table of a NAND gate is shown in Table 9-8 and logic symbol is shown in Figure 9-4.

## 9-5-5 NOR Gate

The NOR gate is a two or more input logic gate. Its output is logic high (1) both the inputs are at logic low (0). The truth table of a NOR gate is shown in the Table 9-9 and the logic symbol is shown in Figure 9-5.


Figure 9-3 Logic symbol of NOT gate


Figure 9-4 Logic symbol of NAND gate


Figure 9-5 Logic symbol of NOR gate

Table 9-8 Truth table of NAND logic

| Input | Output |  |
| :---: | :---: | :---: |
| $A$ | $B$ | $Y$ |
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

NAND, which is a contraction of NOT and AND (AND gate followed by an inverter) gates, has a low output, $Y$, when the two inputs $A$ and $B$ are both high. For all other inputs the output is high.

Logic equation for NAND gate is $Y=\overline{A B}$

Table 9-9 Truth table of NOR logic

| Input | Output |  |
| :---: | :---: | :---: |
| $A$ | $B$ | $Y$ |
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

NOR is the contraction between NOT and OR gates (OR gate followed by an inverter). The output $Y$ of the NOR gate is high only when the two inputs $A$ and $B$ are low.

Logic equation for NOR gate is $Y=\overline{A+B}$

## 9-5-6 XOR Gate

XOR gate is a two or more input logic gate. Its output is logic high (1) if only one of the input is at logic high. The truth table of a XOR gate is shown in Table 9-10 and the logic symbol is shown in Figure 9-6.


Figure 9-6 Logic symbol of XOR Gate

## 9-5-7 XNOR Gate

XNOR gate is a two or more input logic gate. Its output is logic high (1) if both the inputs are either logic high or logic low. The truth table of XNOR gate is shown in Table 9-11 and the logic symbol is shown in Figure 9-7.


Figure 9-7 Logic symbol of XNOR gate

## 9-5-8 Universal Gate

NAND and NOR gates are called universal, as all the basic logic AND, OR and NOT gates can be designed/realized through a combination of NAND/NOR. The design of AND, OR and NOT gates using NAND and NOR gates is shown in Figures 9-8 and 9-9 respectively.

Table 9-10 Truth table of XOR logic

| Input | Output |  |
| :---: | :---: | :---: |
| $A$ | $B$ | $Y$ |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

The exclusive-OR gate or the XOR gate has a high output state only when one and only one of the two inputs $A$ and $B$ is high.

Logic equation for XOR gate is $Y=\bar{A} B+A \bar{B}$

Table 9-11 Truth table of XNOR logic

| Input | Output |  |
| :---: | :---: | :---: |
| $A$ | $B$ | $Y$ |
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

The Exclusive-NOR gate or XNOR is an XOR gate followed by an inverter. The output $Y$ is high if both the inputs $A$ and $B$ have the same logic state. Logic equation for XNOR gate is $Y=A B+\overline{B A}$


NOT gate using NAND


AND gate using NAND


OR gate using NAND


NOR gate using NAND


XOR gate using NAND
Figure 9-8 NAND as universal gate


Figure 9-9 NOR as universal gate

## 9-5-9 Characteristics of Logic Gates

The characteristic features of logic gates are as follows:

## Fan-out

The measure of the maximum number of logic gates that can be driven by a single logic gate without affecting the specified operational characteristics of the driving gate is called fan-out. A standard fan-out for TTL is ten (10).

## Fan-in

The measure of the maximum possible number of inputs that can be connected to a logic gate without affecting the specified operational characteristics of the driven logic gate is called fan-in. A standard fan-in for TTL is ten (10).

## Propagation delay

The time taken by an input signal to pass through a logic gate and emerge from the output is known as propagation delay. A typical delay time for a TTL logic gate is 30 nsec .

## Power dissipation

The power consumed by a logic gate is known as power dissipation.

## Noise

The unwanted input signal in a logic gate is known as noise.

## Noise margin

The maximum level of noise voltage allowed at the input without affecting the output is the noise margin.

## 9-6 DE MORGAN'S THEOREM

De Morgan developed a pair of important rules concerning group complementation in Boolean algebra. Through group complementation, the complement of the logical sum of a number of binary variables is equal to the logical product of the complements of all the individual variables. For all elements $A$ and $B$ of the set $S$ :
(i) $\overline{A B}=\bar{A}+\bar{B}$
(ii) $\overline{A+B}=\bar{A} \bar{B}$

## 9-6-1 Using Basic Logic Gates

Figure 9-10 illustrates the proof of De Morgan's theorem.

$$
\overline{A B}=\bar{A}+\bar{B}
$$



In other way:


| $A$ | $B$ | $Z$ |
| :---: | :---: | :---: |
| $\bar{A}$ | $\bar{B}$ | $Z$ |
| $\bar{A}$ | $B$ | $Z$ |
| $A$ | $\bar{B}$ | $Z$ |
| $A$ | $B$ | $\bar{Z}$ |


| $A$ | $B$ | $Z$ |
| :---: | :---: | :---: |
| $\bar{A}$ | $\bar{B}$ | $Z$ |
| $\bar{A}$ | $B$ | $Z$ |
| $A$ | $\bar{B}$ | $Z$ |
| $A$ | $B$ | $\bar{Z}$ |

Figure 9-10 Proof of De Morgan's theorem


| $A$ | $B$ | $Z$ |
| :---: | :---: | :---: |
| $\bar{A}$ | $\bar{B}$ | $Z$ |
| $\bar{A}$ | $B$ | $\bar{Z}$ |
| $A$ | $\bar{B}$ | $\bar{Z}$ |
| $A$ | $B$ | $\bar{Z}$ |

$\bar{A} \bar{B}=\overline{A+B}$

| $A$ | $B$ | $Z$ |
| :---: | :---: | :---: |
| $\bar{A}$ | $\bar{B}$ | $Z$ |
| $\bar{A}$ | $B$ | $\bar{Z}$ |
| $A$ | $\bar{B}$ | $\bar{Z}$ |
| $A$ | $B$ | $\bar{Z}$ |

Figure 9-11 Proof of De Morgan's theorem
The complement of the logical product of a number of binary variables is equal to the logical sum of the complements, as shown in Figure 9-11.

$$
\overline{A B}=\bar{A}+\bar{B}
$$

## 9-6-2 Application of De Morgan's Theorem

This theorem is used for the simplification of Boolean expressions in a simplest and smallest form of equivalent circuit. De Morgan's theorem describes the equality between gates with inverted inputs and gates with inverted outputs. For example, a NAND gate is equivalent to a negative OR gate, and a NOR gate is equivalent to a negative AND gate. When "breaking" a complementation bar in a Boolean expression, the operation directly underneath the break reverses, and the broken bar pieces remain over the respective terms. Complementation bars function as grouping symbols. So, when a bar is broken, the terms underneath it must remain grouped.

## 9-7 SIMPLIFICATION OF BOOLEAN EXPRESSION

Simplification of Boolean expressions can be done by the algebraic method or by the Karnough Map method. Karnough Map is one of the simplest methods of solving the four variable algebraic equations. In this chapter we will discuss simplification using the algebraic method only.
(i)

$$
\begin{aligned}
& A+A C \\
& =A(1+C) \\
& =A 1 \\
& =A
\end{aligned}
$$

(ii)

$$
\begin{aligned}
& A+\bar{A} B \\
& =(A+\bar{A})(A+B) \\
& =1(A+B) \\
& =(A+B)
\end{aligned}
$$

(iii)

$$
\begin{aligned}
& A+\bar{A} B+A B \bar{C} \\
& =A(1+B \bar{C})+\bar{A} B \\
& =A 1+\bar{A} B \\
& =A+\bar{A} B \\
& =(A+\bar{A})(A+B) \\
& =1(A+B) \\
& =(A+B)
\end{aligned}
$$

(iv)
(v)

$$
\begin{aligned}
& A+\bar{A} B+A B C+\bar{A} C \\
& =(A+\bar{A})(A+B)+C(A B+\bar{A}) \\
& =1(A+B)+C(A+\bar{A}) \\
& =(A+B)+C \\
& =A+B+C
\end{aligned}
$$

$$
\begin{aligned}
& \bar{A} \bar{B} C+A C+A B C+A B \\
& =\bar{A} \bar{B} C+A C+A B(C+1) \\
& =\bar{A} \bar{B} C+A C+A B \\
& =C(\bar{A} \bar{B}+A)+A B \\
& =C(\bar{A}+A)(\bar{B}+A)+A B \\
& =C 1(\bar{B}+A)+A B \\
& =C(\bar{B}+A)+A B \\
& =C \bar{B}+C A+A B
\end{aligned}
$$

(vi)

$$
\begin{aligned}
& A C+\bar{A} \bar{C} \\
& =\bar{A} C+\bar{A}+\bar{C} \\
& =\bar{A}(C+1)+\bar{C} \\
& =\bar{A} 1+\bar{C} \\
& =\bar{A}+\bar{C}
\end{aligned}
$$

(vii)

$$
\begin{aligned}
& A B+B C+B \bar{C}+A C \\
& =A B+A C+B(C+\bar{C}) \\
& =A B+A C+B \\
& =B(A+1)+A C \\
& =B 1+A C \\
& =B+A C
\end{aligned}
$$

(viii)

$$
\begin{aligned}
& \overline{A \bar{B}+\bar{A} B} \\
& =\overline{\bar{A} B} \overline{A \bar{B}} \\
& =(\overline{\bar{A}}+\bar{B})(\bar{A}+\overline{\bar{B}}) \\
& =(A+\bar{B})(\bar{A}+B) \\
& =A \bar{A}+\bar{A} \bar{B}+A B+B \bar{B} \\
& =\bar{A} \bar{B}+A B
\end{aligned}
$$

(ix)
(x)
(xi)
(xii)
(xiii)

$$
\begin{aligned}
& \overline{A B+\overline{A B}+A} \\
& =\overline{\overline{A B}} \overline{\bar{A}} \overline{A B} \\
& =A B A(\bar{A}+\bar{B}) \\
& =A B(\bar{A}+\bar{B}) \\
& =A \bar{A} B+A B \bar{B} \\
& =0+0=0
\end{aligned}
$$

$A B+\bar{A}+\overline{A B}$
$=A B+\bar{A}+\bar{A}+\bar{B}$
$=A B+\bar{A}+\bar{B}$
$=A B+\overline{A B}$
$=1$
$\overline{(\bar{A}+C)(B+\bar{D})}$
$=\overline{(\bar{A}+C)} \overline{(B+\bar{D})}$
$=\overline{\bar{A}} \bar{C}+\bar{B} \overline{\bar{D}}$
$=A \bar{C}+\bar{B} D$
$(B+\bar{C})(\bar{B}+C)+\overline{\bar{A}+B+\bar{C}}$
$=B \bar{B}+\bar{B} \bar{C}+C \bar{C}+B C+\overline{\bar{A}} \bar{B} \overline{\bar{C}}$
$=\bar{B} \bar{C}+B C+A \bar{B} C$
$=\bar{B} \bar{C}+(B+A \bar{B}) C$
$=\bar{B} \bar{C}+(B+\bar{B})(B+A) C$
$=\bar{B} \bar{C}+(B+A) C$
$=\bar{B} \bar{C}+B C+A C$
$\overline{\overline{A+B}+\bar{C}}$
$=\overline{A(\overline{A+B})} \overline{\bar{C}}$
$=(A+B) C=A C+B C$

## 9-8 LOGIC GATE CIRCUITS

Logic gate circuits are divided into two categories based on whether they are with feedback sequential logic circuit or without feedback combinational logic circuit. Thus, digital electronics is classified into combinational logic and sequential logic. Combinational logic output depends on the inputs levels, whereas sequential logic output depends on stored levels of past data and also the present input levels.

## 9-8-1 Combinational Logic

Combinational logic circuit is used to realize different logic functions using different basic logic gates.

## Adder

Adder is a combinational logic circuit is used to add two or more bits.

## Half adder

Half adder is a combinational logic circuit, which is used to add two bits and generate output as sum $(S)$ and carry $\left(C_{y}\right)$. The truth table of half adder is shown in Table 9-12 and the circuit diagram is shown in Figure 9-12.

## Full adder

Full adder is a combinational logic circuit used to add three or more bits. The reason for the name full adder is that it can add the carry bit as third bit $\left(C_{\text {in }}\right)$ along with other two inputs $A$ and $B$. The truth table of full adder is shown in the Table 9-13 and circuit diagram is shown in Figure 9-13.

From the truth table as given in Table 9-12, we can write sum:

$$
S=A \oplus B
$$

And carry: $\quad C_{y}=A B$
A half adder has two inputs and the two bits to be added. The output of the XOR gate is the sum of the two bits and the output of the AND gate is the carry. The full adder produces a sum and carrier values, which are both binary digits. The expression of the sum and carry, is given by:

$$
S=(A \oplus B) \oplus C_{\mathrm{in}}
$$

The full adder takes three inputs. The two inputs A and B are the two bits to be added while the third input is the carry from the previous lower significant position. The output of the XOR gate is the sum while the output of the OR gate is the carry.


Figure 9-12 Block diagram of half adder

Table 9-12 Truth table of half adder

| Input |  | Output |  |
| :---: | :---: | :---: | :---: |
| $A$ | $B$ | $C_{y}$ | $S$ |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 |

Table 9-13 Truth table of full adder

| Input |  |  | Output |  |
| :---: | :---: | :---: | :---: | :---: |
| $A$ | $B$ | $C_{\text {in }}$ | $C_{y}$ | $S$ |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 1 | 1 |



Figure 9-13 Circuit diagram of full adder


Figure 9-14 Block diagram of a multiplexer


Figure 9-15 Circuit diagram of a multiplexer

A full adder can be constructed from two half adders by connecting $A$ and $B$ to the input of one half adder, connecting the sum from that to an input to the second adder, connecting $C_{\text {in }}$ to the other input and OR the two carry outputs. Equivalently, sum $S$ is expressed by a 3-bit XOR of $A, B$, and $C_{\mathrm{in}}$; and $C_{\text {out }}$ could be made the 3-bit majority function of $A, B$, and $C_{\mathrm{in}}$.

$$
\begin{aligned}
C_{y} & =\bar{A} B C_{\mathrm{in}}+A \bar{B} C_{\mathrm{in}}+A B \bar{C}_{\mathrm{in}}+A B C_{\mathrm{in}} \\
& =C_{\mathrm{in}}(\bar{A} B+A \bar{B})+A B\left(\bar{C}_{\mathrm{in}}+C_{\mathrm{in}}\right) \\
& =C_{\mathrm{in}}(A \oplus B)+A B
\end{aligned}
$$

## Multiplexer

Multiplexer means "path selector"; it has many inputs, a single output and select input signals. A multiplexer has $n$ number of select inputs, $2^{n,}$ inputs, and only one output. The truth table of a multiplexer is shown in the Table 9-14, and the block diagram is given in Figure 9-14, The circuit diagram of a multiplexer is shown in Figure 9-15.

If we introduce enable input $E_{n}$ then the equation becomes:

$$
Y=\left(\overline{S_{1}} \bar{S}_{0} I_{0}+\bar{S}_{1} S_{0} I_{0}+S_{1} \bar{S}_{0} I_{2}+S_{1} S_{0} I_{3}\right) E_{n}
$$

A 4-to-1 multiplexer can be implemented by using two inverters, four AND gates and a 4-input OR gate. To each of the AND gates any of the data input lines and the corresponding select lines are applied, and the output of all the AND gates are applied, to the OR gate to get the output.

## De-multiplexer

De-multiplexer operation is the opposite to that of the multiplexer. It has $n$ number of select inputs,

Table 9-14 Truth table of multiplexer

| Select Input |  | Output |
| :---: | :---: | :---: |
| $S_{1}$ | $S_{0}$ | $Y$ |
| 0 | 0 | $I_{0}$ |
| 0 | 1 | $I_{1}$ |
| 1 | 0 | $I_{2}$ |
| 1 | 1 | $I_{3}$ |


| Table 9-15 |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Select Inputh table of de-multiplexer |  |  |  |  |  |
| $S_{1}$ | $S_{1}$ | $Y_{0}$ | $Y_{1}$ | $Y_{2}$ | $Y_{3}$ |
| 0 | 0 | $D$ | 0 | 0 | 0 |
| 0 | 0 | 0 | $D$ | 0 | 0 |
| 1 | 1 | 0 | 0 | $D$ | 0 |
| 1 | 1 | 0 | 0 | 0 | $D$ |



Figure 9-16 Block diagram of de-multiplexer


Figure 9-17 Circuit diagram of de-multiplexer
$2^{n}$ outputs and only one select input. The truth table of de-multiplexer is shown in Table 9-15 and the block diagram is shown in Figure 9-16. The circuit diagram is shown in Figure 9-17.

Considering a common data input $D$ for the de-multiplexer, we can write the following logic expressions for all four outputs from the truth table:

$$
\begin{aligned}
& Y_{0}=\overline{S_{1}} \overline{S_{0}} D \\
& Y_{1}=\overline{S_{1}} S_{0} D \\
& Y_{2}=S_{1} \overline{S_{0}} D \\
& Y_{3}=S_{1} S_{0} D
\end{aligned}
$$

A 1-to-4 demultiplexer can be implemented by two inverters and four 3-input AND gates. The single input $D$ is applied to all the AND gates. The two select lines $S_{1}$, $S_{0}$ enable any one AND gate at a time and the data appears at the output of the selected AND gate as shown in Figure 9-17.

## Encoder

An encoder is a combinational logic circuit which converts non-digital data to digital data. An encoder has $2^{n}$ input lines and $n$ output lines.The output lines generate a binary code corresponding to the input value. For example a single bit 4-to-2 encoder takes in 4 bits and outputs 2 bits. An encoder combinational circuit that performs the inverse operation of a decoder. The truth table of an encoder is shown in Table 9-16 and the block diagram is shown in Figure 9-18. The circuit diagram is shown in Figure 9-19.


Figure 9-18 Block diagram of encoder


Figure 9-19 Circuit diagram of an octal-tobinary encoder

Table 9-16 Truth table of encoder

| Input |  |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $D_{0}$ | $D_{1}$ | $D_{2}$ | $D_{3}$ | $D_{4}$ | $D_{5}$ | $D_{6}$ | $D_{7}$ | $Y_{2}$ | $Y_{1}$ | $Y_{0}$ |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |

For an 8-to-3 binary encoder with inputs $D_{0}-D_{7}$ the logic expressions of the outputs $Y_{0}-Y_{2}$ are:

$$
\begin{aligned}
& Y_{0}=D_{1}+D_{3}+D_{5}+D_{7} \\
& Y_{1}=D_{2}+D_{3}+D_{6}+D_{7} \\
& Y_{2}=D_{4}+D_{5}+D_{6}+D_{7}
\end{aligned}
$$

Octal-to-binary takes 8 inputs and provides 3 outputs. At any one time, only one input line has a value of 1 .

An octal to binary encoder can be implemented using three 4 -input OR gates. The encoder accepts a 3-bit input code and activates one of the eight output lines $\left(D_{0}-D_{7}\right)$ corresponding to the input code.

## Decoder

Decoder is combinational logic circuit multiple-input, multiple-output logic circuit which converts digital data to non-digital data. The truth table of decoder is shown in Table 9-17 and the block diagram is shown in Figure 9-20. The circuit diagram is shown in Figure 9-21.


Figure 9-20 Block diagram of a decoder


Figure 9-21 Circuit diagram of a 3-to-8 decoder

Table 9-17 Truth table of decoder

| Input |  |  | Output |  |  |  |  |  |  |  |
| :---: | :---: | :--- | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $A$ | $B$ | $C$ | $D_{0}$ | $D_{1}$ | $D_{2}$ | $D_{3}$ | $D_{4}$ | $D_{5}$ | $D_{6}$ | $D_{7}$ |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

A 3-to-8 decoder consists of three inputs and eight outputs.
A 3-to-8 decoder is implemented using three inverters and eight 3-input AND gates, as shown in Figure 9-21. The three inputs $A, B, C$-are decoded into eight outputs. Each one of the AND gates produce one minterms of the input variables.

## Applications of the decoder

1. Any $n$-variable logic function, in canonical sum-of-minterms form can be implemented using a single $n$-to- $2^{n}$ decoder to generate the minterms, and an OR gate to form the sum.
2. The output lines of the decoder corresponding to the minterms of the function are used as inputs to the OR gate.
3. Any combinational circuit with $n$ inputs and $m$ outputs can be implemented with an $n$-to- $2^{n}$ decoder with $m$ OR gates.
4. A decoder is suitable when a circuit has many outputs, and each output function is expressed with few minterms. For example, we can implement a full adder with sum:

$$
S(x, y, z)=(1,2,4,7)
$$

And carry:

$$
C_{y}(x, y, z)=(3,5,6,7)
$$

## 9-8-2 Sequential Logic Circuit

Sequential logic circuit is a clock-driven feedback-based circuit, where the present output is a combination of the present input and previous output. Sequential circuits have loops that enable these circuits to receive feedback. Combinational circuits have no memory. In order to build sophisticated digital logic circuits, including computers, we need circuits whose output depends both upon the input of the circuit and its previous state. Therefore, we need circuits that have memory. For a device to serve as a memory, it must have these following characteristics:

1. The device must have two stable states
2. There must be a way to read the state of the device
3. There must be a way to set the state


Figure 9-22 Block diagram of a sequential circuit

It is possible to produce circuits with memory using the digital logic gates that use feedback (see Figure 9-22). The memory elements are devices capable of storing binary information. The binary information stored in the memory elements at any given time defines the state of the sequential circuit. The present input and the state of the memory element determine the output.

There are two types of sequential circuits. Their classification depends on the timing of their signals.

1. Asynchronous sequential circuits: The outputs at any stage of this kind of circuit depend on the previous output stage, and all the outputs do not change their state at the same time.
2. Synchronous sequential circuits: All the stage flip-flops are connected together at the same time; and all stage outputs change at the simultaneously.

## Latch

Latch is a level sensitive sequential circuit with bistable states. The simplest latch is an S-R latch having two inputs- $S$ and $R$, and output $Q$. The complement form of the S-R latch is shown in Figure 9-23 and Figure 9-24 shows the circuit diagram. The S-R latch circuit is a cross-coupled latch with direct feedback from its output $Q$ and $Q^{\prime}$.

## Flip-flop

Flip-flop is an edge sensitive sequential logic circuit. All the flip-flops (FF) are driven by a clock-a feature that is not available in latch. Change of state in FF happens at the rising or falling edge of the clock pulse, but in case of latch it is level sensitive, i.e., in latch, change of state occurs depending upon 1 or 0 state only, but latch is not sensitive to rising or falling edge of the clock pulse. A general block diagram of FF is shown in Figure 9-25.


Figure 9-23 Block diagram of latch


Figure 9-24 Circuit diagram of latch


Figure 9-25 Block diagram of flip-flop

A sequential circuit which has only two states, 1 or 0 , is a flip-flop. The two outputs are complimentary to each other. There are different types of flips flops depending on their inputs and clock pulses that produce transition between two states. These are as follows:

1. Set-Reset Flip-Flop or S-R FF: The S-R FF has two inputs- $S$ and $R . S$ is called set and $R$ is called reset. The $S$ input is used to produce HIGH on $Q$, i.e., store binary 1 in flip-flop. The $R$ input is used to produce LOW on $Q$, i.e., store binary 0 in flip-flop. $Q^{\prime}$ is $Q$ complementary output. The output of the S-R latch depends on current as well as previous stored output. The circuit and the truth table of the S-R latch is shown in Table 9-18 and circuit diagram is shown in Figure 9-26.


Figure 9-26 Circuit diagram of flip-flop

Condition I. $\mathbf{S}=\mathbf{0}$ and $\mathbf{R}=\mathbf{0}$ : If we assume $Q=1$ and $Q^{\prime}=0$ as initial condition, then output $Q$ after input is applied would be $Q=\left(R+Q^{\prime}\right)^{\prime}=1$ and $Q^{\prime}=(\mathrm{S}+Q)^{\prime}=0$. Assuming $Q=0$ and $Q^{\prime}=1$ as the initial condition, then output $Q$ after the input applied would be $Q=\left(R+Q^{\prime}\right)^{\prime}$ $=0$ and $Q^{\prime}=(S+Q)^{\prime}=1$. So it is clear that when both $S$ and $R$ inputs are LOW, the output is retained as before the application of inputs, i.e., there is no state change.

Table 9-18 State table of SR flip-flop

| Input |  | Present Output <br> State |  | Next Output Input <br> State |
| :---: | :---: | :---: | :---: | :--- |
| $S$ | $R$ | $Q$ | $Q+$ | Comments |
| 0 | 0 | 0 | 0 | No change, i.e., Hold state/mode |
| 0 | 0 | 1 | 1 | No change, i.e., Hold state/mode |
| 0 | 1 | X | 0 | Reset state |
| 1 | 0 | X | 1 | Set state |
| 1 | 1 | X | 0 | Forbidden state |

The operation of S-R flip-flop has to be analysed with the 4 input combinations together with the 2 possible previous states.

Table 9-19 State table of direct/delay flip-flop

| Input | Present Output State | Next Output State | Comments |
| :---: | :---: | :---: | :--- |
| $D$ | $Q$ | $Q+$ |  |
| 1 | X | 1 | Set state |
| 0 | X | 0 | Reset state |

Condition II. $\mathbf{S}=\mathbf{1}$ and $\mathbf{R}=\mathbf{0}$ : $\quad$ If we assume $Q=1$ and $Q^{\prime}=0$ as, initial condition, then output $Q$ after input is applied would be $Q=\left(R+Q^{\prime}\right)^{\prime}=1$ and $Q^{\prime}=(S+Q)^{\prime}=0$. Assuming $Q=0$ and $Q^{\prime}=1$ as the initial condition, then output $Q$ after the input applied would be $Q=\left(R+Q^{\prime}\right)^{\prime}=1$ and $Q^{\prime}=(S+Q)^{\prime}=0$. So in simple words when $S$ is HIGH and $R$ is LOW, output $Q$ is HIGH.

Condition III. $\mathbf{S}=\mathbf{0}$ and $\mathbf{R}=\mathbf{1}$ : If we assume $Q=1$ and $Q^{\prime}=0$ as the initial condition, then output $Q$ after input is applied would be $Q=\left(R+Q^{\prime}\right)^{\prime}=0$ and $Q^{\prime}=(S+Q)^{\prime}=1$. Assuming $Q=0$ and $Q^{\prime}=1$ as the initial condition, then output $Q$ after the input applied would be $Q=\left(R+Q^{\prime}\right)^{\prime}=0$ and $Q^{\prime}=(S+Q)^{\prime}=1$. So in simple words, when $S$ is LOW and $R$ is HIGH, output $Q$ is LOW.

Condition IV. $\mathrm{S}=1$ and $\mathrm{R}=1$ : No matter what state Q and Q9 are in, application of 1 at the input of NOR gate always results in 0 at the output which results in both Q and Q9 being set to LOW (Q 5 Q9). LOW in both the outputs basically is wrong, so this case is invalid.
2. Direct/Delay Flip-Flop or D-FF: The S-R FF contains a forbidden/ambiguous state. To eliminate this condition we connect $S$ and $R$ together with an inverter, as shown in Figure 9-27, and ensure that $S$ and $R$ are never equal. D-FF is almost the same as the S-R FF with only one input, as shown in Table 9-19. This input is called $D$ or data input. The $D$ latch is called $D$ transparent latch. The output directly follows input with some delay so it is also known as delay $F F$.
3. J-K Flip-Flops: The forbidden/ambiguous state output in the S-R FF was eliminated in the D-FF by joining the inputs with an inverter. But the D-FF has a single input. The J-K latch is similar to S-R latch in that it has 2 inputs $J$ and $K$,


Figure 9-27 Circuit diagram of flip-flop


Figure 9-28 Circuit diagram of flip-flop

Table 9-20 State table of J-K flip-flop

| Input |  |  | Present Output <br> State | Next Output Input <br> State |
| :--- | :--- | :---: | :---: | :--- | Comments | $J$ | $K$ | $Q$ | $Q+$ |  |
| :--- | :--- | :---: | :--- | :--- |
| 0 | 0 | 0 | 0 | No change, i.e., Hold state/mode |
| 0 | 0 | 1 | 1 | No change, i.e., Hold state/mode |
| 0 | 1 | $X$ | 0 | Reset state |
| 1 | 0 | $X$ | 1 | Set state |
| 1 | 1 | 1 | 0 | Toggle mode/state |
| 1 | 1 | 0 | 1 | Toggle mode/state |

as shown in Figure 9-28. When both inputs are high, output toggles and the ambiguous state is eliminated, as shown in the Table 9-20.
4. Toggle Flip-Flop or T-FF: When the two inputs of J-K latch are shorted as shown in Figure 9-29, a T-FF is formed. When input is held HIGH, output toggles, as shown in the state Table 9-21.


Figure 9-29 Circuit diagram of flip-flop


Figure 9-30 State diagram of 2-bit up counter

Table 9-21 State table of T flip-flop

| Input | Present Output State | Next Output State | Comments |
| :---: | :---: | :---: | :--- |
| $T$ | $Q$ | $Q+$ |  |
| 1 | 0 | 1 | Toggle mode |
| 1 | 1 | 0 | Toggle mode |
| 0 | 1 | 1 | Hold mode |
| 0 | 0 | 0 | Hold mode |

The main difference between latch and flip-flop is that latch is level sensitive but flip-flop is edge sensitive. Thus, in a flip-flop the output change occurs either at the rising edge or falling edge of the clock pulse depending upon the circuit configurations.

Table 9-22 State table of 2-bit up counter

| $A$ | $B$ | Comments |
| :---: | :---: | :--- |
| 0 | 0 | Decimal equivalent 0 |
| 0 | 1 | Decimal equivalent 1 |
| 1 | 0 | Decimal equivalent 2 |
| 1 | 1 | Decimal equivalent 3 |

Table 9-23 State table of 2-bit down counter

| $A$ | $B$ | Comments |
| :---: | :---: | :---: |
| 1 | 1 | Decimal equivalent 3 |
| 1 | 0 | Decimal equivalent 2 |
| 0 | 1 | Decimal equivalent 1 |
| 0 | 0 | Decimal equivalent 0 |

State diagrams are used to describe the behaviour of a system. State diagrams can describe the possible states of events. Each diagram usually tracks the different states of its objects through the system. A 2-bit down counter counts the sequence $11 \rightarrow 10 \rightarrow 01 \rightarrow 00$, as shown in Table 9-23 and state diagram given in Figure 9-31.

The state diagram of a 3-bit down counter is shown in Figure 9-32. The state diagram of a 3-bit updown counter is shown in Figure 9-33. The present/ current state-next state table and state diagram of a 4-bit counter is shown in the Table 9-24 and Figure 9-34, respectively.

Figure 9-31 State diagram of 2-bit down
 counter counter

## Asynchronous counter

Asynchronous counter performs the counting operation where all the basic flip-flop blocks within the counter do not change the state at the same time. A 2-bit asynchronous counter is shown in Figure 9-35. The external clock is connected to the clock input of the first flip-flop only. The first flip-flop changes state at the falling edge of each clock pulse, but the second one changes only when triggered by the falling edge of the $Q$ output of the first one. Because of the inherent propagation delay through


Figure 9-32 State diagram of 3-bit down counter


Figure 9-33 Implementation of up down sequence by special control input U/D

Table 9-24 State table of 4-bit up counter

| Current or Present State |  |  |  | Next State |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $A(t)$ | $B(t)$ | $C(t)$ | $D(t)$ | $A(t+1)$ | $B(t+1)$ | $C(t+1)$ | $D(t+1)$ |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 |
| 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 |
| 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 |
| 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0 |

a flip-flop, the transition of the input clock pulse and a transition of the $Q$ output of the first flip-flop can never occur at exactly the same time. Therefore, the flip-flops cannot be triggered simultaneously, producing an asynchronous operation. Figure 9-36 shows a 3-bit asynchronous binary counter with its timing diagram using T-FF and J-K FF.


Figure 9-34 State diagram of 4-bit up counter


Figure 9-35 A 2-bit asynchronous counter


Figure 9-36 Block diagram of 3-bit asynchronous/ripple counter


Figure 9-37 Block diagram of 4-bit asynchronous/ripple counter


Figure 9-38 Block diagram of synchronous counter

A 3-bit ripple counter is implemented using T flip-flop. The clock pulse is applied to the first flip-flop and the successive flip-flop is triggered by the output of the previous flip-flop. All the T inputs are connected to $V_{c c}$. The flip-flops toggle on the negative edge of the clock input.

## Four-bit asynchronous/ripple counters

A 4-bit asynchronous binary counter with its timing diagram is shown in Figure 9-37.

## Synchronous counter

Synchronous counter performs the counting operation where all the basic flip-flop blocks within the counter clocks inputs are connected together, as shown in Figure 9-38, and change their states exactly at the same time.


Figure 9-39 Block diagram of SISO register

## Shift register

Shift register is a type of sequential circuit used for storing and shifting of digital data. Shift registers consist of a number of single-bit flip-flops connected together in a chain arrangement so that the output from one flip-flop becomes the input of the next one, thereby moving the stored data serially from either the left or the right direction. The numbers of individual data latches used to make up shift registers are determined by the number of bits to be stored. Shift registers are mainly used to store data and to convert data from either a serial to parallel or parallel to serial format with the entire flip-flop being driven by a common clock signal making them a synchronous circuit. They are generally provided with a clear or reset connection so that they can be "SET" or "RESET" as required. There are generally four types of shift registers.

## Serial input serial output (SISO) shift register

SISO registers accept serial data from one input, and after storage and movement, output the data in a serial mode via one output. SISO registers shift data to the right. The block diagram of 4-bit SISO shift resistor is shown in Figure 9-39.

This register accepts data serially and produces the stored information on its output line also in a serial form. It can be built using D-FF where the input of the rightmost flip-flop is used as a serial input line. The clock pulse is applied to all the flip-flops simultaneously. New data is entered into stage A while the data present in stage D are shifted out. Table 9-25 shows the state table of SISO entering data 1111 in the circuit and leaving out after nine cycles.

## Serial input parallel output (SIPO) shift register

SIPO registers accept serial data from one input, and after storage and movement, output the data in a parallel mode via several outputs. The block diagram of 4-bit SIPO Shift resistor is shown in Figure9-40.

Table 9-25 State table of SISO shift register

| $Q_{A}$ | $Q_{B}$ | $Q_{C}$ | $Q_{D}$ |
| :--- | :--- | :--- | :--- |
| 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 |
| 1 | 1 | 1 | 1 |
| 0 | 1 | 1 | 1 |
| 0 | 0 | 1 | 1 |
| 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 0 |



Figure 9-40 Block diagram of SIPO register


Figure 9-41 Block diagram of PISO register

This register consists of one serial input and outputs are taken from all the flip-flops parallel. The clock is applied simultaneously to all the flip-flops. Once the data is stored, each bit appears on its respective output line so that all the bits are available simultaneously.

## Parallel input serial output (PISO) shift register

PISO registers accept parallel data from several inputs, and after storage and movement, output the data in a serial mode via one output. This PISO configuration has the data input on lines $D_{1}, D_{2}, D_{3}$ and $D_{4}$ connected in parallel format. To write the data to the register, the Write/Shift control line must be held LOW. To shift the data, the Write/Shift control line is brought HIGH and the registers are clocked. The arrangement now acts as a SISO shift register, with $D_{1}$ as the data input. The block diagram of 4-bit PISO shift resistor is shown in Figure 9-41.

The four bits $A, B, C, D$ are entered simultaneously into their respective flip-flops. Shift/Load is a control input that allows the four bits of data to enter into the register in parallel or shift data in serial.

Table 9-26 State table of PIPO shift register

| $A$ | $B$ | $C$ | $D$ | Comments |
| :--- | :--- | :--- | :--- | :--- |
| 0 | 0 | 0 | 0 | Empty shift resistor |
| 1 | 0 | 1 | 1 | Storing of data 1011 in shiftresis- <br> tor after the first clock pulse |
| 0 | 0 | 0 | 0 | lifting of data 1011 after second <br> clock pulse the. |



Figure 9-42 Block diagram of PIPO register

## Parallel input parallel output (PIPO) shift register

PIPO registers accept parallel data from several inputs, and after storage and movement, output the data in a parallel mode via several outputs. PIPO is the fastest shift register; it needs only one clock pulse to store the data through its parallel inputs and in the second clock pulse the data out through its parallel out lines. The loading and shifting of a data set, 1011, is shown in the Table 9-26. The block diagram of 4-bit PIPO shift register is shown in Figure 9-42.

In this register, data can be shifted either in or out of the register in parallel. A 4-bit parallel-in-parallel-out register can be implemented using D-FFs. The parallel inputs are to be applied at $A, B, C$ and $D$ inputs, which are directly connected to delay inputs of respective flip flops.

## 9-9 BASIC CONCEPTS OF MEMORY

Semiconductor memories typically store a large number of bits. When an input is applied to a circuit, the output undergoes a change, but it remains in the same state even if the input is removed. This property of retaining the previous state is called memory. Memory circuits play an important role in digital systems because they provide a means for storing data temporarily or permanently. There are two types of memory-read-only memory (ROM) and random-access memory (RAM).

A semiconductor memory circuit can store data permanently as long as the power is on. This is called static memory. On the other hand, dynamic memory cannot store data permanently. The computer has certain internal storage areas, which store data and instructions either permanently or temporarily. The cache, RAM, virtual memory, hard drives and ROM are some of the devices and applications where data is stored.

Random-access memory (RAM): This is the best known form of memory that the computer uses. Every application which the user opens is placed in the RAM. For any computer, the central processing unit or CPU requests data from the RAM, processes it, and then writes new data back on to the RAM. This cycle can take place a millions times within the span of a second. RAM is used for temporary file storage unless the data is saved permanently. There are two different types of RAM—DRAM (dynamic random-access memory) and SRAM (static random-access memory). The technology that is used to hold data in DRAM and SRAM differs. While DRAM is the more commonly used memory, SRAM is the faster of the two. DRAM needs to be refreshed very often, whereas this is not the case with SRAM.


Figure 9-43 The block diagram of memory

Hard drive: A hard drive is a form of computer memory that allows you to permanently store data. The size of a hard drive is typically measured in gigabytes.

Virtual memory: Virtual memory is used when applications are too large for the RAM to handle. The operating system uses the hard drive as its virtual memory to temporarily store information and takes it back when needed. This process is normally a lot slower than temporarily storing data on the RAM.

Cache memory: Cache memory is used as a bridge between the CPU and the RAM. It holds the most frequently used data for instructions to be processed.

Read-only memory (ROM): It is used for permanent storage of data.
Every memory system requires different types of input and output lines to perform the functions described below:
a. Select read/write lines are used for read or write operations.
b. Address lines are used to access the address in the memory for read or write operations.
c. Data input lines are used to supply input data to be stored in the memory at the time of a write operation.
d. Data output lines are used to read data from the stored memory at the time of the read operation.
e. Memory enable lines are used to enable or disable the operation of the memory circuit.

The block diagram of memory is shown in Figure 9-43. The write operation of input data to a memory circuit or a device depends on the read/write line of the memory. It can be enabled or disabled based on the memory select line. Data output is used for reading data from the memory.

## 9-10 REAL-LIFE APPLICATIONS

Nowadays digital circuits are used in almost all daily applications. These include computers, mobile phones, washing machines, and DVD players among other things. Digital devices and instruments give better performance over the analog ones. For example, a digitally equipped DTH provides studio-quality picture at home. New digital compression technologies generate very high quality photographs and movies.

## POINTS TO REMEMBER

1. Binary numbers consist of 1 and 0 .
2. NAND and NOR gates are used as universal logic gates.
3. Multiplexer is called path selector.
4. Decoder with an enable input acts as a de-multiplexer.
5. Encoder converts non-digital data to digital data.
6. Latch is level sensitive whereas flip-flop is edge sensitive.
7. Counter is a kind of sequential circuit used for counting the number of clock pulses.
8. A 2-bit up counter counts the sequence $00 \rightarrow$ $01 \rightarrow 10 \rightarrow 11$.
9. Shift register is a kind of sequential circuit used for storing and shifting of digital data.

## IMPORTANT FORMULAE

1. $X+0=X$
2. $X+1=1$
3. $X+X=X$
4. $X \cdot \bar{X}=1$
5. $X+\bar{X}=1$
6. $\overline{A+B}=\bar{A} \cdot \bar{B}$
7. $\overline{A \cdot B}=\bar{A}+\bar{B}$

## OBJECTIVE QUESTIONS

1. $\overline{\bar{A}}=$
(a) A
(b) 0
(c) 1
(d) None of the above
2. $A+\bar{A}=$
(a) 1
(b) 0
(c) $A$
(d) $\bar{A}$
3. $\bar{A}+\overline{B=}$
(a) $\overline{A \cdot B}$
(b) $\bar{A}$
(c) $\bar{B}$
(d) $A \cdot B$
4. Universel logic gates are:
(a) NAND and NOR
(b) OR and AND
(c) NOT and OR
(d) OR and XOR
5. NAND gate is a combination of :
(a) AND and NOT gates
(b) AND and OR gates
(c) AND and XOR gates
(d) OR and NOR gates
6. Exclusive OR logic equation is:
(a) $\bar{A} B+\overline{B A}$
(b) $\bar{A} B+\overline{B+A}$
(c) $\bar{A} B+\bar{B}$
(d) $\bar{A} B+A \bar{B}$
7. Binary equivalent of decimal 13 is:
(a) 1110
(b) 1111
(c) 0111
(d) 1101
8. Decimal value of 1010 is:
(a) 9
(b) 7
(c) 19
(d) 10
9. How many minimum NAND gates are used in a half adder?
(a) 5
(b) 7
(c) 9
(d) 2
10. The minimum number of NAND gates used in a full adder is:
(a) 5
(b) 7
(c) 9
(d) 2
11. Decoder with an enable input can be used as a :
(a) De-multiplexer
(b) Encoder
(c) XOR
(d) Multiplexer
12. Latch is:
(a) Logic level sensitive
(b) Edge sensitive
(c) Both (a) and (b)
(d) None of the above
13. Flip-flop is:
(a) Logic level sensitive
(b) Edge sensitive
(c) Both (a) and (b)
(d) None of the above
14. Counters are used to count the:
(a) Number of clock pulses
(b) Number of glitches
(c) Number of flip-flop
(d) None of the above
15. Purpose of using a shift register is:
(a) Shifting and storing
(b) Only storing
(c) Only shifting
(d) None of the above
16. Fastest operating shift register is:
(a) PIPO
(b) SIPO
(c) PISO
(d) SISO
17. Slowest operating shift register is:
(a) PIPO
(b) SIPO
(c) PISO
(d) SISO

## REVIEW QUESTIONS

1. What is a logic circuit?
2. What are the differences between positive and negative logic?
3. Draw and explain the operation of AND, OR, NOT, NOR, XOR, XNOR, NAND using the truth table.
4. How does the XOR gate differ from the OR gate?
5. What is the universal gate? Give reasons.
6. State and explain De Morgan's theorem.
7. What is adder?
8. What are the differences between a half adder and a full adder?
9. Draw the block diagrams of half adder and full adder and explain their respective operations?
10. Design a full adder using a half adder.
11. What are the differences between an encoder and a decoder?
12. What is a multiplexer? Explain the operation of multiplexer using the truth table.
13. Explain the significance of the select input in a multiplexer.
14. What is a de-multiplexer? Explain its operation using a block diagram.
15. Why is a decoder with an enable input called a de-multiplexer?
16. What is latch?
17. What is flip-flop?
18. What are the basic differences between a latch and a flip-flop?
19. What is a counter?
20. Explain the working principle of counter.
21. What are the basic differences between asynchronous and synchronous counter?
22. What are the two important properties of shift register?
23. Explain the working principle of SISO?
24. Explain the working principle of SIPO?
25. Explain the working principle of PISO?
26. Explain the working principle of PIPO?

## PRACTICE PROBLEMS

1. Convert the following numbers into the other number system:
(a) $(1111)_{2}=(?)_{8}$
(b) $(238)_{8}=(?)_{10}$
(c) $(111101)_{2}=(?)_{16}$
(d) $\quad(67)_{10}=(?)_{8}$
(e) $(1 \mathrm{DFF}) 16=(?)_{10}$
(f) (FF) $16=(?)_{2}$
(g) $(111.11)_{2}=(?)_{10}=(?)_{16}$
(h) $(455.67)_{10}=(?)_{2}$
(i) $(445.67)_{10}=(?)_{2}$
(j) $(111.11)_{10}=(?)_{2}$
(k) $(1110.11)_{2}=(?)_{10}$
(l) $(45.675)_{10}=(?)_{\text {Hex }}$
(m) $\quad(451.167)_{8}=(?)_{2}$
(n) $(45.67)_{\mathrm{Hex}}=(?)_{2}$
(o) $(745.167)_{8}=(?)_{2}$
2. Simplify the given equations and implement the results with logic gates.
(a) $\bar{A}+\bar{A} B+A B \bar{C}$
(b) $\bar{A}+\bar{A} \bar{B}+A B \bar{C}$
(c) $A B \bar{C}+\bar{A} \bar{B}+A B \bar{C}$
(d) $A B \bar{C}+A \bar{B} \bar{C}$
(e) $A+\bar{A} B+A B \bar{C}+\overline{A B}$
(f) $\bar{A} B C+\bar{A} \bar{B}+A B \bar{C}$
(g) $\bar{A} B C+\bar{A} \bar{B}+A \bar{B} \bar{C}+\overline{A B} C$

3 . Find the output logic expression from the given logic gates and then form a truth table.

(a)

(b)
4. Draw the circuit diagram using any logic gate for the given equations:
(a) $Q=A \bar{B}+\bar{A} B$
(b) $Q=A A+A B+A C+B C$
5. Find the logic expression from the given truth table and implement the result with logic gates.

| Input |  |  | Output |
| :---: | :---: | :---: | :---: |
| $A$ | $B$ | $C$ | $\times$ |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 |

## SUGGESTED READINGS

1. Chattopadhyay, D. and P. C. Rakshit. 2006. Electronics Fundamentals and Applications. New Delhi: New Age International Publishers.
2. Ghosh, K. K. 2008. Basic Electronics. Kolkata: Platinum Publishers.
3. Chaudhury, Diptiman Ray. 2001. Digital Circuits, Digital Electronics. Kolkata: Eureka Publisher.
4. Floyd,ThomasL.2007.Digital Fundamentals. New Delhi: Pearson Education.

## SOLVED QUESTION PAPERS

This page is intentionally left blank.

## Biju Patnaik University of Technology Basic Electronics (Common for all Branches of Engineering) Subject Code: BE-2101

1 (a) Explain with suitable examples the difference between analog, digital and discrete time signals.
(b) Compare the advantages and disadvantages of centre-tapped and bridge-type full-wave rectifiers.
(c) Define the following terms:
(i) The slew rate of an op-amp
(ii) Unity gain bandwidth
(d) Derive the expression for the collector current of a CE transistor.
(e) Distinguish between AC and DC load lines.
(f) Explain with suitable diagrams the difference between a self bias and a fixed bias.
(g) Determine the number of cycles of a 1 kHz sinusoidal signal as viewed on an oscilloscope when the sweep frequencies are (i) 2 kHz and (b) 500 Hz .
(h) The binary number system is used in digital electronic circuits. Why are the octal, decimal or hexadecimal number systems not used in circuit levels?
(i) Convert the decimal number -39 to its equivalent 1's complement and 2's complement forms.
(j) Compare static RAM and dynamic RAM with respect to their speed, volume of data storage, size and cost.

2 (a) What is a clamper circuit? Draw the circuit diagram of a positive clamper and a negative clamper showing their output waveforms.
(b) Analyse and draw the output waveform of the following circuit when $V_{i}=5 \sin 100 \pi t$.


3 (a) Define mobility of a charge carrier. Which of the following materials- $\mathrm{Si}, \mathrm{Ge}$ or $\mathrm{GaAs}-$ will have the best thermal stability and why?
(b) Distinguish between zener breakdown and avalanche breakdown.
(c) Derive an expression for the voltage gain of the given op-amp circuit.


4 (a) For this circuit, determine $I_{B}, I_{C}, V_{E}, V_{C E}$ and $V_{B}$, where the symbols used have their usual meaning.

(b) Draw a simplified hybrid model of a CE transistor amplifier and then find its input impedance, output impedance and voltage gain.

5 (a) Explain the basic principle of a sinusoidal oscillator. How does an oscillator start its operation? What is its voltage gain while starting and during the normal operation?
(b) State and explain the function of the sweep signal in an oscilloscope. What is the Lissajous method? Does the Lissajous method require a sweep signal? Justify your answers in brief along with suitable diagrams or graphs.

6 (a) Which of the logical gates are considered universal gates? Draw circuit diagrams showing the universal properties of any one universal gate.
(b) Implement the following logic functions:
(i) $X=\bar{A}+B C$ using NAND gates
(ii) $Y=\bar{A} B+C$ using NOR gates

7 (a) Write the truth table of the half adder and full adder. Draw logic diagrams.
(b) Convert the following Boolean expression into its equivalent SOP form: $A \bar{B} C+\bar{A} \bar{B}+A B \bar{C}$.
(c) Distinguish between a multiplexer and a demultiplexer. Draw logic diagrams of a 4-to-1 line multiplexer.

8 (a) Explain the temperature effect on the $V-I$ characteristics of a diode.
(b) Derive the expression of output voltages for both inverting and non-inverting amplifiers.
(c) Describe with examples the standard forms of Boolean expression.
(d) Describe the ideal and real characteristics of an op-amp.

## Solutions

1 (a) An analog signal is that signal which varies continuously with time (for example, a sine wave), while a digital signal is one which represents a sequence of numbers, that is, it has two values-high (1) and low (0). A discrete signal, on the other hand, is a signal that is defined only at certain specific values of time. The time instant need not be equidistant. In practice, it is usually taken at equally spaced intervals for computational and mathematical convenience.

$\begin{array}{llll}\text { Figure } 1 & \text { (a) Analog signal } & \text { (b) Digital signal } & \text { (c) Discrete signal }\end{array}$
(b) Refer to Section 3-5-2 on Page 3-14.
(c) (i) Refer to Section 1-5-7 on Page 1-16.
(ii) Usually, the differential gain of an op-amp is very high. As the frequency increases, the open-loop gain drops until it reaches unity. The frequency at this gain value is specified by the manufacturer as the unity gain bandwidth is equal to B .
(d) The expression for the collector current may be derived as shown below:

$$
\begin{gathered}
I_{C \text { total }}=I_{C \text { majority }}+I_{C \text { minority }} \\
I_{C}=\alpha I_{E}+I_{C B O} \\
=\alpha\left(I_{c}+I_{b}\right)+I_{C B O} \\
=\alpha I_{C}+\alpha I_{b}+I_{C B O} \\
I_{C}-\alpha I_{C}=\alpha I_{B}+I_{C B O} \\
\Rightarrow I_{C}(1-\alpha)=\alpha I_{B}+I_{C B O} \\
\Rightarrow I_{C}=\frac{\alpha}{1-\alpha} I_{B}+\frac{1}{1-\alpha} I_{C B O} \\
\Rightarrow I_{C}=\beta I_{B}+(1+\beta) I_{C B O} \quad\left[\text { since } \frac{\alpha}{1-\alpha}=\beta \frac{1}{1-\alpha}=1+\beta\right] .
\end{gathered}
$$

(e) The table below gives the difference between the DC and AC load lines.

| The DC Load Line | The AC Load Line |
| :---: | :---: |
| The load line, $V_{C E}$ versus $I_{C}$, under the DC condition is called the DC load line. It has a CE configuration with an R-load. | This is the load line that is drawn in the output characteristics of transistor circuits. It gives the values of $I_{C}$ and $V_{C E}$ when the AC signal is applied. |

(f) The difference between fixed bias and self bias is given below:

| The Fixed Bias | The Self Bias |
| :--- | :--- |
| In a fixed-biased circuit, $R_{a}$ is not present. <br> This is a less stable circuit compared <br> to the self-biased one. For a fixed bias, <br> $\alpha=\beta+1$. | The $R_{E}$ is present, which helps to stabilize the <br> circuit. Here, $s=1$. |


(g) Viewed signals have frequencies equal to 1 kHz . Therefore,
(i) when sweep frequency is 2 kHz , half a cycle will be seen.
(ii) when sweep frequency is equal to 500 Hz or $1 / 2 \mathrm{kHz}$, two cycles will be seen.
(h) Binary number systems use two digits, 0 and 1 . This is a very convenient way of representation. The octal, hexadecimal or decimal systems, on the other hand, use numbers from 0 to 7 (octal), 0 to 9 (decimal) and $A$ to $F$ (hexadecimal). Since all signals can be converted to the digital form, that is, the binary 0 and 1 structure, logic circuits can easily operate in circuit levels.
(i) We know that $39=100111$.

The 1's complement $(100111)^{1}=011000$.
The 2 's complement $=1$ 's complement $+1=011000+1=011001$.
(j) The comparison between static and dynamic RAM is given below:

| Static RAM | Dynamic RAM |  |
| :--- | :--- | :--- | :--- |
| (i) $\quad$It consists of internal latches, which <br> store binary information. | (i) | It stores the binary information in the <br> form of electrical charges on capacitors. |
| (ii) $\quad$ Its speed is fast. |  |  |$\quad$ (ii) | Its speed is slow. |
| :--- |
| (iii) |
| The storage capacity is low. |
| (iv) It is large in size and expensive. |

2 (a) Refer to Section 3-6-2 on Page 3-35.
(b) Given that

$$
\begin{aligned}
& V_{i}=5 \sin (100 \pi t) \\
& V_{m}=5 .
\end{aligned}
$$



Figure 2(a) A sine waveform
In the positive half, the diode is reverse-biased, while in the negative half, the diode is forward-biased. The latter condition will result in a short circuit.


Figure 2(b) The circuit diagram
Applying KVL, we get

$$
\begin{gathered}
-5 V+V_{C}+0.7 V+3 V=0 \\
V_{C}=5 V-3.7 V=1.3 V
\end{gathered}
$$

The output voltage is given by

$$
\begin{gathered}
+V_{0}+0.7 V+3 V=0 \\
V_{0}=-3.7 V .
\end{gathered}
$$

As mentioned earlier, in the positive half, the diode act as an open circuit.


Figure 2(c) The diode as an open circuit

Applying KVL. We have

$$
\begin{gathered}
+5 \mathrm{~V}+1.3 \mathrm{~V}-V_{0}=0 \\
V_{0}=6.3 \mathrm{~V} .
\end{gathered}
$$

The output waveform is drawn as shown in Figure 2(d).


Figure 2(d) An output waveform
3 (a) If the electric field, $E$, is applied in $V / \mathrm{em}$, the positive charge carriers will drift in the direction of $E$ and acquire a velocity $V_{\text {drift }}$ in $\mathrm{em} / \mathrm{sec}$. This relation is given by $V_{\text {drift }}=\mu p C$, where $\mu p$ is equal to the mobility of holes which is expressed in $\mathrm{cm}^{2} / V \cdot \mathrm{sec}$. Among $\mathrm{Si}, \mathrm{Ge}$ and GaAs , the last element has the best thermal stability because of a high-energy band gap of about $1.41 \mathrm{e} V$.
(b) Refer to Table 2-1 on Page 2-42.
(c) In the given figure, the output voltage

$$
\begin{equation*}
V_{0}=\left[1+\frac{R_{2}}{R_{1}}\right] V_{A}, \text { where } V_{A} \text { is the node voltage. } \tag{1}
\end{equation*}
$$



Figure 3 An op-amp
Applying the voltage divider rule at node $A$, we have

$$
\begin{equation*}
V_{A}=\frac{R_{4} V_{1}}{R_{4}+R_{3}} \tag{2}
\end{equation*}
$$

Putting the value of $V_{A}$ from Equation (2) in Equation (1), we get

$$
\begin{gathered}
V_{0}=\left[1+\frac{R_{2}}{R_{1}}\right]\left[\frac{R_{4}}{R_{4}+R_{3}}\right] V_{\mathrm{i}} \\
\frac{V_{0}}{V_{i}}=A_{v}=\left[1+\frac{R_{2}}{R_{1}}\right]\left[\frac{R_{4}}{R_{4}+R_{3}}\right] .
\end{gathered}
$$

4 (a) The given figure can be represented as shown below.


Figure 4 A self-biased circuit

Here, $V_{B}=\frac{V_{C C} \times R_{2}}{R_{1}+R_{2}}=\frac{18 \times 510}{510+510}=9 \mathrm{~N}$.
By KVL, we have

$$
\begin{aligned}
& V_{R_{2}}-V_{B E}-I_{E} R_{E}+18=0\left(\text { since } V_{R_{2}}=V_{B}\right) \\
\Rightarrow & 9-0.7-I_{E} \times 7.5 \times 10^{3}+18=0 \\
\Rightarrow & I_{E}=\frac{26.3}{7.5 \times 10^{3}}=3.5 \mathrm{~mA} \\
& I_{E} \cong I_{C}=3.5 \mathrm{~mA} \\
& I_{B}=I_{c} / \beta=3.5 \times 10^{-3} / 130=26 \mu \mathrm{~A} .
\end{aligned}
$$

Again,

$$
\begin{aligned}
& V_{c c}-I_{C} R_{C}-V_{C E}-I_{E} R_{E}+18=0 \\
\Rightarrow & 18-V_{C E}-I_{C}\left(R_{C}+R_{E}\right)+18=0 \\
\Rightarrow & V_{C E}=36+I_{C}\left(R_{C}+R_{E}\right) \\
\Rightarrow & V_{C E}=36+35 \times 10^{-3}(9.1+7.5) \times 10^{3} \\
\Rightarrow & V_{C E}=36+58.1=94.1 \mathrm{~V} .
\end{aligned}
$$

(b) A simplified hybrid model of a CE transistor amplifier is shown below.


Figure 5 A hybrid model of a CE transistor amplifier
Now,

$$
\begin{aligned}
& Z_{i}=\text { input impedance }=R_{B} \| h_{i e} \\
& Z_{0}=\text { Output impedance }=R_{C} \| \frac{1}{\text { hoe }} .
\end{aligned}
$$

The voltage gain,

$$
\begin{gathered}
V_{0}=-I_{0} Z_{0}=-I_{c} Z_{0}=-\left(h_{f e} I_{B}\right)\left(R_{C} \| \frac{1}{\mathrm{hoe}}\right) \\
V_{i}=h_{i e} \times I_{B} \\
A_{V}=V_{o} / V_{i}=-\frac{\operatorname{hfe}\left(R_{C} \| \frac{1}{\mathrm{hoe}}\right)}{h_{i e}} .
\end{gathered}
$$

The current gain,

$$
A_{i} \cong h_{f e} .
$$

5 (a) A sinusoidal oscillator is shown below.


Figure 6 Block diagram of a sinusoidal oscillator

The basic principles of the sinusoidal oscillator are derived from the Barkhausen criteria. These are (i) positive feedback, (ii) loop gain is equal to unity or $A \beta=1$, and (iii) $\angle A B=180^{\circ}$ and $\angle A B=180^{\circ}$ (since the phase shift by the feedback network is equal to $180^{\circ}$ ). This means that the phase shift between the input signal and the feedback signal is equal to $360^{\circ}$ or $0^{\circ}$. To start oscillation, it is necessary to design the circuit such that $A \beta$ is slightly greater than unity and the amplitude of the oscillations is limited. The gain at the starting point is:

$$
A_{d}=\frac{A}{1-A B} \rightarrow \text { higher or } \infty
$$

(b) When the vertical input is equal to zero, the signal remains at the vertical centre of the screen. The same is also true for a horizontal input of zero Volts, as a stationary dot of DC voltage applied to an input will shift the dot. The CRO usually displays the vertical input waveform as a function of time. This requires a horizontal deflection voltage that moves or sweeps the circuit spot across the screen from the left to right with constant velocity, and rapidly returns to stability for the next sweep. The Lissajous figure is given below.


Figure 7 The Lissajous figure
When sine waves are applied simultaneously to the horizontal and vertical deflection plates of the CRO, an $\alpha / 0$ sweep is required for a Lissajious pattern.

6 (a) The NAND and NOR gates are considered universal gates.

(a) NAND gate

(b) NOR gate

Figure 8 The universal gates
Considering the NAND gates,


Figure 9 NAND gate as aniversal gate
(b) The implementation of the given logic functions is shown below.
(i) Given that: $X=\bar{A}+B C$

Now,

$$
\overline{\bar{X}}=\overline{\bar{A}+B C}=\overline{\bar{A} \overline{B C}}=\overline{A \overline{B C}} .
$$



Figure 10 NOR gate as a universal gate
(ii) Given that: $Y=\bar{A} B+C$

So,

$$
\begin{gathered}
\overline{\bar{Y}}=\overline{\overline{\bar{A} B+C}}=\overline{(\overline{\bar{A}} \bar{B}) \bar{C}}=\overline{(A+\bar{B}) \bar{C}} \\
\overline{A+\bar{B}}+\overline{\bar{C}}=\overline{A+\bar{B}}+C .
\end{gathered}
$$



Figure 11 Realization of the logic expression using a logic gate

7 (a) The half adder:


Figure 12(a) A half-adder block diagram

| $A$ | $B$ | $S$ | $C$ |
| :---: | :---: | :---: | :---: |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |

Here,

$$
\begin{aligned}
& S=A \oplus B \\
& C=A B .
\end{aligned}
$$

The logic diagram of a half adder:


Figure 12(b) A half-adder logic circuit
The full adder:


Figure 12(c) A full-adder block diagram

| $X$ | $Y$ | $Z$ | $S$ | $C$ |
| :---: | :---: | :---: | :---: | :---: |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | L |
| 1 | 1 | 0 | 0 | L |
| 1 | 1 | 1 | L | L |

$$
S=\Sigma \mathrm{m}(1,2,4,7)=X \oplus Y \oplus Z
$$

$$
C=\Sigma \mathrm{m}(3,5,6,7)=[X \oplus Y] Z+X Y .
$$



$$
e=[X \oplus Y] Z
$$

$$
+X Y
$$

Figure 12(d) A full-adder logic circuit
(b) Given that: $A \bar{B} C+\bar{A} \cdot \bar{B}(C+\bar{C})+A B \bar{C}$

$$
\begin{aligned}
& \Rightarrow A \bar{B} C+\overline{A B} C+\bar{A} \bar{B} \bar{C}+A B \bar{C} \\
& \Rightarrow 101+001+000+110 \\
& \Rightarrow \Sigma \mathrm{~m}(0,1,5,6)
\end{aligned}
$$

(c) The differences between a multiplexer and de-multiplexer are given below.

| Multiplexer | De-multiplexer |
| :--- | :--- |
| (i) It has several inputs but only one output. | (i) It has one input and many outputs. |
| (ii) Its size is equal to $2^{n}: 1$. | (ii) Its size is equal to $1: 2^{n}$. |
| (iii) It is a data selector. | (iii) It is a data distributor. |

The $4: 1$ multiplexer is depicted below.


Figure 13(a) A block diagram of a $4: 1$ multiplexer
A 4:1 multiplexer has a size of $2^{2}: 1$, where 2 is the number of sections $\left(S_{1}\right.$ and $S_{0}$ ). It has one output, $y$, and four inputs $(A, B, C$ and $D)$.

| $S_{1}$ | $S_{0}$ | $I$ |
| :---: | :---: | :---: |
| 0 | 0 | $I_{0}$ |
| 0 | 1 | $I_{1}$ |
| 1 | 0 | $I_{2}$ |
| 1 | 1 | $I_{3}$ |

Here,

$$
\begin{gathered}
Y=S_{1} S_{0} I_{0}+S_{1} S_{0} I_{1} \\
S_{1} S_{0} I_{2}+S_{1} S_{0} I_{3} .
\end{gathered}
$$



Figure 13(b) A 4:1 multiplexer using a logic

8 (a) Temperature has a remarkable effect on the $V-I$ characteristics of a diode. The reverse saturation current will just about double in magnitude for every $10^{\circ} \mathrm{C}$ increase in temperature. This figure shows the transformation for different temperatures. As the temperature increases, the threshold voltage decreases and the forward current rises rapidly.


Figure 14 V-I characteristics of a diode
(b) In an inverting amplifier,

$$
\begin{aligned}
& I_{1}=I_{0}+I_{f} \\
& \text { ( } I_{0}=0 \text { ) } \\
& \Rightarrow I_{1} \cong I_{f} \\
& \Rightarrow \frac{V_{i}-V_{A}}{R_{1}}=\frac{V_{A}-V_{0}}{R_{f}} \quad\left(V_{A}=0 \text { due to the virtual ground concept }\right) \\
& \Rightarrow \frac{V_{i}}{R_{1}}=\frac{-V_{0}}{R_{f}} \\
& \Rightarrow \frac{V_{0}}{V_{i}}=\frac{-R_{f}}{R_{1}}
\end{aligned}
$$

Figure 15 An op-amp as an inverting amplifier

In a non-inverting amplifier,

$$
\begin{aligned}
& I_{1}=I_{i}+I_{f} \Rightarrow I_{1}=I_{f}\left(I_{i}=0\right) \\
\Rightarrow & \frac{0-V_{i}}{R_{1}}=\frac{V_{1}-V_{0}}{R_{f}}\left[V_{A}=V_{i}\right] \\
\Rightarrow & V_{0}=R_{f}\left[\frac{R_{f}+R_{1}}{R_{f} R_{1}}\right] \rightarrow V_{0}=\left[1+\frac{R_{f}}{R_{i}}\right] V_{i} .
\end{aligned}
$$



Figure 16 An op-amp as a non-inverting amplifier
(c) The following expressions illustrate the standard terms of a Boolean expression.

$$
\begin{gathered}
A B C+A \bar{B} C+A B \bar{C} \\
\Rightarrow A C(B+\bar{B})+A B \bar{C} \\
\Rightarrow A C+A B \bar{C} \\
\Rightarrow A[C+B \bar{C}]=A[C+B][C+\bar{C}]=A[C+B]=A C+A B .
\end{gathered}
$$

(d) The characteristics of an ideal and a real op-amp are described below.

| A Real Op-amp | An Ideal Op-amp |
| :---: | :---: |
| (i) The voltage gain, $\mathrm{A}_{\mathrm{v}}$, is high. | (i) $\mathrm{A}_{V}$ is infinite. |
| (ii) $\mathrm{R}_{\mathrm{i}}$ is high. | (ii) $\mathrm{R}_{\mathrm{i}}$ is infinite. |
| (iii) $\mathrm{R}_{\mathrm{o}}$ is low. | (iii) $\mathrm{R}_{\mathrm{o}}$ is equal to 0 . |
| (iv) BW is high. | (iv) BW is infinite. |
| (v) CMRR is high. | (v) CMRR is infinite. |
| (vi) SR is high. | (vi) SR is infinite. |

## Biju Patnaik University of Technology Basic Electronics (Common for all Branches of Engineering) Subject Code: BE-2101

1 (a) Explain the difference between analog, digital and discrete time signals.
(b) A signal is represent by $y=5 \sin \left(628 t+30^{\circ}\right)=A \sin (\omega t+\phi)$. Find the frequency, amplitude and initial phase of the signal.
(c) What is the meaning of CMRR of an op-amp? How does it affect the performance of the op-amp?
(d) Why is voltage-series feedback most commonly used in amplifiers?
(e) Derive the expression for collector currents of CE transistors?
(f) Write down the advantages of a negative feedback amplifer?
(g) Define the terms $h_{f e}, h_{i e}, h_{o e}$, and $h_{r e}$ of a transistor?
(h) What is the relationship between the period of a waveform and its frequency?
(i) What do you mean by digital waveforms? Explain rise time, fall time and pulse width by drawing the pulse circuit.
(j) What do you mean by the three-state gate? What is its importance in a combinational circuit?

2 A crystal diode having an internal resistance $R_{f}=10 \Omega$ is used for centre-tapped full-wave rectification. If the applied voltage $V=50 \sin \pi t$ and the load resistance is $R_{L}=1 \mathrm{k} \Omega$,
(a) draw the input and output voltage and current waveforms,
(b) determine the efficiency of the circuit,
(c) determine the Ripple factor.

3 (a) Write down the ideal characteristic of an op-amp.
(b) Draw the circuits for both inverting and non-inverting amplifiers using the op-amp. Derive an expression for the gain of an inverting amplifier.

4 (a) A negative feedback amplifier has open-loop gain of $10^{5}$ and a closed-loop gain of 100.
(i) Determine the feedback factor.
(ii) If a manufacturing error results in a reduction of the open-loop gain to 103, what does the closed-loop gain result in?
(iii) How does the percentage change in the closed-loop gain correspond to the change in the open-loop gain?
(b) Explain the bandwidth extension and reduction in non-linear distortion properties of a negative feedback amplifier.

5 (a) Explain the difference between the voltage divider bias and the self-bias circuits.
(b) For the given circuit, determine $I_{B}, I_{C Q}, V_{E}, V_{c t Q}$ and $V_{B}$, where the symbols denote their usual meanings.


6 (a) State and explain the function of the sweep generator in an oscillator.
(b) Explain how phase measurement can be done using an oscilloscope through the Lissajous method.

7 (a) State the associative and communicative laws of Boolean algebra.
(b) State De Morgan's Theorem and apply it to the following expression: $Y=A \bar{B}+\bar{C} D+E F$.
(c) Using the Boolean algebra technique, simplify the following expressions:
(i) $A B+A(B+C)+B(B+C)$
(ii) $(A \bar{B}(C+B D)+\bar{A} \bar{B}) C$

8 (a) Apply De Morgan's Theorem to minimize:
(i) $\overline{W X Y Z} \overline{W+X+Y+Z}$
(ii) $\bar{W} \bar{X} \bar{Y} \bar{Z}$
(iii) $\overline{A+B+\bar{C}}+D(\overline{E+\bar{F}})$
(b) The binary values for which the following POS expression is equal to 0 :
$(X+\bar{Y}+Z)(\bar{X}+Y+Z)(X+Y+\bar{Z})(\bar{X}+\bar{Y}+\bar{Z})(X+\bar{Y}+\bar{Z})$.

## Solutions

1 (a) Refer to the solution to Question 1(a) of the 2009 paper.
(b) For the given values, amplitude,

$$
A=5 \mathrm{~V}
$$

We know that $\omega=628$. So,

$$
\begin{aligned}
& 2 \pi f=628 \\
& f=100 \mathrm{~Hz}
\end{aligned}
$$

The initial plane, $\phi=30^{\circ}$.
(c) Refer to Section 1-5-9 on Page 1-13.
(d) The voltage-series feedback is commonly used in amplifiers because it provides high voltage gain. Moreover, it gives a high-input impedance as well as a low-output impedance.
(e) Refer to the solution to Question 1(d) of the 2009 paper.
(f) Refer to Section 6-3 on Page 6-4.
(g) Input impedance is represent by $h_{i e}$, which is equal to $V_{B E} / I_{B}$ for the common emitter configuration. Reverse voltage gain is represented by $h_{r e}$, and it is equal to $V_{B E} / V_{C E}$. The forward current gain is $h_{f e}$, which is equal to $I_{C} / I_{B}$, whereas $h_{o e}$ is the output admittance and is equal to $I_{C} / V_{C E}$.


Figure 17 The $h$ parameter model of a transistor
(h) Refer to Section 8-5-1 on Page 8-6.
(i) In a digital waveform, the amplitude has two states, high and low.


Figure 18 Digital waveforms
(j) When $C$ is equal to 0 , the output behaves as the high-input impedance. When $C=1$, the output is equal to the input. $C$ is the controlling input.


Figure 19 A tri-state buffer

2 (a) Given that:

$$
\begin{aligned}
& \mathrm{V}_{\mathrm{m}}=50 \sin (\pi \mathrm{t})=\mathrm{V}_{\mathrm{m}} \sin (\omega \mathrm{t}) \\
& \Rightarrow \mathrm{V}_{\mathrm{m}}=50 \mathrm{~V} \\
& I_{m}=\frac{V_{m}}{R_{f}+R_{L}}=\frac{50}{10+10^{3}}=49.5 \mathrm{~mA} \\
& \mathrm{I}_{\mathrm{m}}=\text { peak current } .
\end{aligned}
$$


(a) A sinusoidal waveform

(b) A rectified output waveform

Figure 20 Rectified waveforms
(b) Efficiency is equal to

$$
n=\frac{0.812}{1+\frac{r c f}{R_{L}}} \times 100=\frac{0.812}{\left[1+\frac{10}{10^{3}}\right]} \times 100=80.4 \text { per cent }
$$

(c) Ripple factor is equal to $\sqrt{\left[\frac{1 \mathrm{rms}}{1 \mathrm{dc}}\right]^{2}-1}$

$$
\begin{aligned}
1 \mathrm{rms} & =\frac{1 \mathrm{~m}}{\sqrt{2}}=\frac{49.5}{\sqrt{2}} \mathrm{ma}=35 \mathrm{~mA} \\
1_{\mathrm{dc}}=\frac{2 \mathrm{I}_{\mathrm{m}}}{\pi} & =\frac{2 \times 49.5}{\pi} \mathrm{~mA}=31.5 \mathrm{~mA} .
\end{aligned}
$$

Therefore, the Ripple factor $=\sqrt{\left(\frac{35}{31.5}\right)^{2}-1}=0.485$.

3 (a) Refer to Section 1-3 on Page 1-5.
(b) The circuits for inverting and non-inverting op-amps are given below.

(a) An inverting op-amp

(b) A non-inverting op-amp

Figure 21 Operational amplifiers

For an inverting op-amp, by applying the virtual ground concept, we have

$$
V_{A}=V_{B}=0 .
$$

Now, by applying KCL at Node $A$, we get

$$
\begin{aligned}
& I_{1}=I_{2}+I_{3} \\
& \Rightarrow \frac{V_{i n}-V_{A}}{R_{l}}=0+\frac{V_{A}-V_{0}}{R_{f}}\left(\mathrm{I}_{2}=0 \text { as } \mathrm{R}_{\mathrm{in}}=\infty\right) \\
& \Rightarrow \frac{V_{i n}}{R_{l}}=\frac{-V_{0}}{R_{f}} \Rightarrow A_{v}=\frac{V_{0}}{V_{i n}}=\frac{-R_{f}}{R_{l}} .
\end{aligned}
$$

4 (a) (i) Feedback factor, $\beta=0.09$.
(ii) The new open-loop gain $=A_{i}=103$.

The new closed-loop gain $=A_{f_{1}}=\frac{A_{1}}{1+A_{1} \beta}=\frac{103}{1+103 \times 0.09}=10.03$.
(iii) The percentage change of open-loop gain

$$
\begin{aligned}
& =\frac{\Delta A}{A} \times 100 \\
& =\frac{A-A_{1}}{A} \times 100=\frac{10^{5}-103}{10^{5}} \times 100 \\
& =99.9 \text { per cent. }
\end{aligned}
$$

The percentage change of closed-loop gain

$$
=\frac{\Delta A_{f}}{A_{f}} \times 100=\frac{10^{2}-10.03}{10^{2}} \times 100=89.7 \text { per cent. }
$$

(b) For an amplifier, the gain bandwidth product is always constant. So, $A B=A_{f} B_{f}$, where $A=$ gain without feedback, $A_{f}=$ gain with feedback, $B=$ bandwidth without feedback and $B_{f}=$ bandwidth with feedback.
Now,

$$
A_{f} B_{f}=A B \Rightarrow B_{f}=\frac{A B}{A_{f}}=\frac{A-B}{\left(\frac{A}{1+A B}\right)} \beta(1+A \beta)
$$

For the bandwidth with feedback $B_{f}, D_{f}$ is equal to the distortion with feedback and $D$ is the distortion without feedback.

$$
D_{f}=\frac{D}{1+A \beta}
$$

Here, distortion decreases with negative feedback.
5 (a) The differences between voltage-divider bias and self-bias circuits are as follows.

(b) At the input side,

$$
\begin{gathered}
I_{1}=I_{2} \Rightarrow I_{B}=0 . \\
V_{B}=V_{R_{2}}=\frac{V_{c c} \times R_{2}}{R_{1}+R_{2}}=\frac{18 \times 510}{510+510}=9 \mathrm{~V}
\end{gathered}
$$

Applying KVL on the input side, we get

$$
\begin{aligned}
& V_{B}-V_{B E}-1_{E} R_{E}+18=0 \\
\Rightarrow & 9-0.7-1_{E} \times 7.5 \times 10^{3}+18=0 \\
\Rightarrow & 1_{E}=3.5 \times 10^{-3} \mathrm{~A} \\
\Rightarrow & I_{C}=3.5 \times 10^{-3} \mathrm{~mA} . \text { or } 1 \mathrm{E} \\
& I_{B}=\frac{I_{C}}{\beta}=\frac{3.5 \times 10^{-3}}{130}=26 \mu \mathrm{~A} .
\end{aligned}
$$



Figure 22(a) A self-biased circuit

At the output side, on applying KVL, we get

$$
\begin{aligned}
& V_{C C}-1_{C} R_{C}-V_{C t} \\
& \quad-1_{E} R_{E}+18=0 \\
& 18-V_{C t}-1_{C}\left(R_{C}+R_{E}\right)+18=0 \\
& \Rightarrow V_{c t}=36+1_{c}\left(R_{c}+R_{t}\right) \\
& \Rightarrow 36+3.5 \times 10^{-3}(9.1+7.5) \times 10^{3} \\
& \Rightarrow V_{C E}=94.1 \mathrm{~V} .
\end{aligned}
$$



Figure 22(b) The transistor circuit
6 (a) Refer to Section 8-4 on Page 8-5.
(b) Refer to Section 8-5-2 on Page 8-7.

7 (a) According to the commutative law, $A+B=B+A, A B=B A$.
As per the associative law, $(A+B)+C=A+(B+C),(A B) C=A(B C)$.
(b) According to De Morgan's theorem, $\overline{A B}=\bar{A}+\bar{B}, \overline{A+B}=\bar{A} \cdot \bar{B}$.

$$
\begin{aligned}
Y & =\overline{A \bar{B}+\bar{C} D+E F}=\overline{A \bar{B} \cdot \overline{\bar{C}} \cdot \overline{E F}} \\
& =(\bar{A}+B)(C+\bar{D})(\bar{E}+\bar{F}) \\
& =\bar{A} C \bar{E}+\bar{A} \bar{D} \bar{E}=B C \bar{E}+B C \bar{F}+B \bar{D} \bar{E}+B \bar{D} \bar{F}
\end{aligned}
$$

(c) (i) Given that: $A B+A(B+C)+B(B+C)$. Now,

$$
\begin{aligned}
& =A B+A B+A C+B B+B C \\
& =A B+A C+B+B C \\
& =B(A+1+C)+A C \\
& =B+A C \quad[\text { since } A \cdot A=A \text { and } A+1=1] .
\end{aligned}
$$

(ii) Given that: $(A B(C+B D)+A B) C$. Therefore,

$$
=(A \bar{B} C+A \bar{B} B D+\bar{A} \bar{B}) C
$$

We know that $B \cdot \bar{B}=0$. So,

$$
(A \bar{B} C+\bar{A} \bar{B} C)
$$

8 (a) (i) $\overline{W X Y Z}=\overline{W+X+Y+Z}$ or $\overline{W+X+Y+Z}=\bar{W}+\bar{X}+\bar{Y}+\bar{Z}$.
(ii) $\overline{\bar{W}} \bar{X} \bar{Y} \bar{Z}=\overline{\bar{W}}+\overline{\bar{X}}+\overline{\overline{Y Z}}=W+X+Y Z$.
(iii) $\overline{A+B+\bar{C}}+D(\overline{E+\bar{F}})=\bar{A} \bar{B} \bar{C}+\bar{D}+(\overline{E+\bar{F}}) \bar{A} \bar{B} \bar{C}+\bar{D}+\bar{E} F$.
(b) The given expression can be tabulated as shown below:

| $X$ | $Y$ | $Z$ | $X+\bar{Y}+Z$ | $\bar{X}+Y+Z$ | $X+Y+\bar{Z}$ | $X+\bar{Y}+\bar{Z}$ | $f$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |
| $\mathbf{0}$ | $\mathbf{0}$ | $\mathbf{1}$ | $\mathbf{1}$ | $\mathbf{1}$ | $\mathbf{1}$ | $\mathbf{1}$ | 0 |
| $\mathbf{0}$ | $\mathbf{1}$ | $\mathbf{0}$ | $\mathbf{0}$ | $\mathbf{1}$ | $\mathbf{1}$ | $\mathbf{1}$ | 0 |
| $\mathbf{0}$ | $\mathbf{1}$ | $\mathbf{1}$ | $\mathbf{1}$ | $\mathbf{1}$ | $\mathbf{1}$ | $\mathbf{0}$ | $\mathbf{0}$ |
| $\mathbf{1}$ | $\mathbf{0}$ | $\mathbf{0}$ | $\mathbf{1}$ | $\mathbf{0}$ | $\mathbf{1}$ | $\mathbf{1}$ | $\mathbf{0}$ |
| 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| $\mathbf{1}$ | $\mathbf{1}$ | $\mathbf{1}$ | $\mathbf{1}$ | $\mathbf{1}$ | $\mathbf{0}$ | $\mathbf{1}$ | $\mathbf{0}$ |

Here, $f=(X+\bar{Y}+Z)(\bar{X}+Y+Z)(X+Y+\bar{Z}) \cdot(\bar{X}+\bar{Y}+\bar{Z})(X+\bar{Y}+\bar{Z})$, where $f=0$ for the values marked in bold.

## Biju Patnaik University of Technology Basic Electronics (Common for all Branches of Engineering) Subject Code: BE-2101 2011

1 (a) The $p-n$ junction diode is usually made up of $\mathrm{Si}, \mathrm{Ge}$, or GaAs. Which of the material has the highest basic potential?
(b) Why are the configurations of an open-loop op-amp not used in linear applications?
(c) Determine the DC resistance of a diode of $V_{D}=-20 \mathrm{~V}$ if its reverse saturation current is $1 \mu \mathrm{~A}$.
(d) What is a load line? How it is used to calculate the operating point?
(e) The CMRR of a differential amplifier is 55 dB . If its gain in differential mode $\left(A_{D}\right)$ is 1,200 , then calculate its gain in the common mode $\left(A_{C M}\right)$.
(f) What are the virtual short circuit and the virtual ground concept in op-amps.
(g) Write down the De Morgan's Theorem. Also show the corresponding logic diagram.
(h) What is a Lissajous pattern? Write down its uses.

2 (a) What is the condition of oscillation? Derive the expression of frequency of oscillation and also the condition of oscillation in an RC-phase shift oscillator.
(b) Implement the function $f(A, B, C, D)=\sum m(1,3,4,11,12,13,14,15)$ using multiplexers. Also implement the function into NAND only logic after simplifying the expression.

3 Calculate the output of the diode circuit shown below. Input is a sinusoidal signal.


4 A crystal diode having an internal resistance $r_{f}=20 \Omega$ is used for full-wave rectification. If the applied voltage $V=50 \sin 2 t$ and the load resistance $R_{L}=800 \Omega$, determine the following:
(a) $I_{m}, I_{d e}, I_{r m s}$ of output.
(b) AC power input and DC power output.
(c) The Ripple factor.

5 (a) A transistor has $I_{B}=100 \mu A$ and $I_{C}=2 m A$. Find $\alpha$ and $\beta$ of the transistor. If $I_{B}$ changes by $+25 \mu A$ and $I_{c}$ by +0.6 mA , find the new value of $\beta$.
(b) Why are biasing circuits required for a transistor? Discuss the different biasing techniques.

6 (a) Derive an expression for the sum and carry output of a full-adder circuit. Also implement the full adder using two half adders and an OR gate.
(b) What is a differenctial amplifier? Derive an output voltage expression for the difference amplifier.

7 Write short notes on any two of the following:
(a) Working principle of a CRT display
(b) Function generator
(c) Clipper and clamper
(d) Instrumentation amplifier

## Solutions

1 (a) A p-n junction diode made up of silicon has the highest barrier potential.
(b) Open-loop op-amp configurations are not used in linear application because they have an unstable operation capacity.
(c) The DC resistance of a diode at $V_{D}=-20 V$. If its reverse saturation current is $1 \mu A$, then $R_{D}=\frac{-20 \mathrm{~V}}{1 \mu \mathrm{~A}}$.
(d) The line which is plotted on an output characteristics curve is called a load line. The intersection point of the load line and the characteristics curve is called operating point.


Figure 23 A load line diagram of the output characteristics of a transistor
(e) Given that $C M R R$ is equal to $55 d B$. Now,

$$
\begin{aligned}
A D & =1,200=20 \log 1,200 \\
A C M & =\frac{A d}{55 d B} \\
C M R R_{d B} & =20 \log _{10} \frac{A D}{A C M} .
\end{aligned}
$$

(f) Refer to Section 1-5-19 on Page 1-8.
(g) Refer to Section 9-6 on Page 9-14.
(h) Refer to Section 8-5 on Page 8-6.

2 (a) The two conditions of oscillation are:
(i) The $A v \beta$ loop gain must be at least 1 .
(ii) The total phase shift of the loop gain, $A v \beta$, must be equal to $0^{\circ}$ or $360^{\circ}$.

The RC-phase shift oscillator is shown in Figure 24.


Figure 24 The RC-phase shift oscillator

The condition under which oscillation occurs in the RC-phase shift is when the total phase shift around the loop is $360^{\circ}$ or $0^{\circ}$. The frequency is called the frequency of oscillation, $f_{o}$, and is given by

$$
f_{0}=\frac{1}{2 \pi \sqrt{b} R C}=\frac{0.065}{R C}
$$

At this frequency, $A V \cong 29$. So,

$$
\begin{aligned}
& \left|\frac{R_{f}}{R_{1}}\right|=29 \\
& \Rightarrow R_{f}=29 R_{1}
\end{aligned}
$$

(b) Given that: $F(A, B, C, D)=\Sigma m(1,3,4,11,12,13,14,15)$.


Figure 25 A 16:1 multiplexer-based function realization

Simplifying this expression using the NAND gates, we have

$$
\begin{aligned}
F(A, B, C, D) & =\Sigma \mathrm{m}(1,3,4,11,12,13,14,15) \\
& =m_{1}+m_{3}+m_{4}+m_{11}+m_{12}+m_{13}+m_{14}+m_{15} \\
& =0001+0011+0100+1011+1100+1101+1110+1111 \\
& =\bar{A} \bar{B} \bar{C} D+\bar{A} \bar{B} C D+\bar{A} B \bar{C} \bar{D}+A \bar{B} C \bar{D}+A B \bar{C} \bar{D}+A B \bar{C} D+A B C \bar{D}+A B C D \\
& =\bar{A} \bar{B} D(C+\bar{C})+B \bar{C} \bar{D}(A+\bar{A})+A \bar{B} C D+A B \bar{D}(C+\bar{C})+A B C D \\
& =\bar{A} \bar{B} D+B \bar{C} \bar{D}+A B \bar{D}+A C D \\
& =\overline{\bar{A} \bar{B} D+B \bar{C} \bar{D}+A B \bar{D}+A C D} \\
& =\overline{\overline{\bar{A} \bar{B} D}+\overline{B \bar{C} \bar{D}}+\overline{A B \bar{D}}+\overline{A C D}} .
\end{aligned}
$$

The logic diagram for this is given in Figure 26.


Figure 26 A logic diagram for function realization

3 During the positive half-cycle, the silicon diode's forward-biased short circuit, $V_{D}=0.7 \mathrm{~V}$.


Figure 27(a) The forward-biased condition of a silicon diode

The output voltage,

$$
\begin{aligned}
V_{0}-0.7 \mathrm{~V}+4 \mathrm{~V} & =0 \\
V_{0} & =-3.3 \mathrm{~V} .
\end{aligned}
$$

During the negative half-cycle, the silicon diode is reverse biased. So, there is an open circuit.

$$
\begin{aligned}
V_{0}+5 v & =0 \\
\Rightarrow V_{0} & =-5 v .
\end{aligned}
$$



Figure 27(b) The reverse-biased condition of a silicon diode

4 (a) Given that:

$$
\begin{aligned}
r_{f} & =20 \Omega \\
R_{L} & =800 \Omega \\
V & =50 \sin 2 f \\
V_{m} & =50 v .
\end{aligned}
$$

This is a full-wave rectifier. So,

$$
\begin{aligned}
I_{m} & =\frac{V_{m}}{r_{f}+R_{L}}=\frac{50}{20+800}=\frac{50}{820}=0.060 \mathrm{damp} \\
I_{d e} & =\frac{2 I_{m}}{\pi}=\frac{2 \times 0.0609}{\pi}=0.0388 \mathrm{amp} \\
I_{r m s} & =\frac{I_{m}}{\sqrt{2}}=\frac{0.0609}{\sqrt{2}}=0.0430 \mathrm{amp}
\end{aligned}
$$

(b)

$$
\begin{aligned}
P_{a c} & =I^{2} r m s\left(R_{f}+R_{L}\right) \\
& =(0.0430)^{2} \times 820 \\
& =1.5161 \mathrm{watt} \\
P_{d c} & =I^{2} d c \times R_{L} \\
& =(0.0388)^{2} \times 800 \\
& =1.204 \mathrm{watt} .
\end{aligned}
$$

Q-34 | Basic Electronics
(c)

$$
\begin{aligned}
R_{C} & =\sqrt{\left(\frac{I_{r m s}}{I_{d e}}\right)-1} \\
& =\sqrt{\left(\frac{0.0430}{0.0388}\right)^{2}-1} \\
& =0.477 .
\end{aligned}
$$

5 (a) Given that: $i_{B}=100 \mu A$ and $i_{C}=2 m A$. Now,

$$
\begin{aligned}
i_{E} & =i_{B}+i_{C} \\
& =2 \mu A+100 \mu A \\
& =2 \times 10^{-3}+100 \times 10^{-6} \\
& =10^{-3}\left(2+100 \times 10^{-3}\right) \\
& =2.1 \times 10^{-3} \\
& =2.1 \mathrm{~mA} . \\
\alpha & =\frac{i_{C}}{i_{E}}=\frac{2 m A}{2.1 \mathrm{~mA}} \\
& =0.95 . \\
\beta & =\frac{i_{C}}{i_{B}}=\frac{2 \mathrm{~mA}}{100 \mathrm{~mA}} \\
& =\frac{2 \times 10^{-3}}{100 \times 10^{-6}} \\
& =\frac{2}{100} \times 10^{3}=20 .
\end{aligned}
$$

If $i_{B}$ changes by $+25 \mu A$ and $i_{C}$ changes by $0.6 m A$, then

$$
\begin{aligned}
i_{B} & =25 \mu A \\
i_{C} & =0.6 \mathrm{~mA} \\
\alpha & =\frac{i_{C}}{i_{E}} \\
& =\frac{0.6 \mathrm{~mA}}{0.625 \mathrm{~mA}} \\
& =96 .
\end{aligned}
$$

$$
\begin{aligned}
i_{B}+i_{C} & =i_{E} \\
i_{E} & =25 \times 10^{-6}+0.6 \times 10^{-3} \\
& =10^{-3}\left(25 \times 10^{-3}+0.6\right) \\
& =10^{-3}(0.025+0.65) \\
& =0.625 \mathrm{~mA} . \\
\beta=\frac{i_{C}}{i_{B}}=\frac{0.6 m A}{25 m A} & =\frac{0.6 \times 10^{-3}}{25 \times 10^{-6}}=0.024 \times 10^{3} \\
& =24 .
\end{aligned}
$$

(b) Refer to Section 5-2 on Page 5-2.
(a) Refer to Section 9-8-1 on Page 9-12.
(b) Refer to Section 6-2-4 on Page 6-3.

7 (a) Refer to Section 8-2 on Page 8-2.
(b) Refer to Section 8-11 on Page 8-22.
(c) Refer to Section 3-6 on Page 3-29.
(d) In an instrumentation amplifier, three op-amps are used. For op-amp ' 3 ', $V_{01}$ and $V_{02}$ are the two inputs. So, this amplifier is a subtractor.

$$
\begin{equation*}
V_{0}=\left(V_{01}-V_{02}\right) . \tag{1}
\end{equation*}
$$

By the nodal analysis (taking the node at $A$ ), we have

$$
\begin{align*}
& \frac{V_{A}-V_{B}}{R_{P}}+\frac{V_{A}-V_{02}}{R}=0 \\
\Rightarrow & \frac{V_{2}-V_{1}}{R_{P}}+\frac{V_{2}-V_{02}}{R}=0 \\
\Rightarrow & \frac{V_{2}}{R_{P}}-\frac{V_{1}}{R_{P}}+\frac{V_{2}}{R}-\frac{V_{02}}{R}=0 \\
\Rightarrow & V_{02}=\left(1+\frac{R}{R p}\right) V_{2}=\left(\frac{R}{R p}\right) V_{1} . \tag{2}
\end{align*}
$$

A circuit diagram of an instrumentation amplifier is shown in Figure 28.


Figure 28 A circuit diagram of an instrumentation amplifier

## INDEX

2-bit down counter, 9-27
2-bit up counter, 9-26-27, 35
4-bit asynchronous binary counter, 9-30

## A

ac-coupled amplifiers, 8-4
active region, 4-14; 5-2, 7-8, 13, 15-16
adder, $1-19,32,48 ; 9-18-19,22,36$
AF signal generator, $8-1,22,24$
amplifier, 1-1,4
analog CRO, 8-11
analog signal, 1-3
AND gate, $9-9-10,12-13,15,18,20$
asynchronous counter, 9-27, 29
asynchronous sequential circuits, 9-23
avalanche breakdown, 2-39-43, 47, 53; 3-60; 4-37.
See also breakdown diode
avalanche multiplication, 2-40, 53

## B

bandwidth stability, 6-1, 18
Barkhausen criterion, 6-6, 21-22, 43; 7-11, 30-31
barrier filed, effect on doping, 2-5
base-emitter loop, 2-5
basic amplifier, 6-2-5, 7-8, 14-15, 28, 32-33, 39
biasing, 5-1-2, 5-6, 13-14, 27, 29; 7-2
binary number, 9-2-5; 9-7, 35
conversion to decimal, 9-3
bipolar junction transistor (BJT), 4-1, 34
common-base (CB) mode, 4-8
common-collector (CC) mode, 4-9
common-emitter (CE) mode, 4-8
current gain, 4-10-12
energy band diagrams, 2-1-2, 6; 4-1, 3
formation of $\boldsymbol{p - n - p}$ and $\boldsymbol{n - p}-\boldsymbol{n}$ junctions, 4-12
load line, 4-18
n-p-n transistor, 4-2; 5-2, 29, 31
operating point, 4-17-18; 5-2; 6-1; 7-12
transistor characteristics, 4-1, 12; 5-2, 27
transistor current components, 4-1, 4
transistor mechanism, 4-1-2
bits, $9-1,4,18,20,31-33$
block diagrams, 6-1-2, 44; 7-2; 9-36
Boolean algebra, 9-1, 5, 14
addition, 9-5-6
laws of, 9-1, 5, 8
subtraction, 1-47; 9-5, 7
Boolean expression, 9-1, 15
simplification of, 9-1, 2, 15
boost converter, 3-42-43
breakdown diode, 2-1, 33, 38, 52-53
avalanche breakdown, 2-1, 39-43, 47; 3-60; 4-37
Zener breakdown, 107
bridge rectifier, 3-13-14, 26, 57, 60-62
advantages of, 3-14
disadvantages, 3-14
bridge type full-wave rectifier, 3-12
broad-bandwidth amplifer, 8-4
buck converter, 3-40
buck-boost converter, 3-43
built-in potential, 2-1, 4-5, 7, 58, 60

## C

cascode crystal oscillator, 7-26
cathode-ray oscilloscope (CRO), 8-1
analog CRO, 8-11
digital CRO, 8-11
measurement of frequency, 8-6
measurement of phase, 8-6, 7
storage CRO, 8-11
cathode-ray tube (CRT), 8-1-2, 11
deflection systems, 8-12-13, 18
electron gun, 8-2, 11-12, 24
fluorescent screen, 8-11-13, 15-16, 18, 24, 26
centre-tapped transformer full-wave rectifier, 3-12
centre-tapped transformer rectifier, 3-13
charge conservation equation. See continuity
equation
circuit configurations, 5-1; 9-26
clamper, 3-1, 29, 35, 37, 58
clipper, 3-1, 29-32, 38, 58, 62
series clipper, 3-29, 30
parallel clipper, 3-29, 31-32
collector current, 4-6
collector current stability, 5-11
collector junction (JC), 4-2
collector-base junction, 4-3
collector-emitter loop, 5-3, 5
Colpitt oscillator, 7-1, 6-7, 15, 20, 24, 26-32
combinational logic circuit, 9-17-18, 20-21, 23
common base mode, $4-8,13,34,36 ; 5-14$
input characteristics, 5-14
output characteristics, 5-14-15
common-base (CB) mode, 4-8
common-collector (CC) mode, 4-9
common-emitter (CE) mode, 4-8; 5-12
input characteristics, 5-12
output characteristics, 5-13
common-mode rejection ratio (CMRR), 1-13, 47
common-mode signal voltage, 1-13
common-mode voltage, 1-13-15, 47
comparator, 1-25
comparator, 1-17, 25-26, 50; 3-1, 38-39, 58. See
also diode circuits
counter circuit, 9-26
crystal oscillator, 7-1, 13, 15, 26-27, 29-31
current gain $\left(A_{l}\right), 4-26$
current gain, 4-10-11
current-series feedback, 6-7
current-shunt feedback, 6-7
cutin voltage, 2-27; 3-38
cut-off region, 4-16

## D

Darlington pair, 5-25
dc-coupled amplifiers, 8-4
de-multiplexer, 9-19, 20, 35-37
decimal number, 9-3-4
conversion to binary, 9-3
decoder, 9-20-22, 35-37
deflection systems, 8-12-13, 18
De Morgan's theorem, 9-1-2, 15, 36
de-sensitivity, 6-4, 17
difference signal voltage, 1-13-14
differential input resistance, 1-13
differentiator, 1-19, 29-30, 48-51; 8-1
differentiator output waveform, 1-30
diffusion equation. See continuity equation
diffusion process, 2-2
digital circuits, 3-39; 5-25; 9-2, 8; 9-35
applications of, 9-35
digital CRO, 8-11
digital logic inverter, 1-5
digital signal, 1-3
diode circuits, $3-1,3,5,7,9,11,65$
analysis of, 3-1
digital circuits, 3-40
load line and $Q$-point, 3-2-4
peak detector, 3-39-40
rectifiers, 3-10-21
switching regulator, 3-40
voltage multiplier, 3-39
Zener diode, 3-4-7
diode, 1-1, 30-31; 2-1; 3-1-2; 4-4, 11; 7-27; 8-4, 6
applications of, 3-53-54
$\boldsymbol{p}-\boldsymbol{n}$ junction diode, 2-1-2
direct recombination,
direct/delay flip-flop, 9-25
dual-beam CRO, 8-11
duality, 9-8
dynamic random access memory (DRAM), 9-33

## E

early effect, 4-19
Ebers-Moll model, 4-1, 11-12, 34, 36
electron gun, 8-2, 11-12, 24
electrostatic deflection, 8-12, 13, 24-25
emitter junction (JE), 4-2
emitter, 4-2
emitter-base junction, 4-3
encoder, 9-20-21, 35-36
energy band diagrams, 2-1-2, 6; 4-1, 3
Esaki diode. See tunnel diode

## F

fain -in,
fan-out, 9-13
feedback amplifier, 6-1-11, 13-17, 19-21
bandwidth stability, 6-1, 10
block diagrams, 6-1-2, 44; 7-2; 9-36
effect of positive feedback, 6-1, 19
effect on input impedance, 6-9
effects on output impedance, 6-11-13
loop gain, 6-6
negative feedback, 6-4
practical implications of, sensitivity, 6-17-18
topologies of, 6-1, 7, 44
FET biasing,
filter, 3-14
rectification and, 3-1
fixed bias, 5-2-4, 29
with emitter resistance, 4-38; 5-4
fixed-bias circuit, 5-2-4
flip-flop, 6-2; 9-23-28, 30-31, 37
fluorescent screen, 8-14-15
forward-biased p-n junction, 2-9; 4-5; 5-14
frequency response, 1-28; 4-1, 28; 5-1; 6-4, 20; 8-4, 5
frequency spectram, 1-3
frequency, measurement of, 8-6
full-wave rectifier, 3-12-14
peak inverse voltage, 3-1, 17, 19, 57, 61
function generator, 8-1, 19, 22-23

## G

gain bandwidth product (GB), 1-18
ground-collector configuration, 4-9

## H

half adder, 9-18-19, 36
half-power frequency, 6-29
half-wave rectifier, 3-10-11
Hartley oscillator, 7-5
homoepitaxy,
hybrid IC,
hybrid parameters, 5-23

## I

IC741C ,
IC symbols, infrared LEDs, 3-51
input capacitance, 1-13
input offset current, 1-8, 10-12
input offset null voltage, 1-12
input resistance, 1-12; 6-33
integrated circuits, advantages, disadvantages, fabrication of resistors , hybrid IC,
monolithic IC,
types of IC chips
integration
scale of,
integrator output waveform, 1-30, 49
integrator, 1-26
inverting configuration, 1-21-22
inverting mode, operation, 1-19-21, 25
ion beam etching ,
ion implantation ,
ionizing radiation detectors, 3-55

J-K flip-flop, 9-25
junction capacitance, 2-11, 13-14, 16-17
junction potential, 2-4

## L

large signal voltage gain, 1-14, 15
latch, 9-23
leakage current, 3-52, 55; 4-6-7
light-emitting diode (LED), 3-58
advantages, 3-50
limitations, 3-50
operation of, 1-19
line regulation, 3-5, 6
linear piecewise models, 2-1, 37
linearly-graded junction, 2-2, 46
Lissajous figures, 8-6
measurement of frequency, 8-6
measurement of phase, 8-6-7
load line, 3-1-4, 7-8, 56, 61; 4-1, 17-18, 37; 5-8-9, 29
load regulation, 3-5, 6, 65
load-line analysis, 3-2
logarithmic amplifier, 1-30
logic gate circuits, $9-1,17$
combinational logic circuit, 9-17-18, 20-21, 23
sequential logic circuit, 9-17, 22-23
logic gates, $3-55$; 9-1, $8,13-14,17,23,35,37-38$
AND gate, $9-9-10,12-13,15,18,20$
characteristics of, 9-13
NAND gate, 9-10, 13, 15, 35
NOR gate, $9-10-12,15,25$
NOT gate, 1-5; 9-10, 12, 13
OR gate, $9-9,11-12,15,18-19,22,36$
universal gate, $9-11-13,36$
XNOR gate, 9-11-12
XOR gate, 9-11-13, 18, 36
loop gain, 6-6

## M

Multiplexer, 9-19-20, 35-37

## N

NAND gate, $9-10,13,15,35$
narrow-bandwidth amplifier, 8-4
negative feedback, 6-4
negative logic, 9-2, 36
noise margin, 9-14
noise, 9-14
non-inverting configuration, 1-20, 22, 39
non-inverting mode, operation, 1-20, 25
NOR gate, 9-10-12, 15, 25
NOT gate, 1-5; 9-10, 12-13
$\boldsymbol{n}$-p-n transistor, 4-2, 7-9, 19, 21, 23, 25, 38-39; 5-2, 29, 31
current components in, 4-4, 5, 7
number system, 9-1, 2, 4, 37
conversion of, 3-19, 53; 9-1-2, 5
binary to decimal, 9-1-3
decimal to binary, 9-2, 3
Nyquist criterion, 6-20, 44; 7-11
for oscillation, 7-11

## 0

offset minimizing resistor, 1-10
offset voltage adjustment range, 1-13
op-amp. See operational amplifier
operating point, 4-17-18
operational amplifier, $1-1,5,7,9,11,13,15,17-20$, $27,29,37,39,41,51 ; 8-20$
applications of, 1-1, 19; 3-1, 55; 5-1, 26; 6-13; $7-1,31 ; 8-6,25 ; 9-1,22$
common-mode rejection ratio (CMRR), 1-13, 47
differential input resistance, 1-13
input capacitance, 1-13
input offset current, 1-8, 10
input offset null voltage, 1-12
input offset voltage and output offset voltage, 1-8
input offset voltage, $1-8-9,11-13,15,29$
input resistance, 1-12
input voltage range, 1-13
input-bias current, 1-8-11
large signal voltage gain, 1-14-15
offset voltage adjustment range, 1-13
output offset current, 1-10
output offset voltage, 1-8-13
output resistance, 1-15
output voltage swing, $1-15,17$
power consumption, 1-16, 50
properties of, 1-1, 5, 47; 2-52, 56; 6-1, 4; 9-37
slew rate, 1-6, 16-18, 31, 47-50
supply current,1-16
supply voltage rejection ratio (SVRR), 1-15
supply voltage, 1-16
OR gate, $9-9,11-13,15,18-19,21-22,36$
organic field-effect transistor (OFET),
oscillation, 1-44, 45; 6-4, 20-22; 7-1, 4-6, 9-13, 16-22, 24-32; 8-22
Nyquist criterion, 6-20, 44; 7-11
oscillator, 1-48; 6-1, 22; 7-1, 2, 5, 7, 25-26, 28, 30;
8-5-6, 22, 24
applications of, $1-1,19 ; 3-1,35 ; 5-1,26,6-13$; $7-1,31 ; 8-6,25 ; 9-1,22$
cascode crystal oscillator, 7-22, 26
classification of, 7-2; 9-2
Colpitis oscillator,
crystal oscillator, 7-1, 13, 15, 26-27, 29-31
Hartley oscillator, 7-1, 5-6; 7-17-18, 21, 24, 27, 29-32
phase-shift oscillator, 7-1, 7, 9, 27-28, 30-31
tuned oscillator, 7-1, 12, 31; 8-5
voltage-controlled oscillator (VCO), 7-25
Wien-bridge oscillator, 7-1, 9-11, 19, 28, 32;
8-22, 24
oscilloscope amplifiers, 8-4
output offset current, 1-10
output resistance, 1-15-16
output voltage swing, 1-15, 17

## P

parallel clipper, 3-29, 31-32
parallel input parallel output (PIFO) shift register, 9-33
parallel input serial output (PISO) shift register, 9-32
parameter $\alpha^{\prime}$, 4-25
peak detector, 3-39-40
peak inverse voltage (PIV), 3-17
phase, measurement of, 8-6-7
phase-shift oscillator, 7-1, 7, 9, 27-28, 30-31
phosphor, 8-2, 12, 15
photo detector diode, 3-1, 51, 62
photoelectric effect, 3-53
photovoltaic diode, 3-53,
construction and working principle, 3-53
current-voltage characteristics, 3-2, 53
piecewise linear equivalent model, 2-37
$\boldsymbol{p}$ - $\boldsymbol{n}$ junction diode, 2-1-2
breakdown diode, 2-1, 33, 38, 52-53
derivation of the I-V characteristics, 2-1
with external applied voltage, 2-10-11
formation, 2-1-2, 5, 52; 3-51; 4-1-2
light-emitting diode (LED), 3-50
modes of, 2-1, 9
photo detector diode, 3-1, 51, 62
photovoltaic diode, 3-53
rectifying voltage-current characteristics, 2-10
at thermal equilibrium, 2-2, 5-6, 8, 46, 49, 52
tunnel diode, 2-47; 3-47, 49, 62
p-n-p transistor, 4-2-9, 12, 38-40, 42; 5-2
current components in, 4-4-5, 7
positive feedback, effect of, 6-1
positive logic, 9-2
power consumption, 1-16; 3-50
power dissipation, 2-43; 3-63; 4-35; 9-14
power supply rejection ratio (PSRR), 1-15
power supply sensitivity (PSS), 1-15
propagation delay, 9-13

## Q

quiescent point ( $Q$-point), 3-3

## R

radio demodulation, 3-55
random-access memory (RAM), 9-33
recombination, 2-23, 27, 40, 47, 49, 51, 54, 58-60; 3-50; 4-5; 5-13
rectification, 3-1, 10, 14, 18, 20, 61
use of filters in, 3-14
rectifier, 1-48; 2-50; 3-1, 11, 21, 39, 65; 7-1, 27, 31
effectiveness of, 3-18
full-wave rectifier, 3-12-14
half-wave rectifier, 3-10, 12-13
performance analysis of various rectifier circuits, 3-17
regulation, 2-46; 3-4-6, 17, 21-22, 62, 65
reliability, testing for, 3-52
return ratio, 6-6
reverse collector saturation current, 4-5, 6-7
reverse-active region, 4-14
reverse-biased $\boldsymbol{p}-\boldsymbol{n}$ junction, 2-9, 38, 52
ripple factor, 3-1, 14-16, 18-20, 28, 57-58, 62

## S

saturation region, 1-16; 13, 16-17, 35; 5-4, 8, 13, 15
Schmitt trigger circuit, 8-19, 21, 23
self-bias current, 5-5, 8, 9, 20, 29, 30; 6-1
semiconductor memory, 9-33
sensitivity, 6-17-18
sequential logic circuit, 9-17, 22-23
serial input parallel output (SIPO) shift register, 9-31
serial input serial output (SISO) shift register, 9-31
series clipper, 3-29-30
series-series feedback, 6-7
series-shunt feedback, 6-7
set-reset flip-flop, 9-24
shift register, 9-31-33, 35-37
shunt connection, 6-2-3
shunt-series feedback, 6-7-8
shunt-shunt feedback, 6-7-8
signal, 1-2
sine wave generator, 8-1, 19-21
slew rate, 1-6, 16-18, 31, 47-50
solar cell. See photovoltaic diode
space-charge region, 2-4-5; 2-11
spot beam deflection sensitivity, 8-13
square wave generator, 8-1, 20
stability factor S, 5-9-10, 17, 20-21
stabilization factor $S^{\prime}, 5-18$
stabilization factor $\mathrm{S}^{\prime \prime}, 5-18$
stabilization, 5-7, 18
state diagram, 9-26-28
step-graded semiconductor junction, 2-2
storage capacitance, 2-20-21
storage CRO, 8-11
subtractor, 1-24
summing amplifier, 1-21-23, 49-50
supply current, 1-16
supply voltage, 1-15
supply voltage rejection ratio (SVRR), 1-15
sweep frequency generator, 8-1, 5-6
switching regulator, 3-40
boost converter, 3-42-43
buck converter, 3-40
buck-boost converter, 3-43
synchronous counter, 9-30, 37
synchronous sequential circuits, 9-23

## T

time-base generators, 8-1-2
time-base measurement, 8-6
toggle flip-flop, 9-26
total diode-current density, 2-23, 48
transistor
Ebers-Moll model of, 4-1, 11-12
at high frequencies, 5-1, 26
real-life applications of, 5-1, 26; 9-1
as simplifier,
small-signal low-frequency operation of, 5-1, 23
transistor characteristics, 4-1, 12; 5-2, 27
common-base mode, 4-8, 13, 34, 36; 5-14
common-emitter mode, 4-8, 11, 13, 20, 34, 36
input characteristics, 4-12-13, 38; 5-12, 14
output characteristics, 1-22-23; 4-12-13, 17-18, 38-39; 5-5, 13, 15, 23
transistor current components, 4-1, 4
transistor mechanism, 4-1, 2
tuned oscillator, 7-1, 12, 31; 8-5
tunnel diode, 2-47; 3-47, 49, 62
two-port network, 5-1, 23, 25
equivalent circuits through hybrid parameters, 5-1, 25

## U

unity gain amplifier, 1-25
universal gate, 9-11-13, 36

## V

varactor diode, 2-19-20, 50, 52; 3-59-66; 7-26
vertical amplifiers, 8-4
virtual ground, 1-18-19, 31, 48, 50
voltage amplification, 4-24, 27, 38; 6-45
voltage divider bias, 5-5
voltage follower, 1-17-19, 21, 25
voltage gain, 4-27-28
voltage multiplier, 1-47; 3-39, 55, 62
voltage regulator, $3-1,4,9,56,65$
voltage-controlled oscillator (VCO), 7-25
voltage-feedback biasing, 5-6
voltage-series feedback, 6-7, 9
voltage-shunt feedback, 6-9-10, 15, 43

## W

Wien-bridge oscillator, 7-9-10
advantages, 7-9
disadvantages, 7-9

## X

XNOR gate, 9-11-12
XOR gate, 9-11-13, 18, 36

## Z

Zener breakdown, 2-38-44. See also breakdown diode
Zener diode, 3-4
line regulation, 3-5-6
load regulation, 3-5, 6, 65
Zener effect, 2-39; 3-48, 60

